

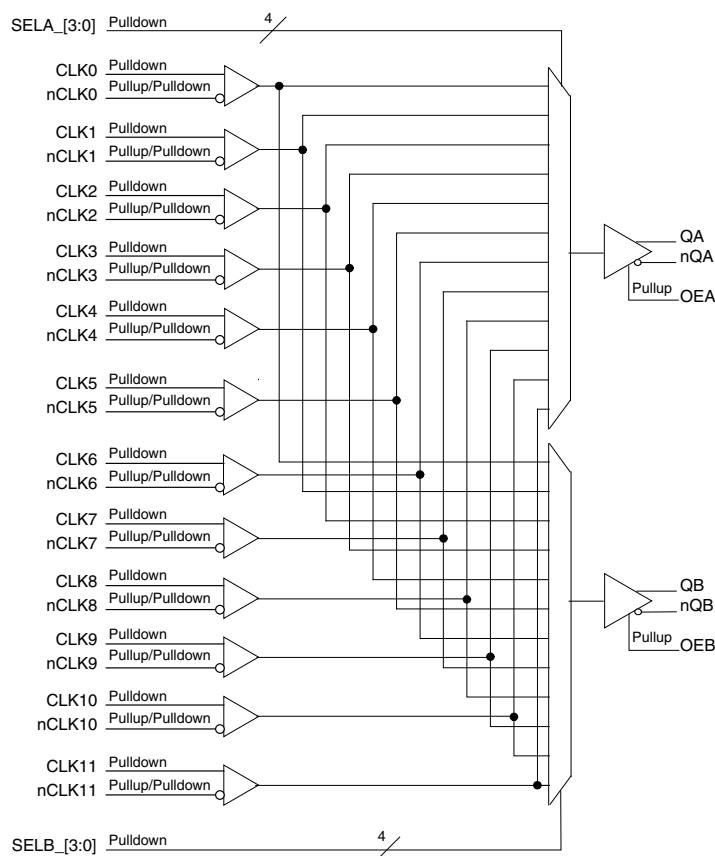
## Description

The 853S202 is a 12:2 Differential-to-LVPECL Clock Multiplexer which can operate up to 3GHz. The 853S202 has twelve selectable differential clock inputs, any of which can be independently routed to either of the two LVDS outputs. The CLKx, nCLKx input pairs can accept LVPECL or LVDS levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits.

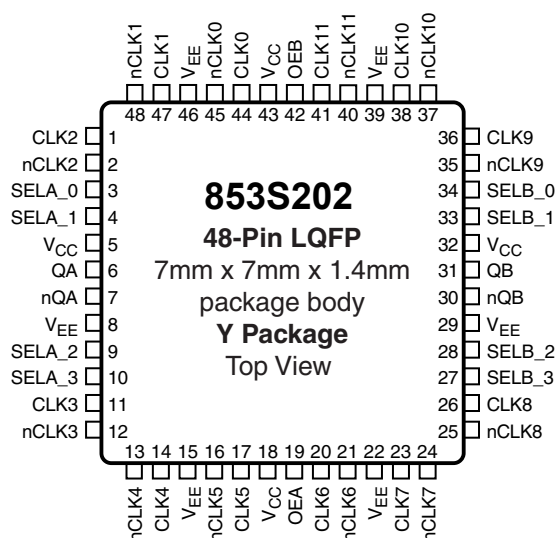
## Features

- High speed 12.2 differential multiplexer
- Two differential 3.3V or 2.5V LVPECL outputs
- Twelve selectable differential clock or data inputs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS
- Maximum output frequency: 3GHz
- Translates any single ended input signal to LVPECL levels with resistor bias on nCLKx input
- Propagation delay: 1.15ns (maximum)
- Input skew: 150ps (maximum)
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Additive phase jitter, RMS: 0.114ps (typical) @ 155.52MHz, 3.3V
- Full 3.3V or 2.5V operating supply mode
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

## Block Diagram



## Pin Assignments



## Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK2	Input	Pulldown	Non-inverting differential clock input.
2	nCLK2	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
3, 4, 9, 10	SELA_0, SELA_1, SELA_2, SELA_3	Input	Pulldown	Clock select pins for Bank A output pair. See Control Input Function Table. LVCMOS/LVTTL interface levels. See Table 3B.
5, 18, 32, 43	$V_{CC}$	Power		Power supply pins.
6, 7	QA, nQA	Output		Clock outputs. LVDS interface levels.
8, 15, 22, 29, 39, 46	$V_{EE}$	Power		Power supply ground.
11	CLK3	Input	Pulldown	Non-inverting differential clock input.
12	nCLK3	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
13	nCLK4	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
14	CLK4	Input	Pulldown	Non-inverting differential clock input.
16	nCLK5	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
17	CLK5	Input	Pulldown	Non-inverting differential clock input.
19	OEA	Input	Pullup	Output enable pin. Controls enabling and disabling of QA, nQA output pair. LVCMOS/LVTTL interface levels.
20	CLK6	Input	Pulldown	Non-inverting differential clock input.
21	nCLK6	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
23	CLK7	Input	Pulldown	Non-inverting differential clock input.
24	nCLK7	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
25	nCLK8	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
26	CLK8	Input	Pulldown	Non-inverting differential clock input.
27, 28, 33, 34	SELB_3, SELB_2, SELB_1, SELB_0	Input	Pulldown	Clock select pins for Bank B output pair. See Control Input Function Table. LVCMOS/LVTTL interface levels. See Table 3C.
30, 31	nQB, QB	Output		Clock outputs. LVDS interface levels.
35	nCLK9	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
36	CLK9	Input	Pulldown	Non-inverting differential clock input.
37	nCLK10	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
38	CLK10	Input	Pulldown	Non-inverting differential clock input.

**Table 1. Pin Descriptions**

Number	Name	Type		Description
40	nCLK11	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
41	CLK11	Input	Pulldown	Non-inverting differential clock input.
42	OEB	Input	Pullup	Output enable pin. Controls enabling and disabling of QB, nQB output pair. LVCMOS/LVTTL interface levels.
44	CLK0	Input	Pulldown	Non-inverting differential clock input.
45	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
47	CLK1	Input	Pulldown	Non-inverting differential clock input.
48	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance			2		pF
$R_{PULLUP}$	Input Pullup Resistor			51		$k\Omega$
$R_{PULLDOWN}$	Input Pulldown Resistor			51		$k\Omega$

## Function Tables

**Table 3A. OEA, OEB Control Input Function Table**

Input	Output
OEA, OEB	QA, nQA, QB, nQB
0	Disabled (Logic LOW)
1	Active (default)

**Table 3B. SEL\_A Control Input Function Table**

Control Input				Input Selected to QA, nQA
SELA_3	SELA_2	SELA_1	SELA_0	
0	0	0	0	CLK0, nCLK0 (default)
0	0	0	1	CLK1, nCLK1
0	0	1	0	CLK2, nCLK2
0	0	1	1	CLK3, nCLK3
0	1	0	0	CLK4, nCLK4
0	1	0	1	CLK5, nCLK5
0	1	1	0	CLK6, nCLK6
0	1	1	1	CLK7, nCLK7
1	0	0	0	CLK8, nCLK8
1	0	0	1	CLK9, nCLK9
1	0	1	0	CLK10, nCLK10
1	0	1	1	CLK11, nCLK11
1	1	0	0	Output at logic LOW
1	1	0	1	Output at logic LOW
1	1	1	0	Output at logic LOW
1	1	1	1	Output at logic LOW

**Table 3C. SEL\_B Control Input Function Table**

Control Input				Input Selected to QA, nQA
SELB_3	SELB_2	SELB_1	SELB_0	
0	0	0	0	CLK0, nCLK0 (default)
0	0	0	1	CLK1, nCLK1
0	0	1	0	CLK2, nCLK2
0	0	1	1	CLK3, nCLK3
0	1	0	0	CLK4, nCLK4
0	1	0	1	CLK5, nCLK5
0	1	1	0	CLK6, nCLK6
0	1	1	1	CLK7, nCLK7
1	0	0	0	CLK8, nCLK8
1	0	0	1	CLK9, nCLK9
1	0	1	0	CLK10, nCLK10
1	0	1	1	CLK11, nCLK11
1	1	0	0	Output at logic LOW
1	1	0	1	Output at logic LOW
1	1	1	0	Output at logic LOW
1	1	1	1	Output at logic LOW

## Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, $\theta_{JA}$	70.2°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Characteristic Tables

**Table 4A. Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current	No Load		85	95	mA

**Table 4B. Power Supply DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current	No Load		80	88	mA

**Table 4C. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		$V_{CC} = 3.3V$	2.2		$V_{CC} + 0.3$	V
			$V_{CC} = 2.5V$	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		$V_{CC} = 3.3V$	-0.3		0.8	V
			$V_{CC} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	SELA_[3:0], SELB_[3:0]	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
		OEA, OEB	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu A$
$I_{IL}$	Input Low Current	SELA_[3:0], SELB_[3:0]	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu A$
		OEA, OEB	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu A$

**Table 4D. Differential DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK[0:11]	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$		150	$\mu A$
		nCLK[0:11]	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$		150	$\mu A$
$I_{IL}$	Input Low Current	CLK[0:11]	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	- 5		$\mu A$
		nCLK[0:11]	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	- 150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage;		0.15		1.5	V
$V_{CMR}$	Common Mode Input Voltage: NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is  $V_{CC} + 0.3V$ .

**Table 4E. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.2$		$V_{CC} - 0.8$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

## AC Characteristics Table

**Table 5A. AC Characteristics**,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				3	GHz
$t_{PLH}$	Propagation Delay, Low to High; NOTE 1		450	600	850	ps
$t_{PHL}$	Propagation Delay, High to Low; NOTE 1		450	600	850	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3			14	50	ps
$t_{sk(i)}$	Input Skew; NOTE 3			30	150	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				250	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	155.52MHz, Integration Range: 12kHz - 20MHz		0.114	0.152	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	55		250	ps
odc	Output Duty Cycle; NOTE 6		40	50	60	%
$MUX_{ISOLATION}$	MUX Isolation	$f_{OUT} < 1.2GHz$		75		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range. Note that phase noise may increase slightly with higher operating temperature. However, they will remain in spec as long as the maximum transistor junction temperature is not violated. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from  $V_{CC}/2$  of the input to  $V_{CC}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{CC}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{CC}/2$ .

NOTE 5: Driving only one input clock.

NOTE 6: The output duty cycle will depend on the input duty cycle.

**Table 5B. AC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				3	GHz
$t_{PLH}$	Propagation Delay, Low to High; NOTE 1		450	630	875	ps
$t_{PHL}$	Propagation Delay, High to Low; NOTE 1		450	630	875	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3			14	50	ps
$t_{sk(i)}$	Input Skew; NOTE 3			35	150	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				250	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	155.52MHz, Integration Range: 12kHz - 20MHz		0.147	0.215	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	55		250	ps
odc	Output Duty Cycle; NOTE 6		40	50	60	%
$MUX_{ISOLATION}$	MUX Isolation	$f_{OUT} < 1.2GHz$		75		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range. Note that phase noise may increase slightly with higher operating temperature. However, they will remain in spec as long as the maximum transistor junction temperature is not violated. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from  $V_{CC}/2$  of the input to  $V_{CC}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{CC}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{CC}/2$ .

NOTE 5: Driving only one input clock.

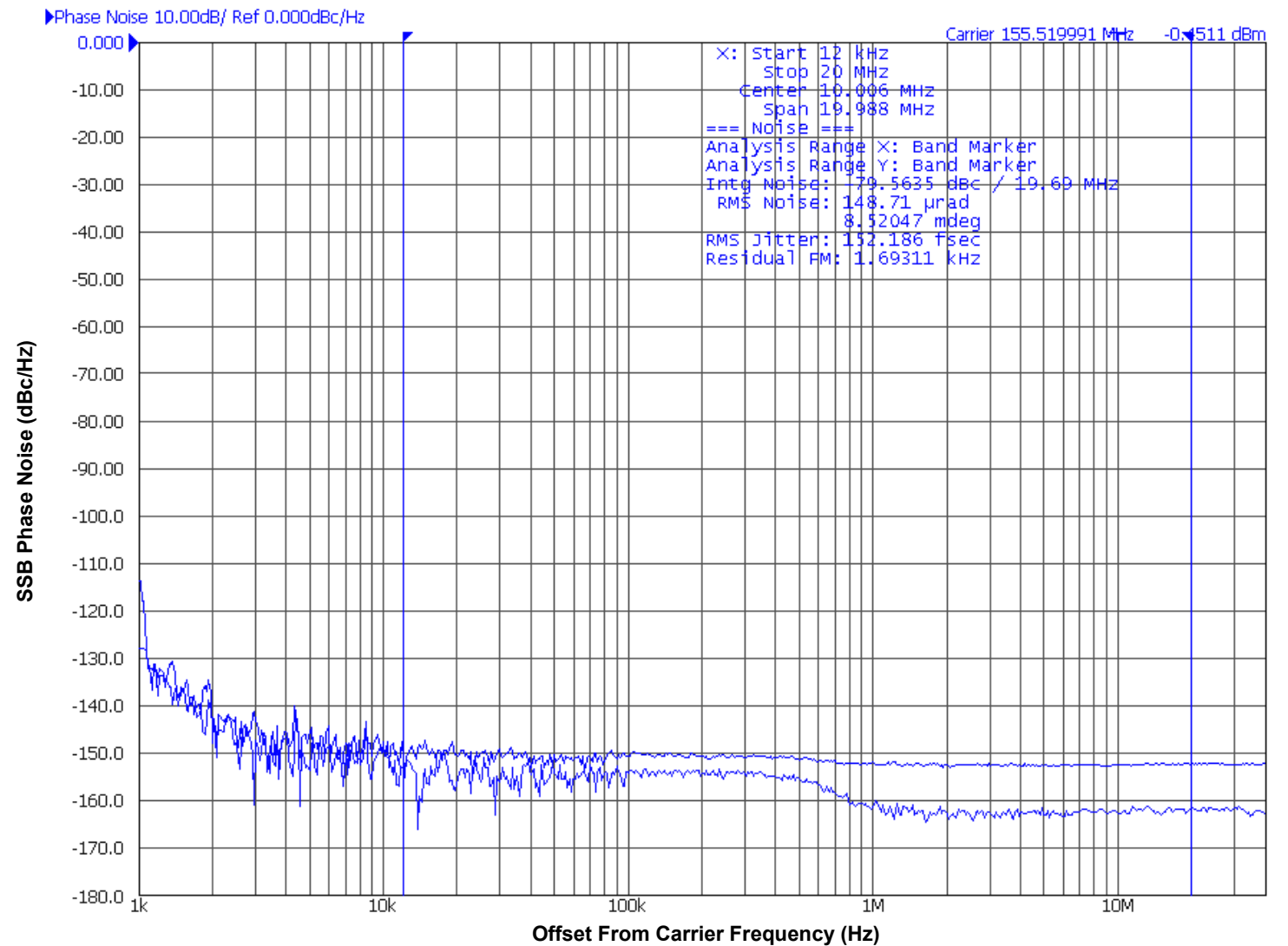
NOTE 6: The output duty cycle will depend on the input duty cycle.



### Additive Phase Jitter (3.3V)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise*. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise

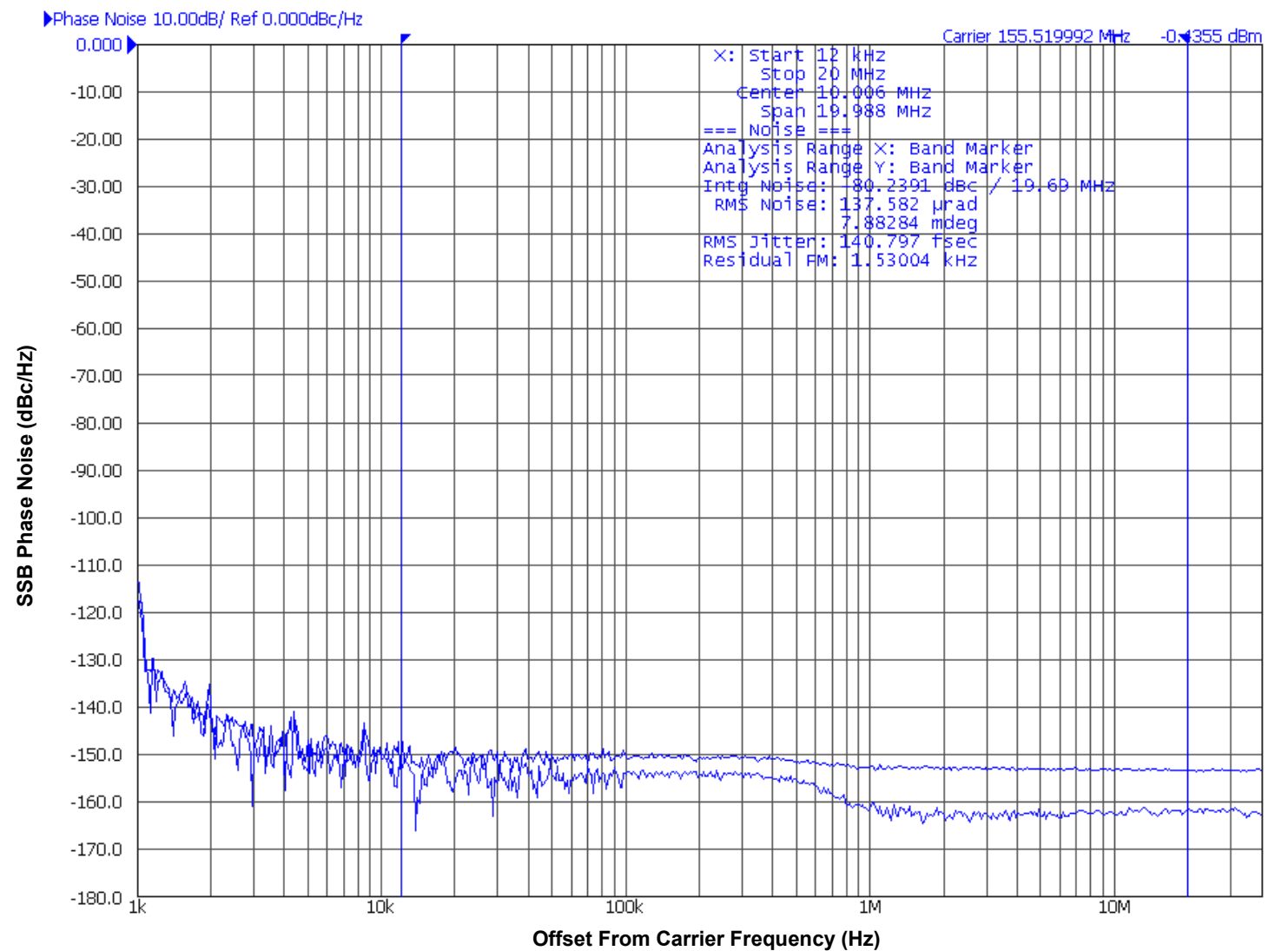
floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using the Rhode & Schwartz SMA100 as the input source.

# Additive Phase Jitter (2.5V)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise*. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

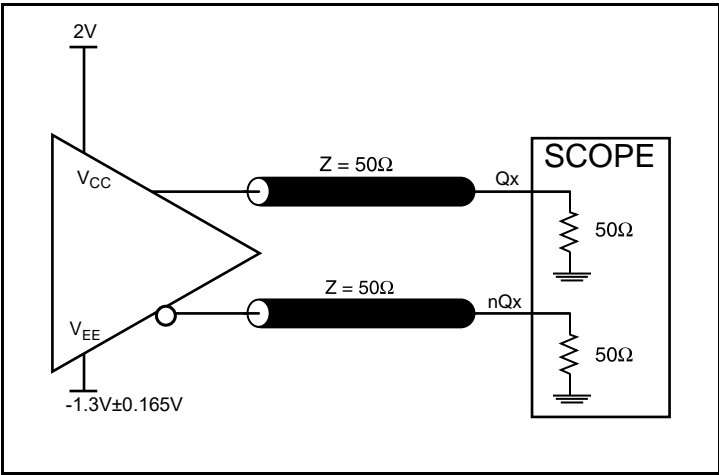


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise

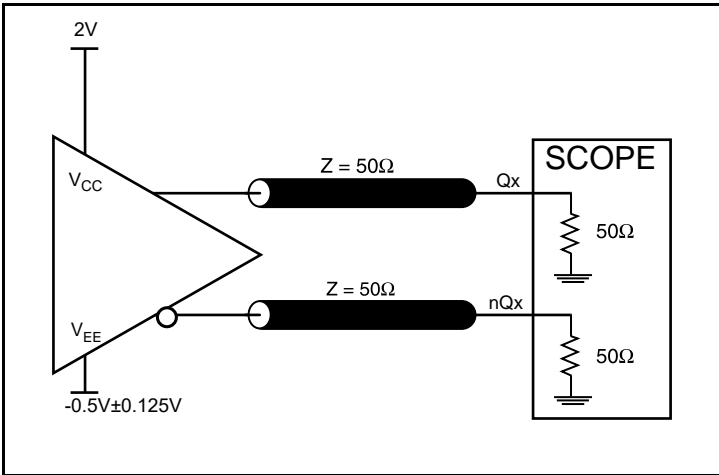
floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using the Rhode & Schwartz SMA100 as the input source.

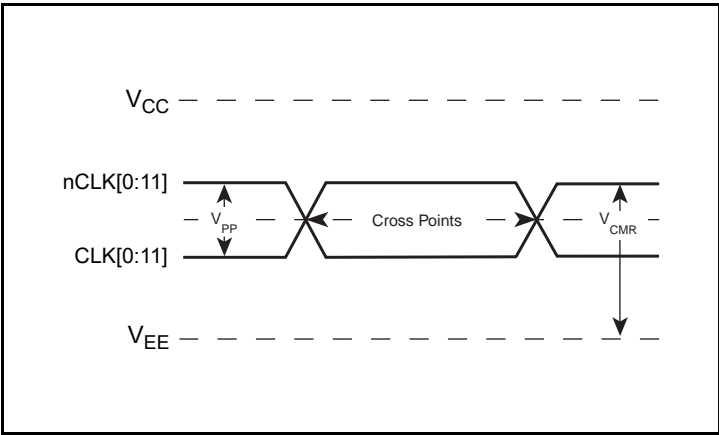
# Parameter Measurement Information



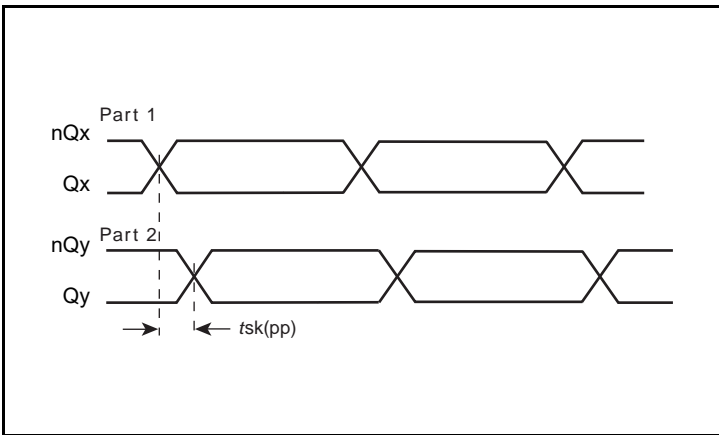
3.3V Output Load Test Circuit



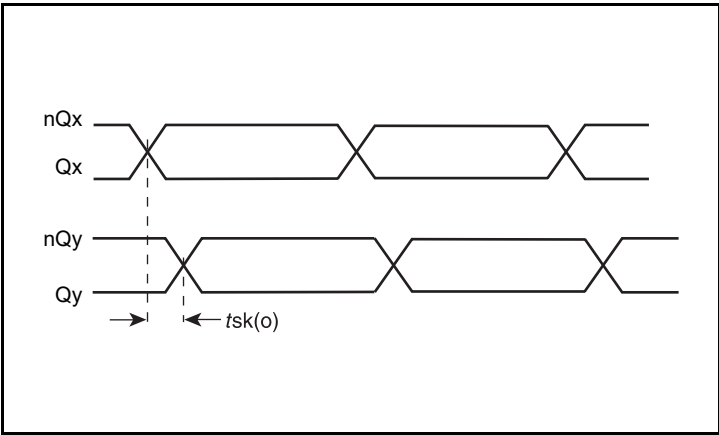
2.5V Output Load Test Circuit



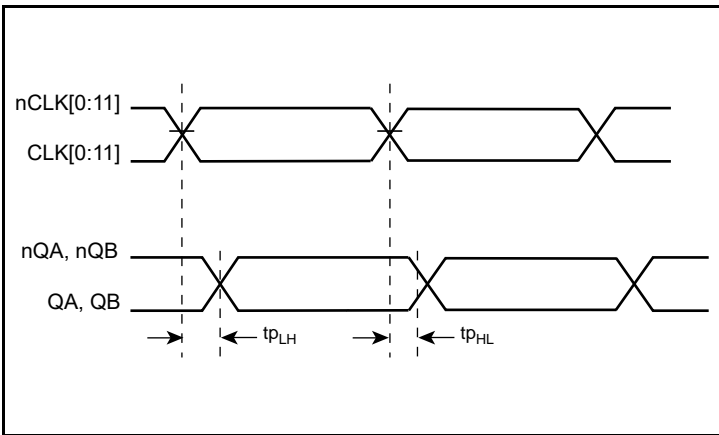
Differential Input Level



Part-to-Part Skew

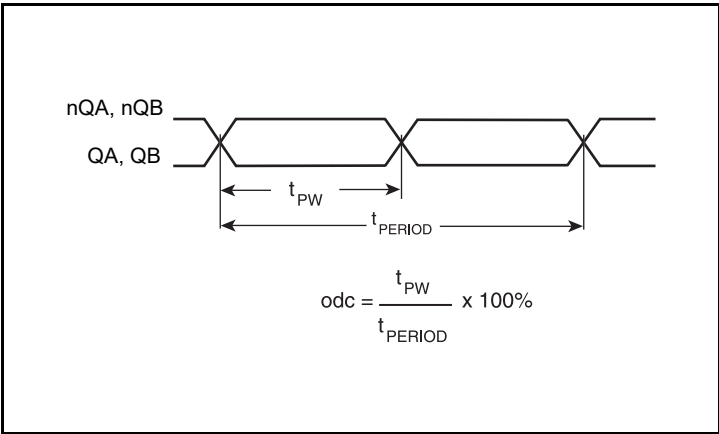


Output Skew

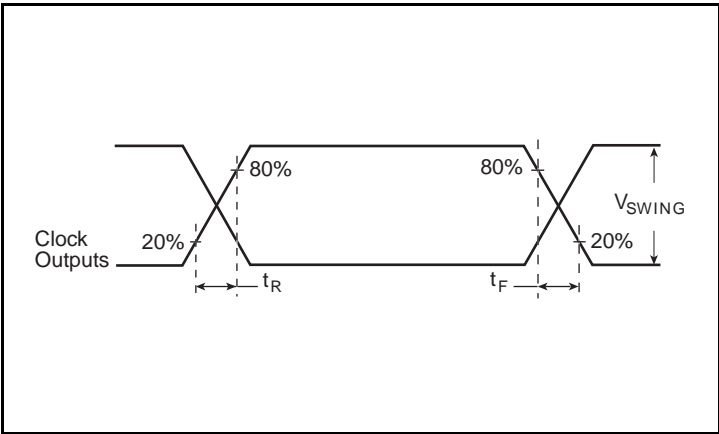


Propagation Delay

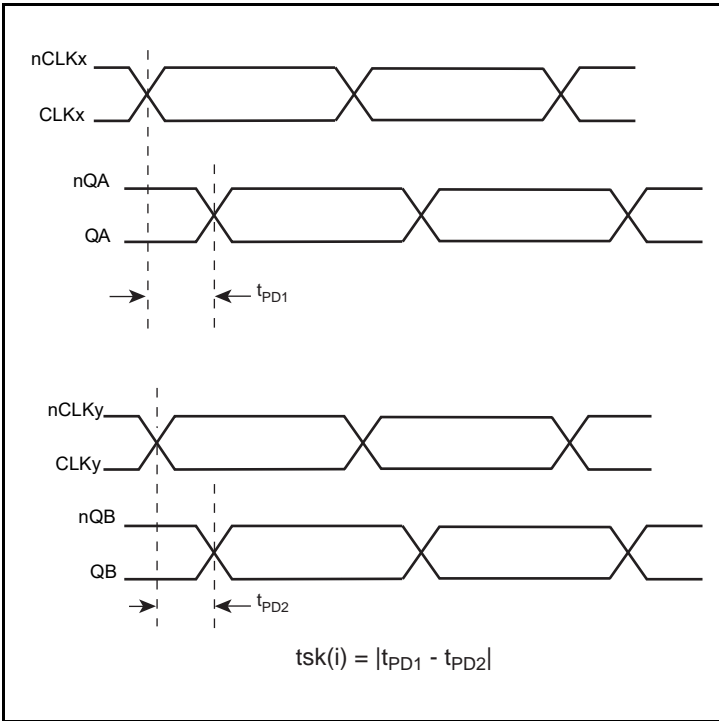
# Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



Input Skew

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### CLK/nCLK Inputs

For applications requiring only one differential input, the unused CLK and nCLK input can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from CLK pin to ground.

##### LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### Outputs:

##### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating, there should be no trace attached

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_1$  at 1.25V. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50 $\Omega$  applications, R3 and R4 can be 100 $\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than -0.3V and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

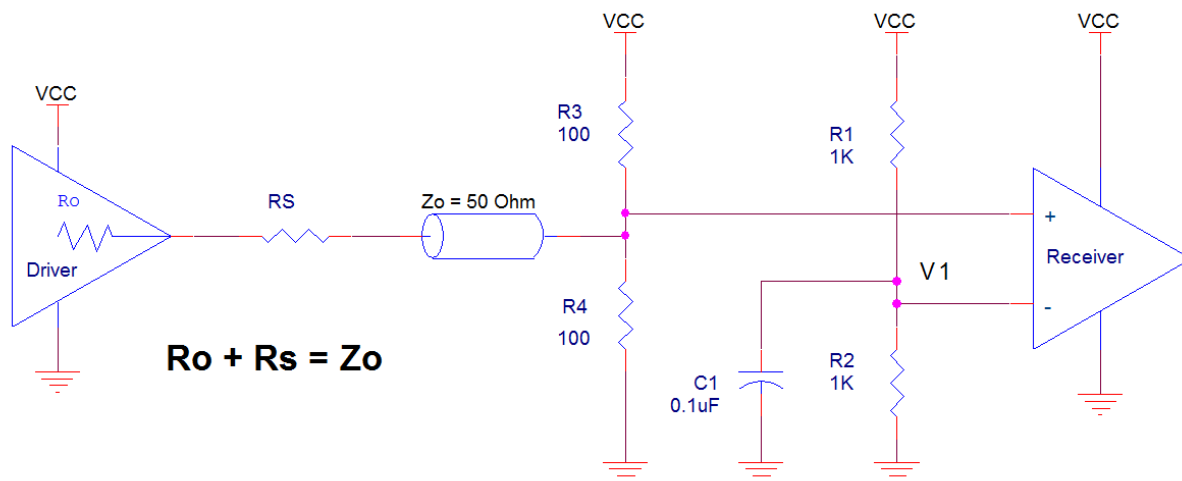
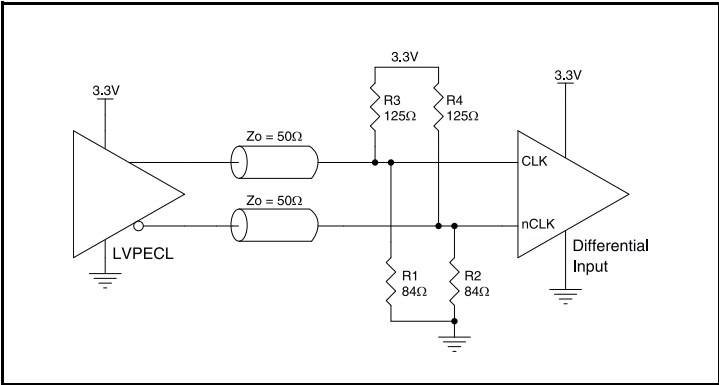


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

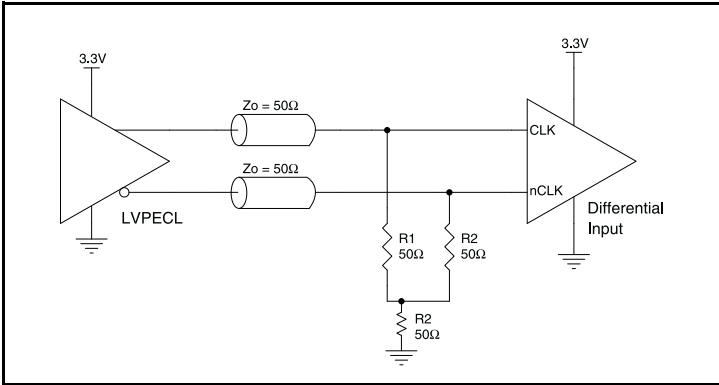
### 3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 2A to 2C* show interface examples for the CLK/nCLK input driven by the most common driver types. The input

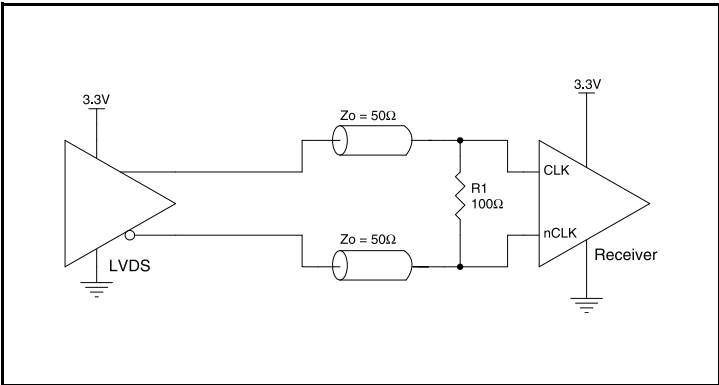
interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 2A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

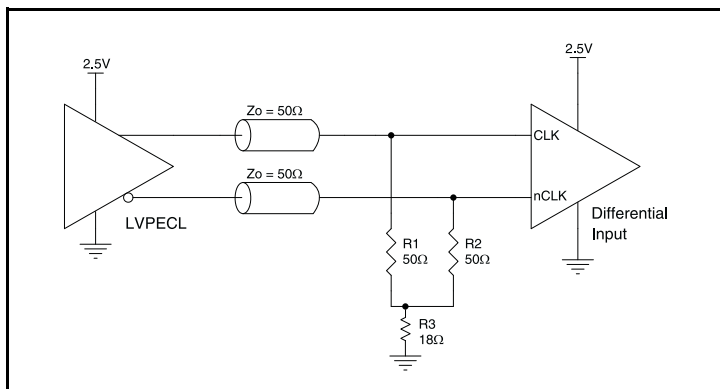


**Figure 2C. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

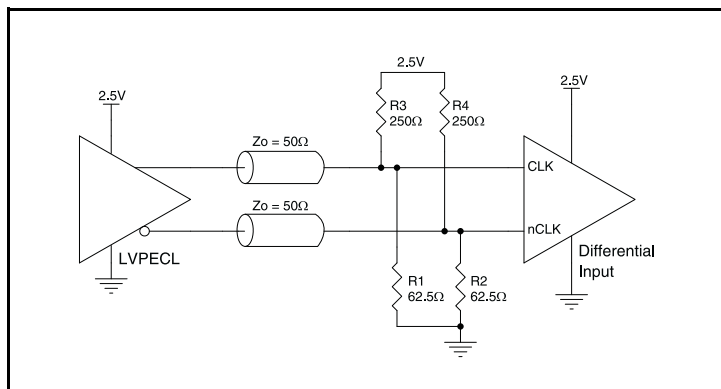
## 2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and other differential signals. Both  $V_{\text{SWING}}$  and  $V_{\text{OH}}$  must meet the  $V_{\text{PP}}$  and  $V_{\text{CMR}}$  input requirements. *Figures 3A to 3C* show interface examples for the CLK/nCLK input driven by the most common driver types. The input

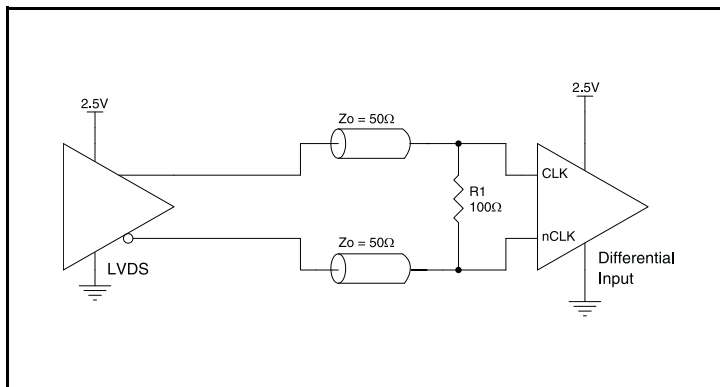
interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 3A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver**



**Figure 3B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver**



**Figure 3C. CLK/nCLK Input Driven by a 2.5V LVDS Driver**

### Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

*Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

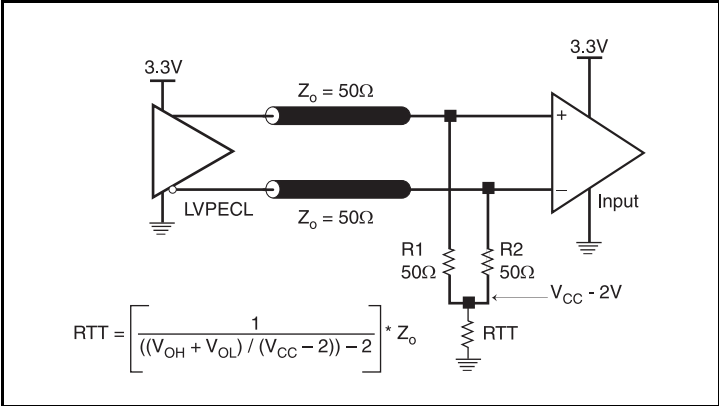


Figure 4A. 3.3V LVPECL Output Termination

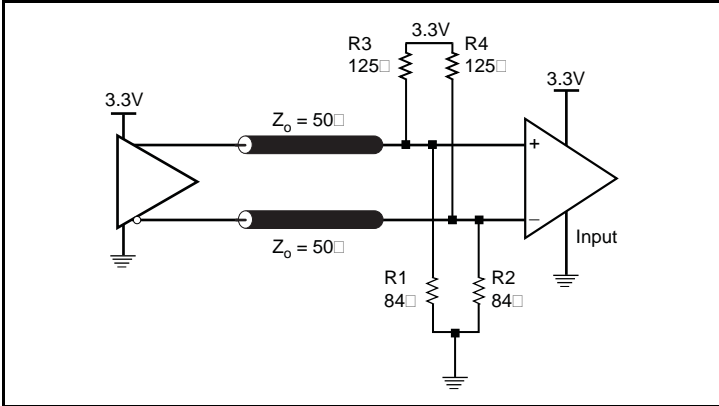


Figure 4B. 3.3V LVPECL Output Termination



## Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground

level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

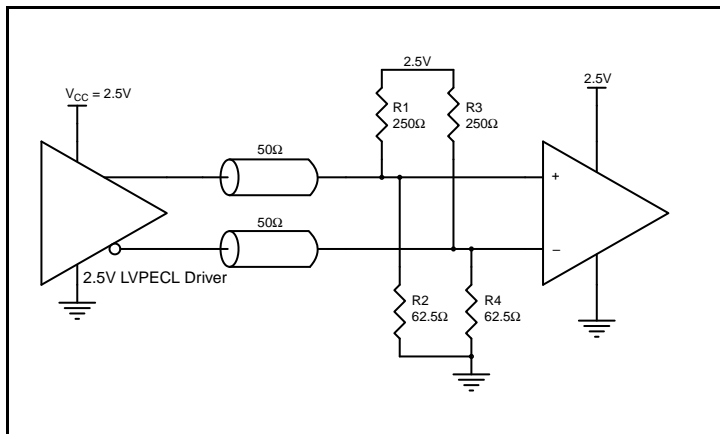


Figure 5A. 2.5V LVPECL Driver Termination Example

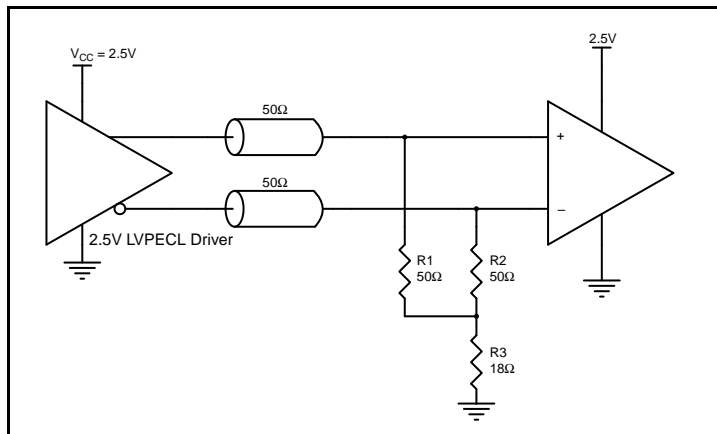


Figure 5B. 2.5V LVPECL Driver Termination Example

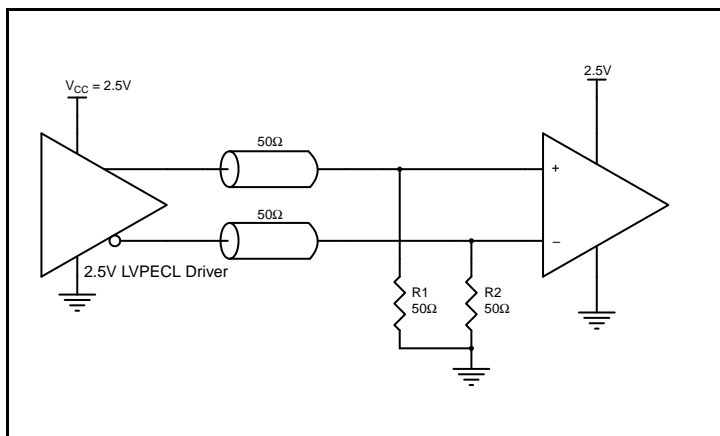


Figure 5C. 2.5V LVPECL Driver Termination Example

# Power Considerations

This section provides information on power dissipation and junction temperature for the 853S202. Equations and example calculations are also provided.

## 1. Power Dissipation.

The total power dissipation for the 853S202 is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 94mA = \mathbf{325.71mW}$
- Power (outputs)<sub>MAX</sub> = **29.4mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 29.4mW = \mathbf{58.8mW}$

**Total Power** (3.465V, with all outputs switching) =  $325.71W + 58.8mW = \mathbf{384.51mW}$

## 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 70.2°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^{\circ}C + 0.385W * 70.2^{\circ}C/W = 112^{\circ}C. \text{ This is below the limit of } 125^{\circ}C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

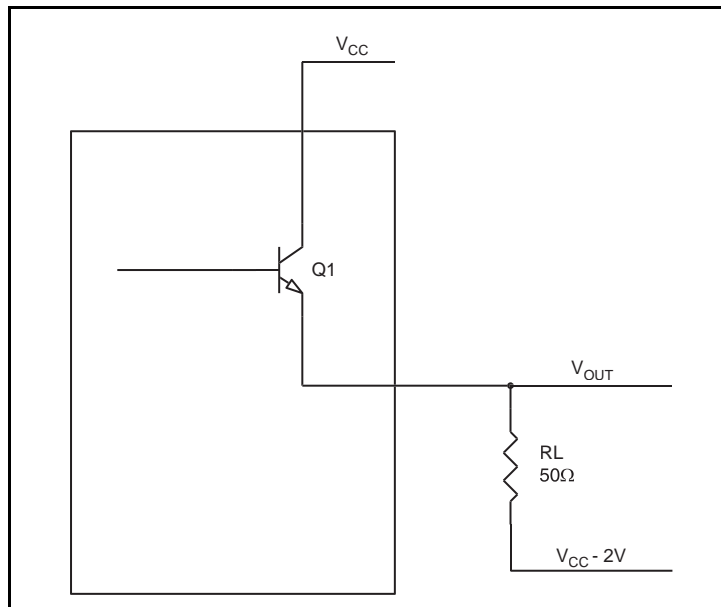
**Table 6. Thermal Resistance  $\theta_{JA}$  for 48 Lead LQFP, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70.2°C/W	60.4°C/W	56.9°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

The LVPECL output driver circuit and termination are shown in *Figure 4*.



**Figure 4. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.8V$   
 $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.8V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$   
 $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.8V)/50\Omega] * 0.8V = \mathbf{19.20mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.20mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{29.4mW}$$

# Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 48 Lead LQFP

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70.2°C/W	60.4°C/W	56.9°C/W

# Transistor Count

The transistor count for 853S202 is: 8,537

# Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available.

# Ordering Information

Table 9. Ordering Information

Orderable Part Number	Marking	Package	Carrier Type	Temperature
853S202AYILF	ICS53S202AIL	Lead-Free 7 x 7 mm, 1.4 pitch 48-LQFP	Tray	-40°C to 85°C
853S202AYILFT	ICS53S202AIL		Tape and Reel	-40°C to 85°C

# Revision History

Revision Date	Description of Change
July 23, 2018	<ul style="list-style-type: none"> <li>Updated the maximum values for <math>t_{p_{LH}}</math> and <math>t_{p_{HL}}</math> in Table 5A and Table 5B</li> <li>Updated the package outline drawings; however, no technical changes</li> <li>Completed other minor improvements throughout the document</li> </ul>
October 4, 2016	<ul style="list-style-type: none"> <li>Corrected Tape &amp; Reel Orderable Part Number.</li> <li>Deleted “ICS” prefix and “I” suffix from the part number.</li> <li>Updated datasheet header/footer.</li> </ul>

SHEET 1 OF 2

01	ADD "GREEN" PRG NOMENCLATURE	10/08/04	TU VU
02	ADDED 48 LEAD	10/13/06	PKP
03	ADDED PACKAGE CODE	12/12/12	RC

PR/PRG32				
SYMBOL	JEDEC VARIATION			NOTE
	BBA			
	MIN	NOM	MAX	
A	—	—	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	9.00 BSC			4
D1	7.00 BSC			5,2
E	9.00 BSC			4
E1	7.00 BSC			5,2
N	32			
e	.80 BSC			
b	.30	.37	.45	7
b1	.30	.35	.40	
ccc	—	—	.10	
ddd	—	—	.20	

PR/PRG48				
SYMBOL	JEDEC VARIATION			NOTE
	BBC			
	MIN	NOM	MAX	
A	—	—	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	9.00 BSC			4
D1	7.00 BSC			5,2
E	9.00 BSC			4
E1	7.00 BSC			5,2
N	48			
e	.50 BSC			
b	.17	.22	.27	7
b1	.17	.20	.23	
ccc	—	—	.08	
ddd	—	—	.08	

NOTES:

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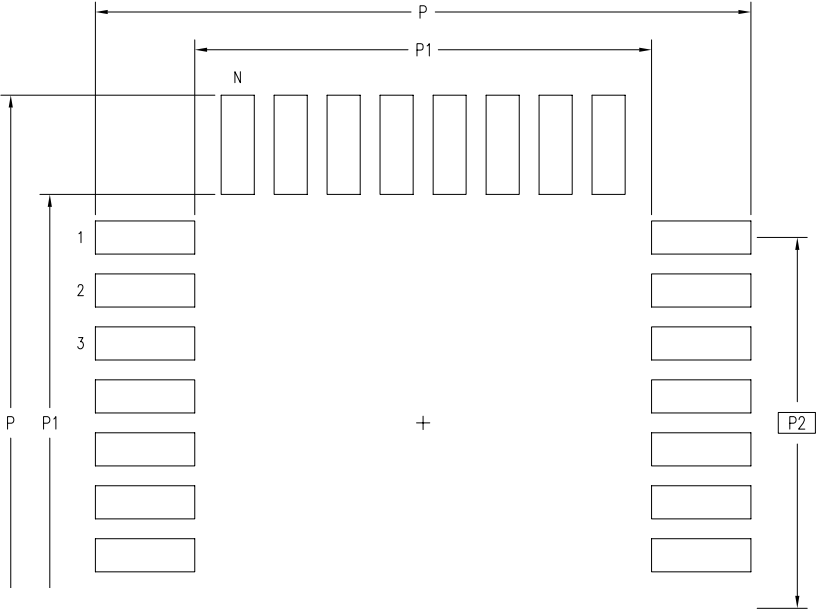
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LAND PATTERN DIMENSIONS



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