Low Skew, 1-to-22 Differential-to-HSTL Fanout Buffer

8524

DATA SHEET

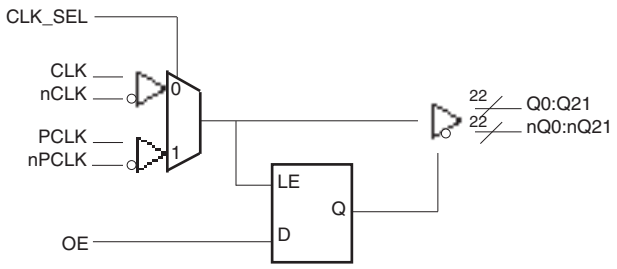
General Description

The 8524 is a low skew, 1-to-22 Differential-to-HSTL Fanout Buffer . The 8524 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The device is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the OE pin. The 8524's low output and part-to-part skew characteristics make it ideal for workstation, server, and other high performance clock distribution applications.

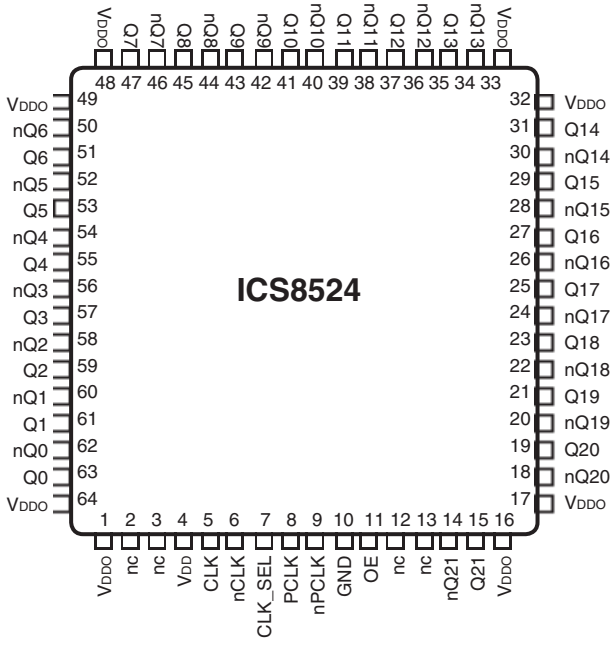
Features

- Twenty-two differential HSTL outputs each with the ability to drive 50Ω to ground
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, HSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 500MHz
- Translates any single-ended input signal (LVCMOS, LVTTL, GTL) to HSTL levels with resistor bias on nCLK input
- Output skew: 80ps (maximum)
- Part-to-part skew: 700ps (maximum)
- Jitter, RMS: 0.04ps (typical)
- LVPECL and HSTL mode operating voltage supply range: V_{DD} = 3.3V ± 5%, V_{DDO} = 1.6V to 2V, GND = 0V
- 0°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



64-Lead TQFP E-Pad
10mm x 10mm x 1.0mm package body
Y package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 16, 17, 32, 33, 48, 49, 64	V_{DDO}	Power		Output supply pins.
2, 3, 12, 13	nc	Unused		No connect.
4	V_{DD}	Power		Core supply pin.
5	CLK	Input	Pulldown	Non-inverting differential clock input pair.
6	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input pair. Biased to $^2/_3$ V_{CC}.
7	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVCMOS / LVTTL interface levels.
8	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input pair.
9	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input pair. Biased to $^2/_3$ V_{CC}.
10	GND	Power		Power supply ground.
11	OE	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q0:Q21, nQ0:nQ21. LVCMOS / LVTTL interface levels.
14, 15	nQ21, Q21	Output		Differential clock outputs. HSTL interface levels.
18, 19	nQ20, Q20	Output		Differential clock outputs. HSTL interface levels.
20, 21	nQ19, Q19	Output		Differential clock outputs. HSTL interface levels.
22, 23	nQ18, Q18	Output		Differential clock outputs. HSTL interface levels.
24, 25	nQ17, Q17	Output		Differential clock outputs. HSTL interface levels.
26, 27	nQ16, Q16	Output		Differential clock outputs. HSTL interface levels.
28, 29	nQ15, Q15	Output		Differential clock outputs. HSTL interface levels.
30, 31	nQ14, Q14	Output		Differential clock outputs. HSTL interface levels.
34, 35	nQ13, Q13	Output		Differential clock outputs. HSTL interface levels.
36, 37	nQ12, Q12	Output		Differential clock outputs. HSTL interface levels.
38, 39	nQ11, Q11	Output		Differential clock outputs. HSTL interface levels.
40, 41	nQ10, Q10	Output		Differential clock outputs. HSTL interface levels.
42, 43	nQ9, Q9	Output		Differential clock outputs. HSTL interface levels.
44, 45	nQ8, Q8	Output		Differential clock outputs. HSTL interface levels.
46, 47	nQ7, Q7	Output		Differential clock outputs. HSTL interface levels.
50, 51	nQ6, Q6	Output		Differential clock outputs. HSTL interface levels.
52, 53	nQ5, Q5	Output		Differential clock outputs. HSTL interface levels.
54, 55	nQ4, Q4	Output		Differential clock outputs. HSTL interface levels.
56, 57	nQ3, Q3	Output		Differential clock outputs. HSTL interface levels.
58, 59	nQ2, Q2	Output		Differential clock outputs. HSTL interface levels.
60, 61	nQ1, Q1	Output		Differential clock outputs. HSTL interface levels.
62, 63	nQ0, Q0	Output		Differential clock outputs. HSTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			37		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			75		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs		Outputs	
OE	CLK_SEL	Q0:Q21	nQ0:nQ21
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	CLK	nCLK
1	1	PCLK	nPCLK

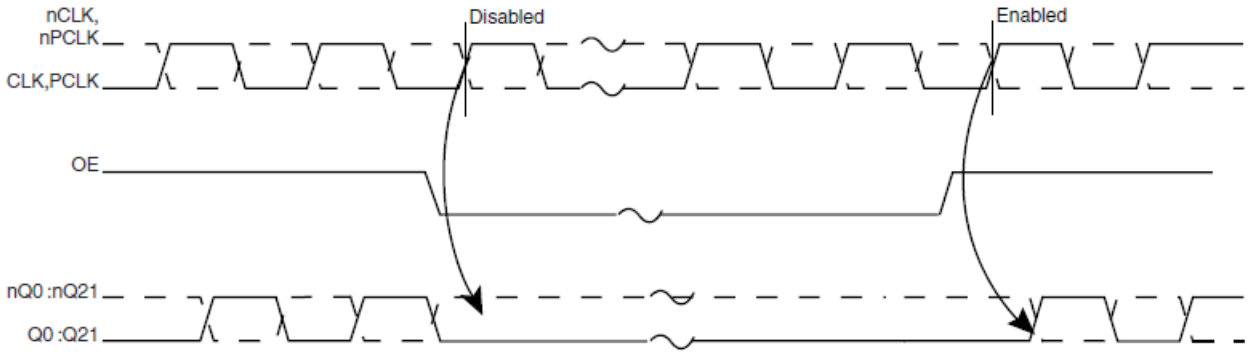


FIGURE 1. OE TIMING DIAGRAM

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	22.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA=0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				220	mA
I_{DDO}	Output Supply Current	No Load		1		mA

Table 4B. LVCMOS / LVTTL DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA=0°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE, CLK_SEL				5	µA
I_{IL}	Input Low Current	OE, CLK_SEL		-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA=0°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK, nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK and nCLK is V_{DD} + 0.3V.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA=0°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK, nPCLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK, nPCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.5		V_{DD}	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.

TABLE 4E. HSTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA=0°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1.0		1.4	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage; NOTE 2		40		60	%
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: Outputs terminated with 50Ω to ground.
NOTE 2: Defined with respect to output voltage swing at a given condition.

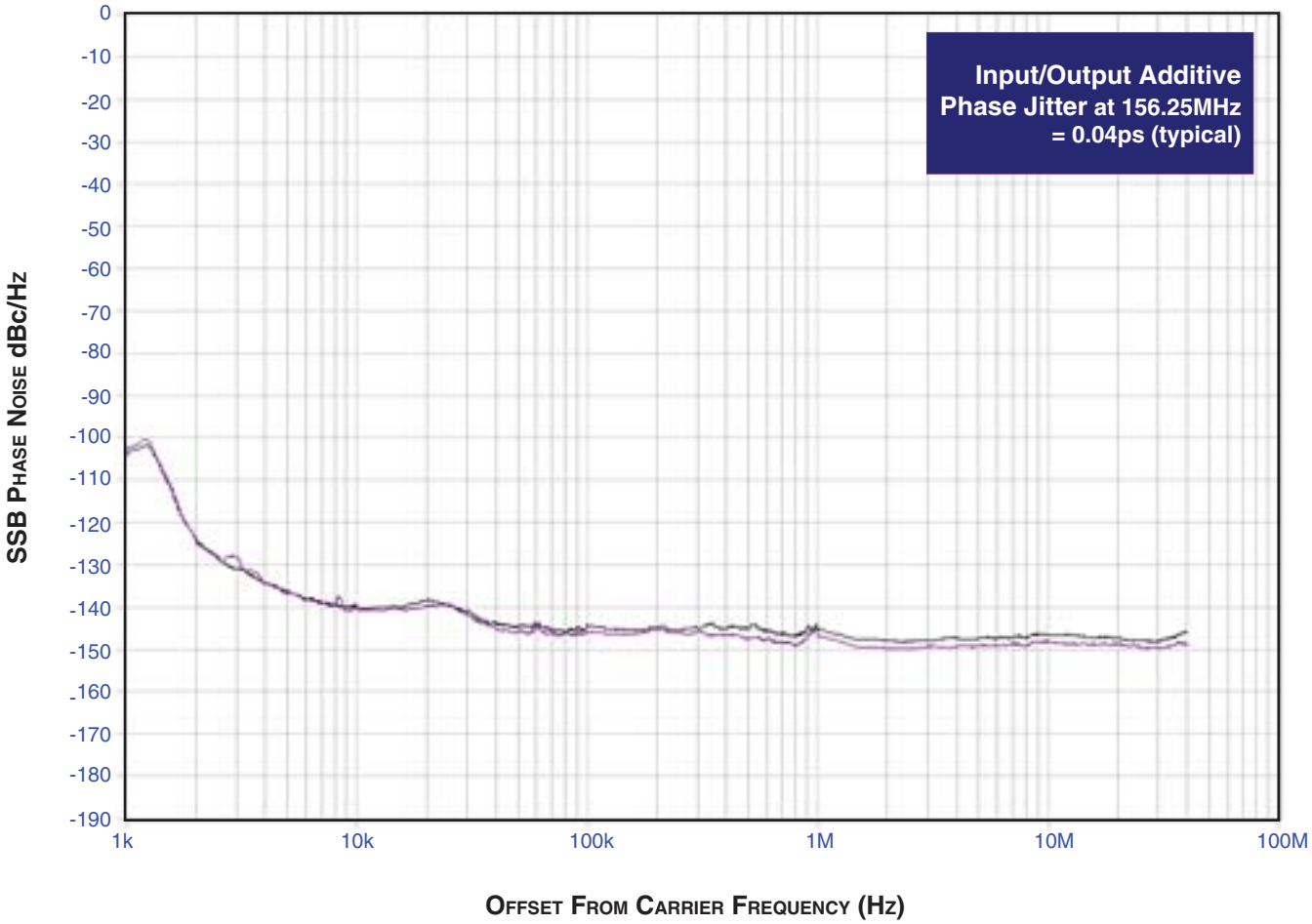
TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA=0°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				500	MHz
t_{PD}	Propagation Delay; NOTE 1		1.7		2.7	ns
tsk(o)	Output Skew; NOTE 2, 4				80	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				700	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section			0.04		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
t_S	Setup Time		1.0			ns
t_H	Hold Time		0.5			ns
odc	Output Duty Cycle	$f \leq$ 133MHz	49		51	%
		133 < $f \leq$ 266MHz	48		52	%

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions at the same temperature. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

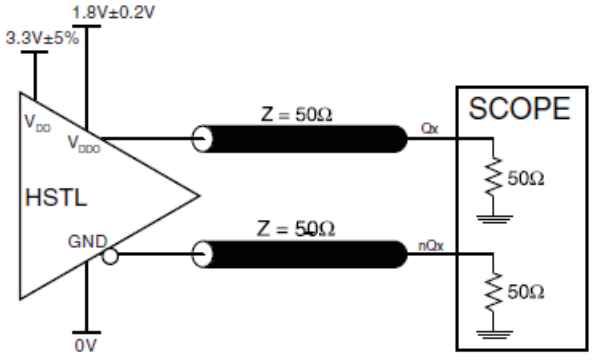
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

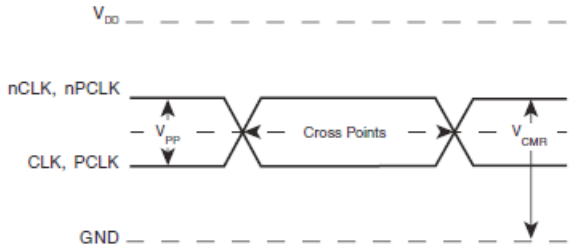


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

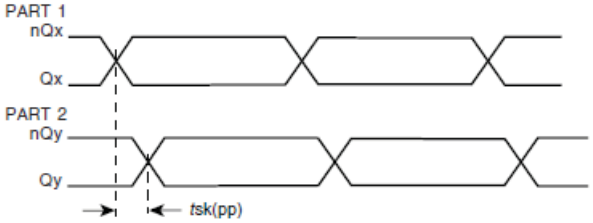
PARAMETER MEASUREMENT INFORMATION



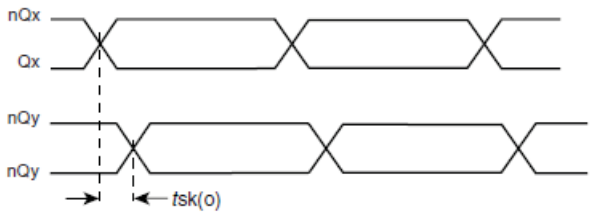
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



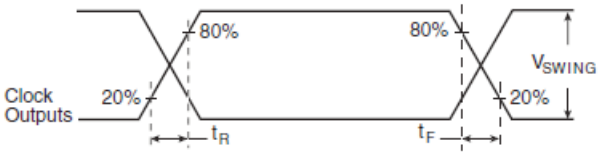
DIFFERENTIAL INPUT LEVEL



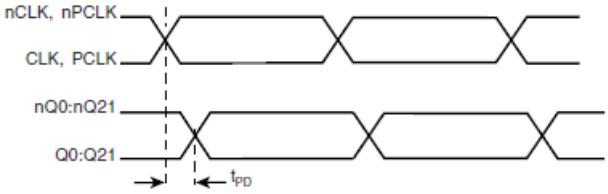
PART-TO-PART SKEW



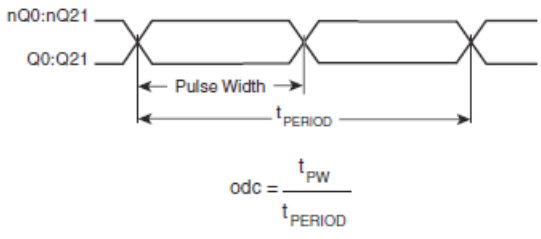
OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

OUTPUT CROSSOVER VOLTAGE

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

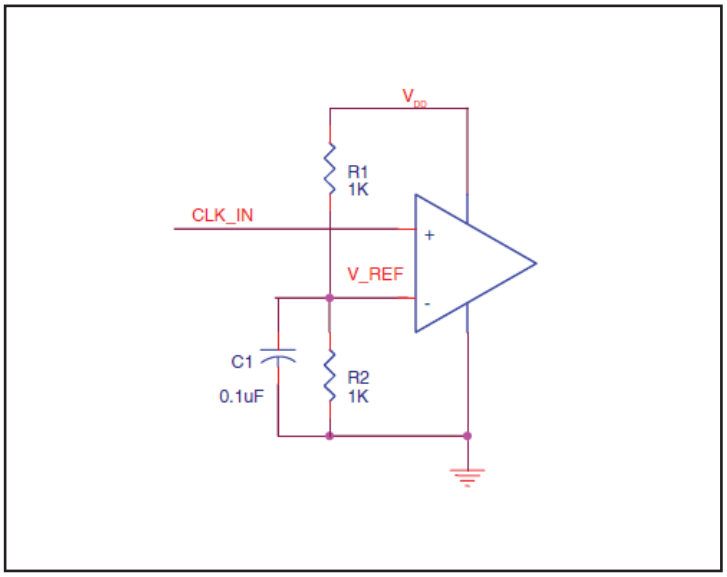


Figure 2. Single Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for HSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

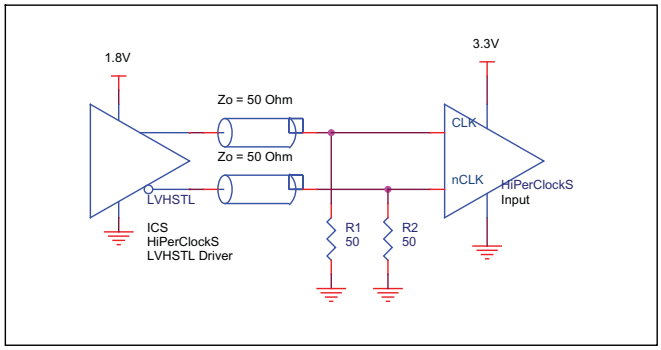


Figure 3A. CLK/nCLK Input Driven by HSTL Driver

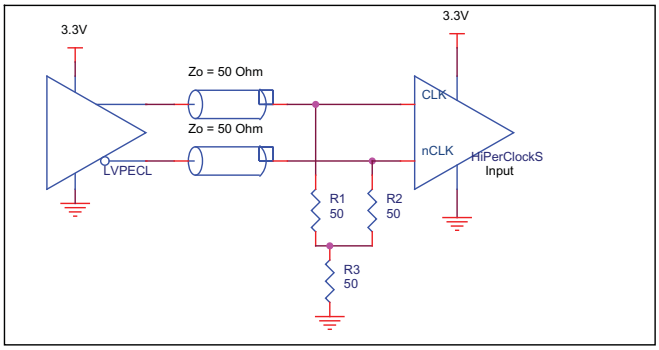


Figure 3B. CLK/nCLK Input Driven by 3.3V LVPECL Driver

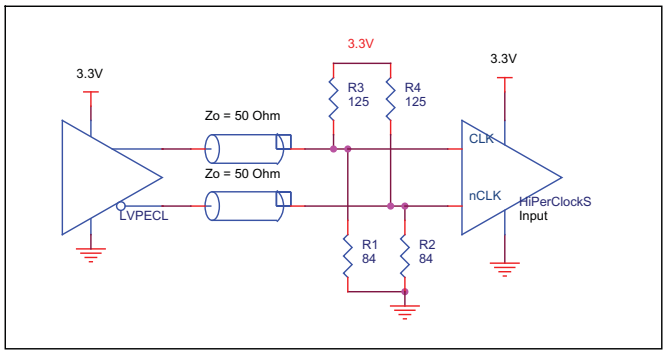


Figure 3C. CLK/nCLK Input Driven by 3.3V LVPECL Driver

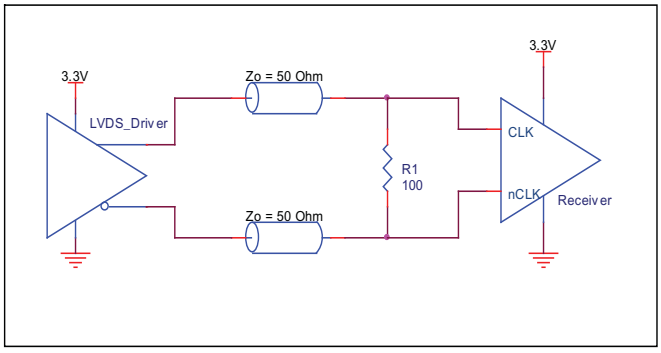


Figure 3D. CLK/nCLK Input Driven by 3.3V LVDS Driver

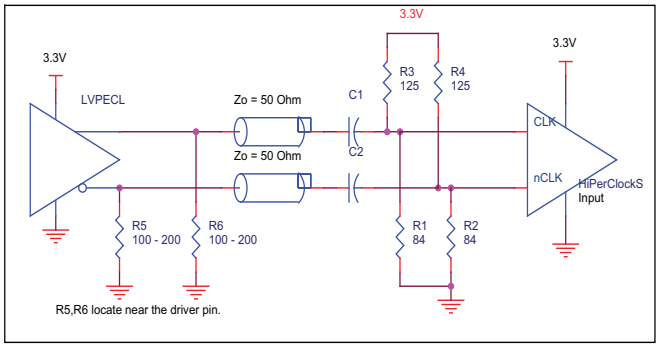


Figure 3E. CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

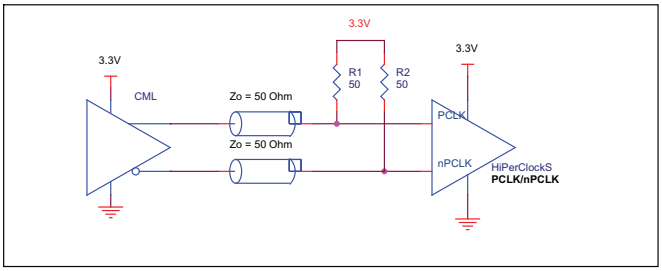


Figure 4A. PCLK/nPCLK Input Driven by a CML Driver

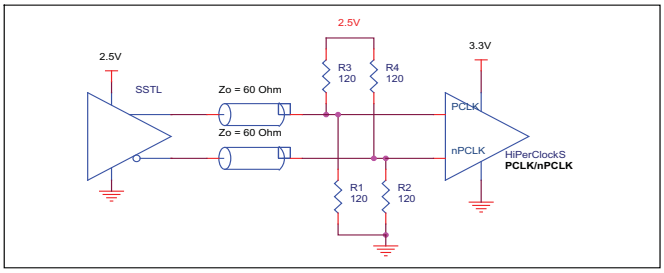


Figure 4B. PCLK/nPCLK Input Driven by an SSTL Driver

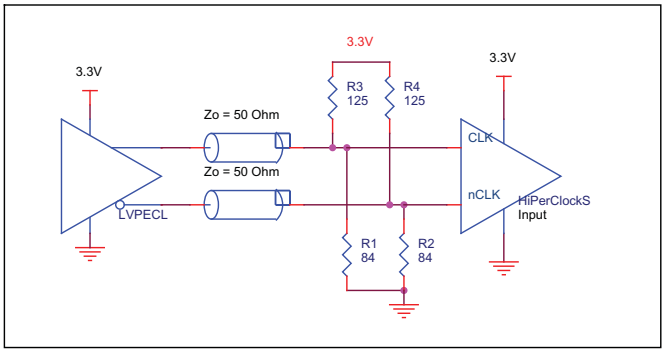


Figure 4C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

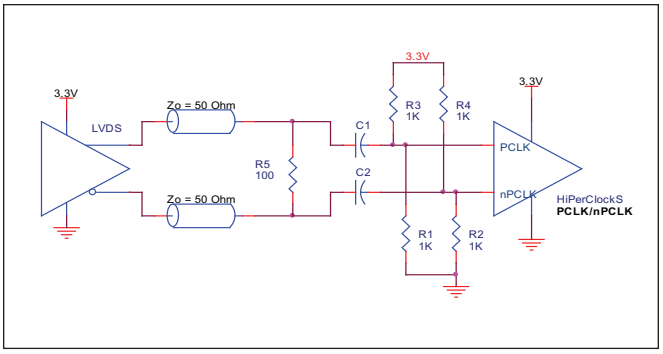


Figure 4D. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

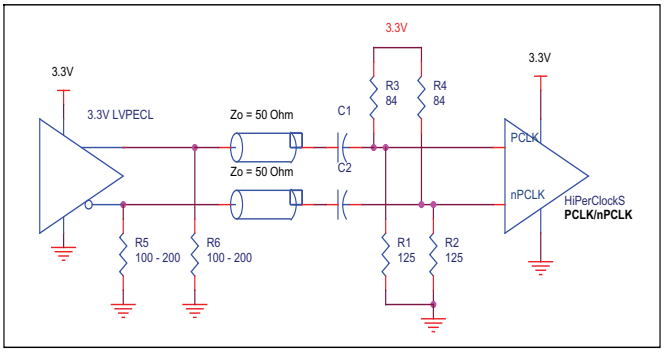


Figure 4E. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

Schematic Example

Figure 5 shows a schematic example of the 8524. In this example, the input is driven by a HSTL driver. The decoupling capacitors should be physically located near the power pin. For 8524, the unused clock outputs can be left floating.

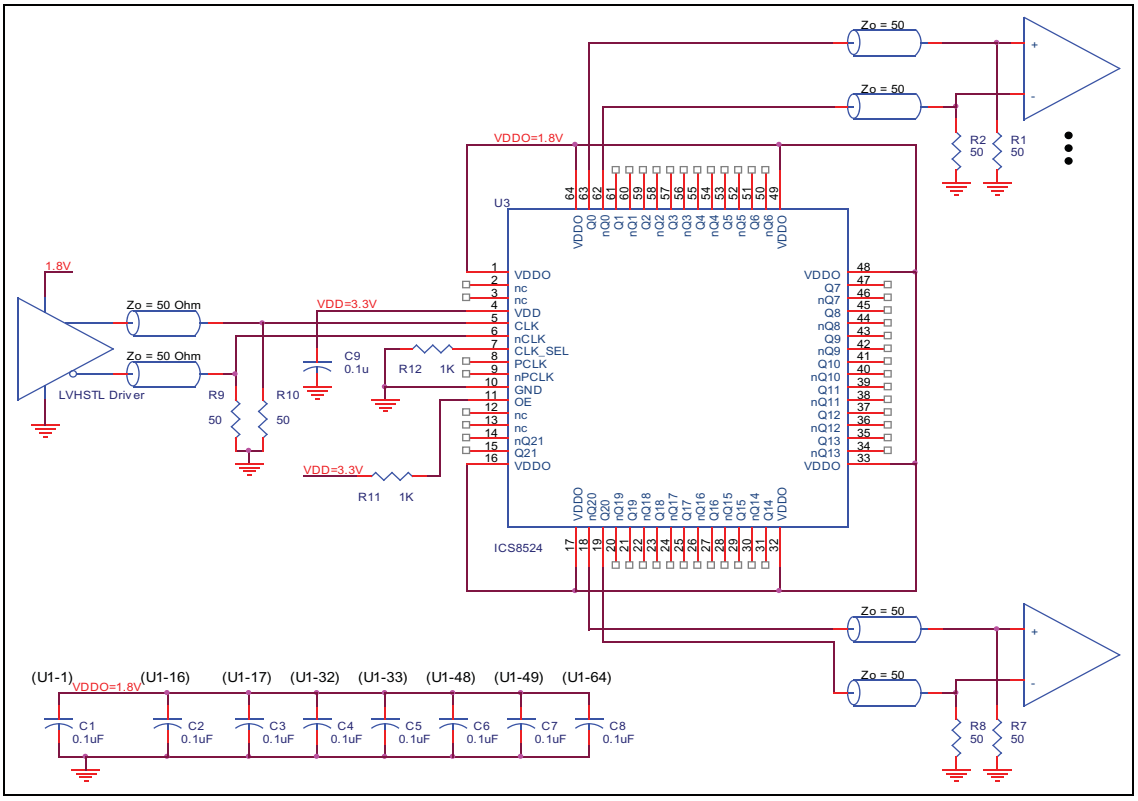


Figure 5. 8524 HSTL Buffer Schematic Example

Thermal Release Path

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder as shown in *Figure 6.* For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

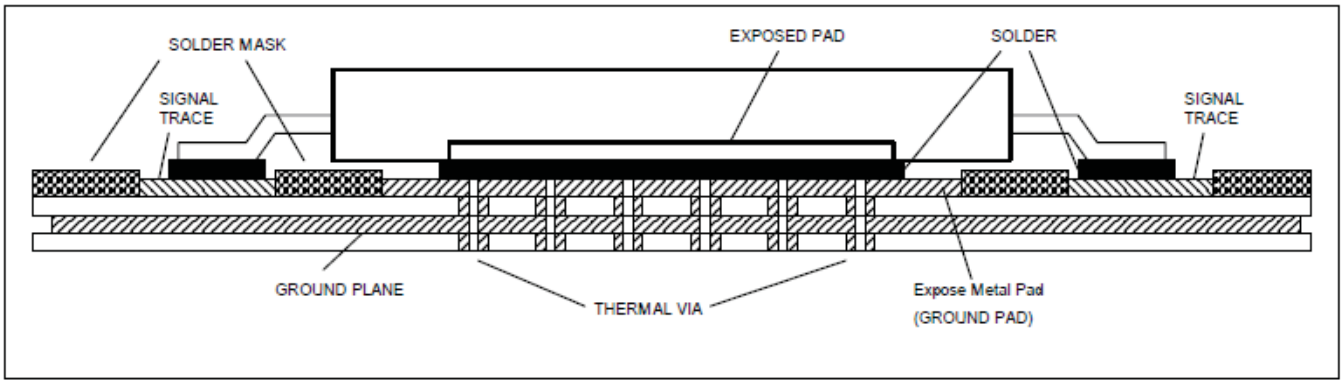


Figure 6. P.C. Board for Exposed Pad Thermal Release Path Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8524.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 8524 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 220mA = **762.3mW**
- Power $(outputs)_{MAX}$ = **32.8mW/Loaded Output pair**
  If all outputs are loaded, the total power is 22 * 32.8mW = **721.6mW**

Total Power $_{MAX}$ (3.465V, with all outputs switching) = 762.3mW + 721.6mW = **1483.9mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming an air flow of 500 linear feet per minute and a multi-layer board, the appropriate value is 15.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 1.484W * 15.1°C/W = 107.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 64-PIN TQFP, E-PAD FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	22.3°C/W	17.2°C/W	15.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 7.*

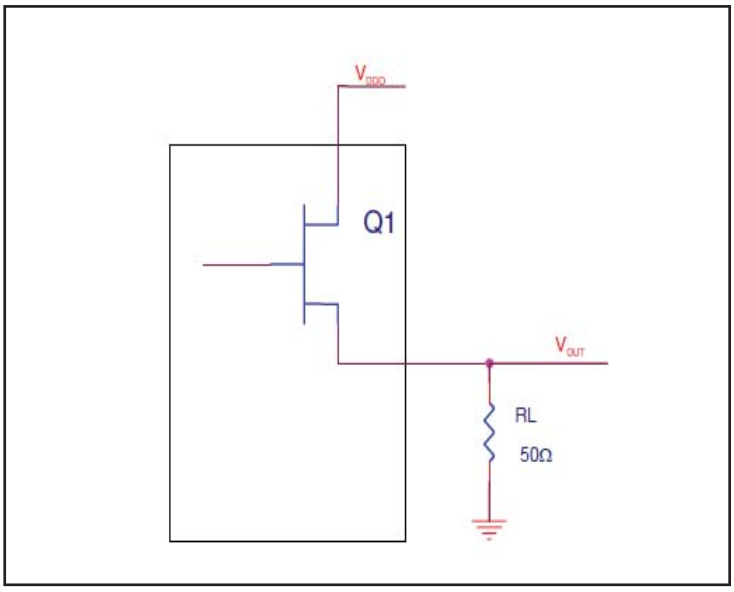


FIGURE 7. HSTL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MIN}/R_L) * (V_{DDO\_MAX} - V_{OH\_MIN})$

$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$

Pd_H = (1V/50Ω) * (2V - 1V) = **20mW**
Pd_L = (0.4V/50Ω) * (2V - 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.8mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 64 Lead TQFP, E-Pad

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	22.3°C/W	17.2°C/W	15.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 8524 is: 1474

Package Outline - Y Suffix for 64 Lead TQFP, E-Pad

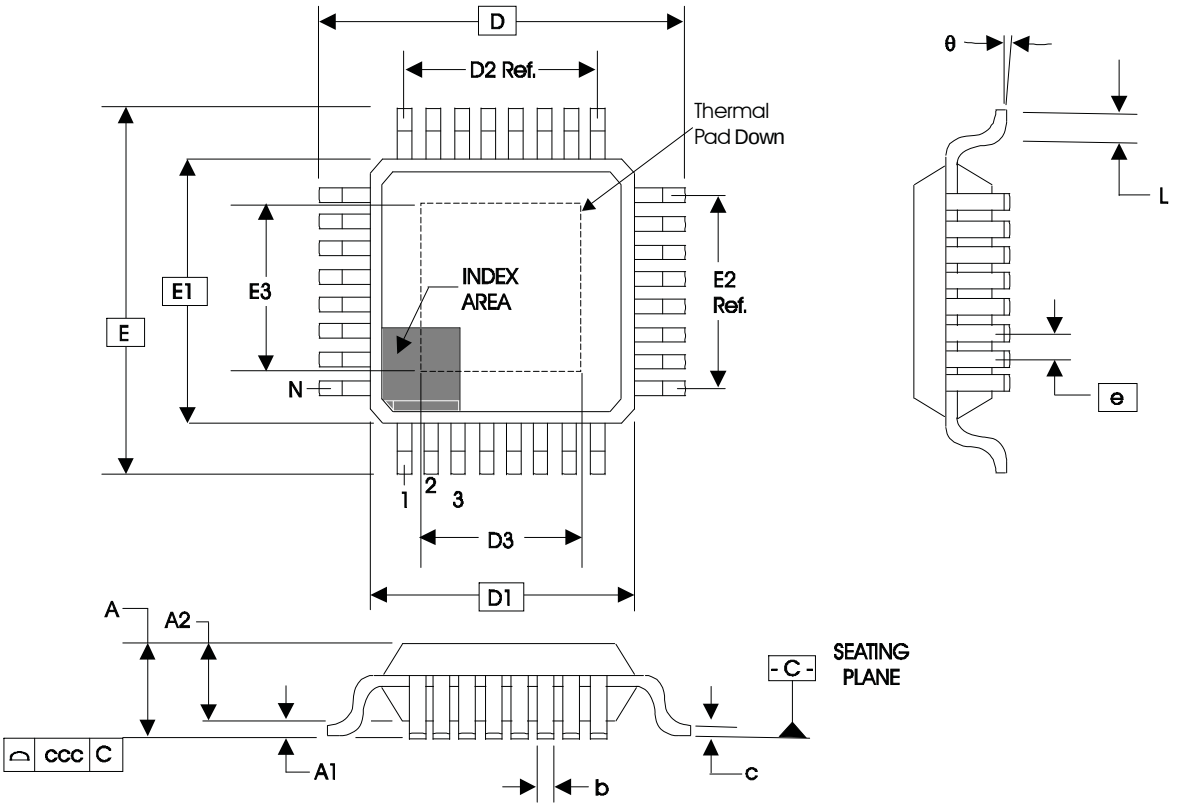


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	ACD-HD		
	MINIMUM	NOMINAL	MAXIMUM
N		64	
A	--	--	1.20
A1	0.05	0.10	0.15
A2	0.95	1.0	1.05
b	0.17	0.22	0.27
c	0.09	--	0.20
D		12.00 BASIC	
D1		10.00 BASIC	
D2		7.50 Ref.	
E		12.00 BASIC	
E1		10.00 BASIC	
E2		7.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08
D3 & E3	2.0	--	10.0

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8524AYLF	ICS8524AYLF	64 lead TQFP, E-Pad	tray	0°C to 85°C
8524AYLFT	ICS8524AYLF	64 lead TQFP, E-Pad	Tape and Reel	0°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS com

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T5	1 5 6	Added Phase Jitter to Features section. AC Characteristics Table - added Phase Jitter row. Added Additive Phase Jitter section.	9/18/03
B		15	Updated Package Outline and Package Dimensions Table.	11/19/04
B	T9	16	Ordering Information Table - Added LF Marking and note	8/1/07
B	T9	10 12	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	12/6/10
B	T9	16	Ordering Information - removed leaded devices. Updated data sheet format.	11/9/15

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