

## GENERAL DESCRIPTION

The 843023I is a Gigabit Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from IDT. The 843023I uses a 25MHz crystal to synthesize 250MHz. The 843023I has excellent phase jitter performance, over the 1.875MHz – 20MHz integration range. The 843023I is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

## FEATURES

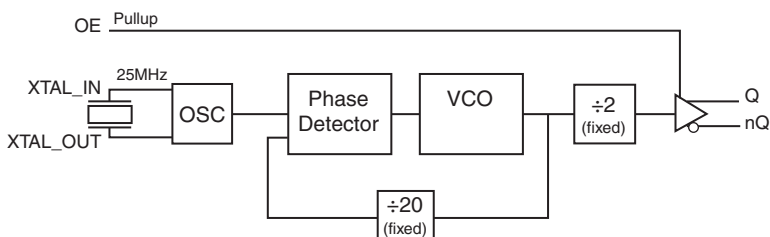
- One differential 3.3V or 2.5V LVPECL output
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- Output frequency range: 240MHz - 320MHz
- VCO range: 480MHz - 640MHz
- RMS phase jitter @ 250MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.39ps (typical)

Phase noise:

Offset	Noise Power
100Hz .....	-86.3 dBc/Hz
1kHz .....	-114.6 dBc/Hz
10kHz .....	-125.6 dBc/Hz
100kHz .....	-126.0 dBc/Hz

- Full 3.3V and 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## BLOCK DIAGRAM



## PIN ASSIGNMENT

Vcc	1	8	Q
XTAL_OUT	2	7	nQ
XTAL_IN	3	6	Vcc
VEE	4	5	OE

**843023I**

**8-Lead TSSOP**

4.40mm x 3.0mm x 0.925mm package body

**G Package**

Top View

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 6	V <sub>CC</sub>	Power		Core supply pin.
2, 3	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	V <sub>EE</sub>	Power		Negative supply pin.
5	OE	Input	Pullup	Active high output enable. When logic HIGH, the outputs are enabled and active. When logic LOW, the outputs are disabled and the device is in power down mode. LVCMOS/LVTTL interface levels.
7, 8	nQ, Q	Output		Differential clock outputs. LVPECL interface levels.

*Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	101.7°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				75	mA

**TABLE 3B. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{CCA}$	Analog Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				70	mA

**TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{CC} = 3.3V$	2		$V_{CC} + 0.3$	V
		$V_{CC} = 2.5V$	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{CC} = 3.3V$	-0.3		0.8	V
		$V_{CC} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	OE $V_{CC} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	OE $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu\text{A}$

**TABLE 3D. LVPECL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**TABLE 4. CRYSTAL CHARACTERISTICS**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		24		32	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

**TABLE 5A. AC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

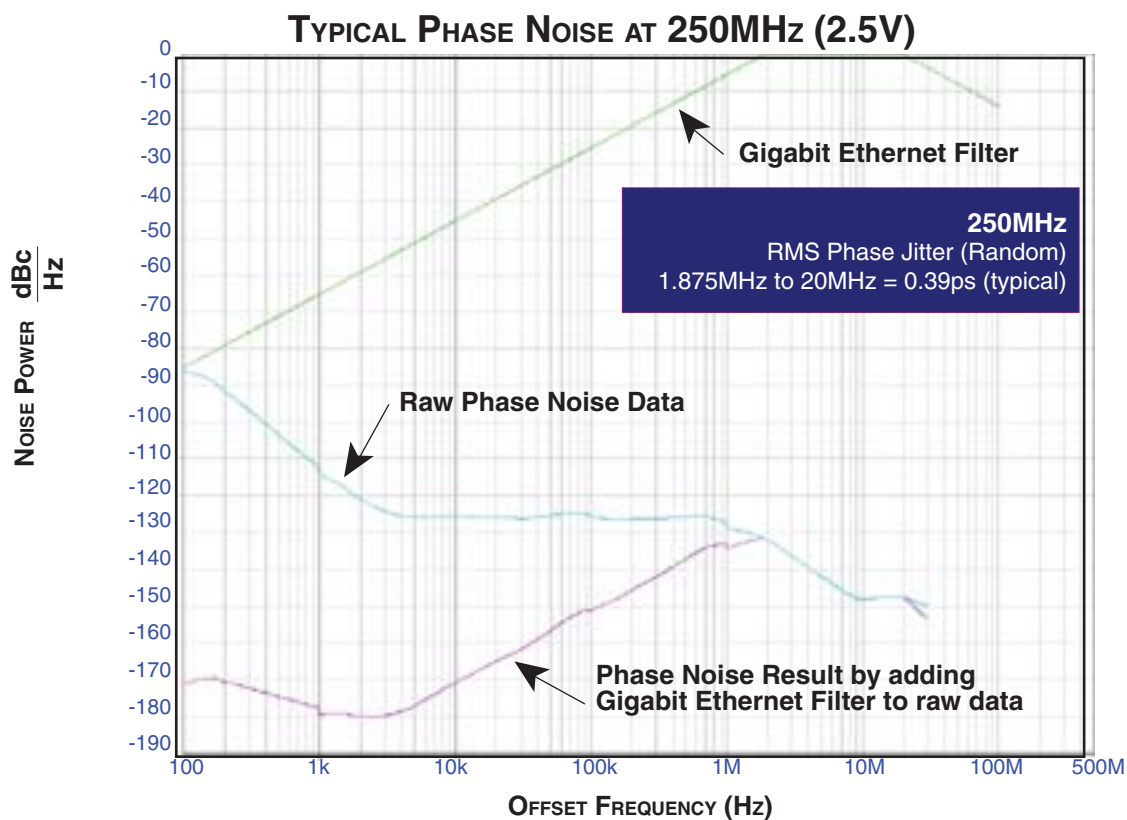
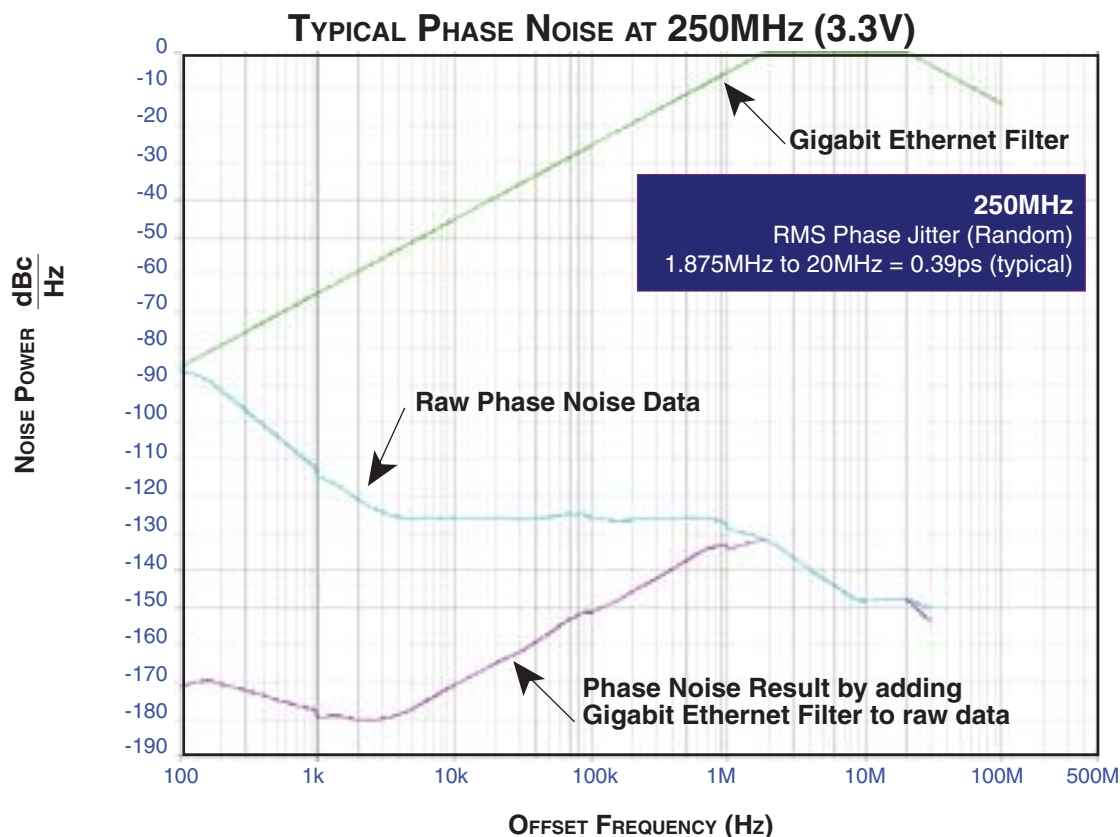
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		240		320	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	250MHz, Integration Range: 1.875MHz - 20MHz		0.39		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		600	ps
odc	Output Duty Cycle		47		53	%

NOTE 1: Please refer to the Phase Noise Plot after this section.

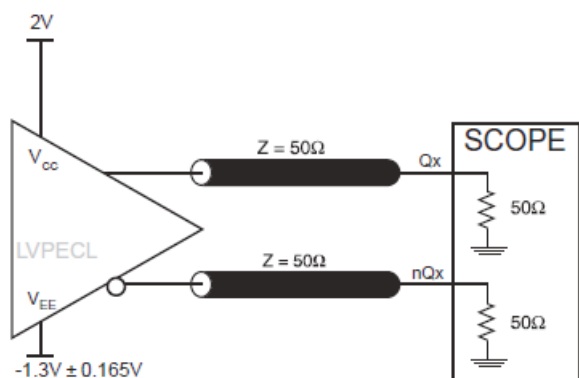
**TABLE 5B. AC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		240		320	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	250MHz, Integration Range: 1.875MHz - 20MHz		0.39		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		600	ps
odc	Output Duty Cycle		47		53	%

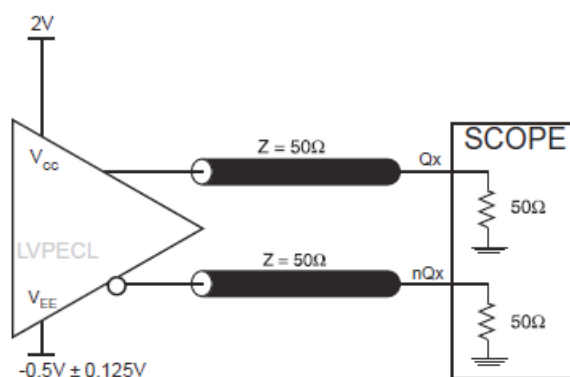
NOTE 1: Please refer to the Phase Noise Plot after this section.



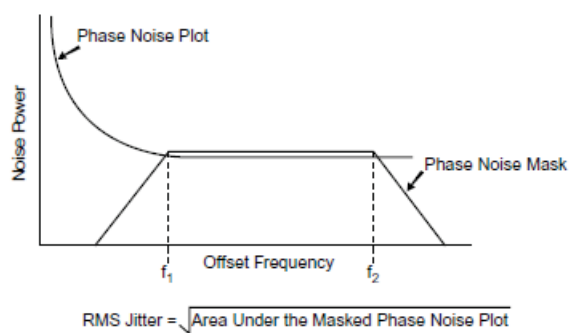
## PARAMETER MEASUREMENT INFORMATION



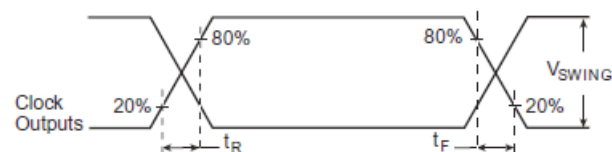
3.3V OUTPUT LOAD AC TEST CIRCUIT



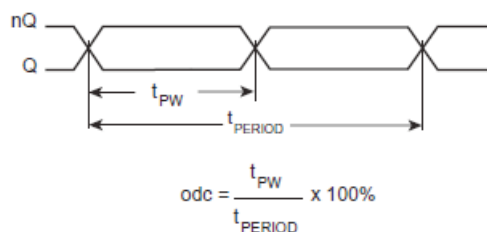
2.5V OUTPUT LOAD AC TEST CIRCUIT



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## APPLICATION INFORMATION

### CRYSTAL INPUT INTERFACE

The 843023I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel resonant crystal and

were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

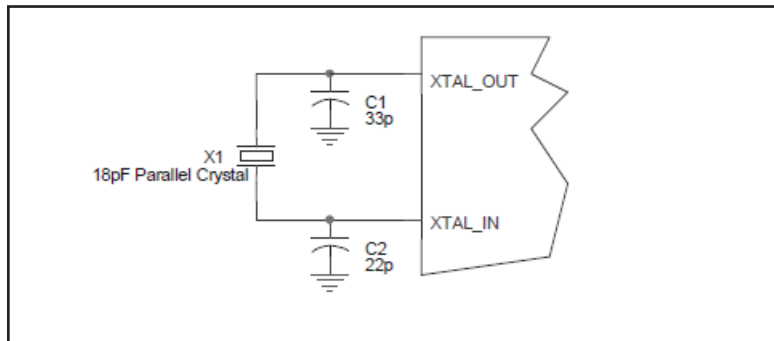


FIGURE 1. CRYSTAL INPUT INTERFACE

### LVC MOS TO XTAL INTERFACE

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 2*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission

line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω.

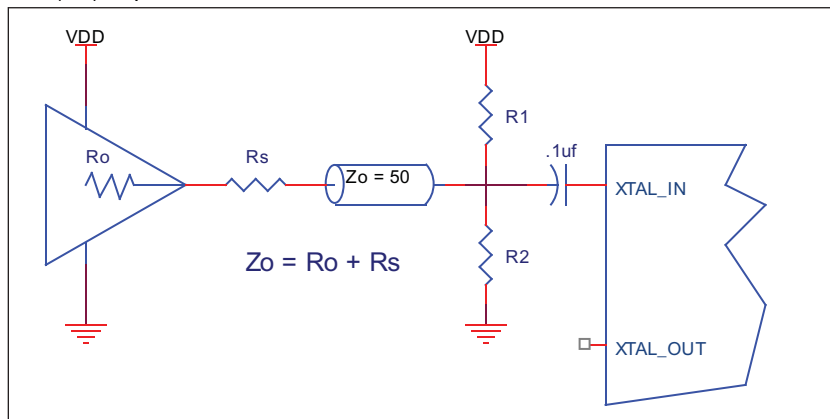


FIGURE 2. General Diagram for LVC MOS Driver to XTAL Input Interface

## TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

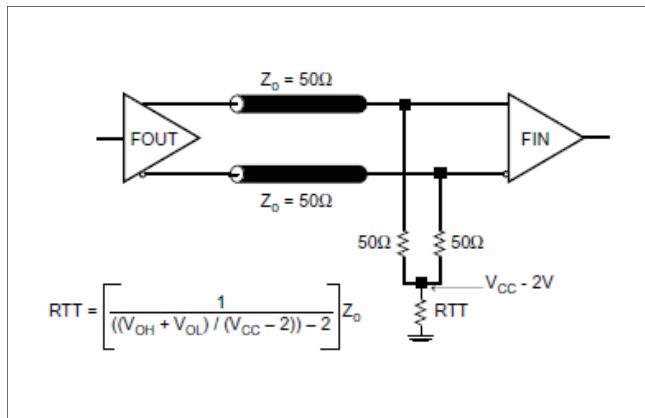


FIGURE 3A. LVPECL OUTPUT TERMINATION

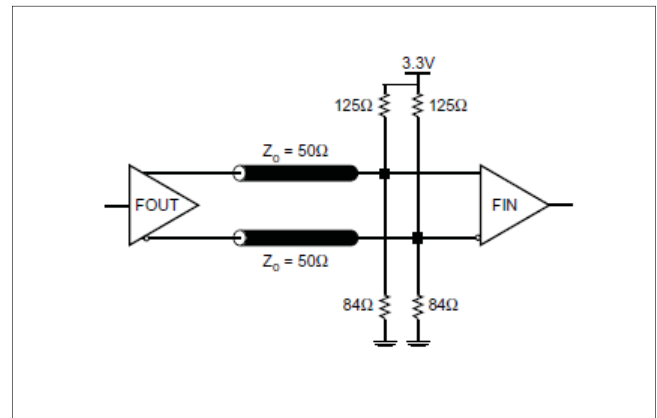


FIGURE 3B. LVPECL OUTPUT TERMINATION

## TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{cc} - 2V$ . For  $V_{cc} = 2.5V$ , the  $V_{cc} - 2V$  is very close to ground

level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.

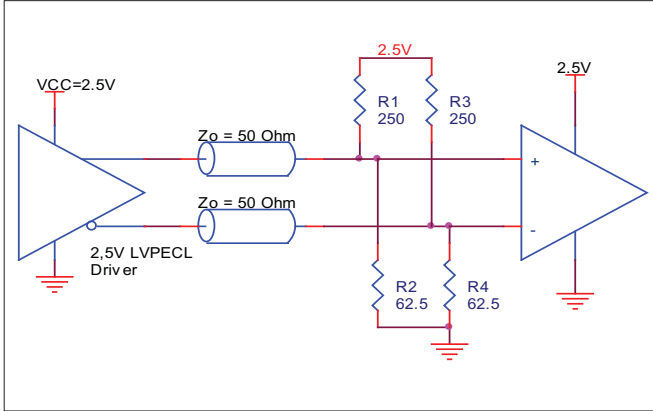


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

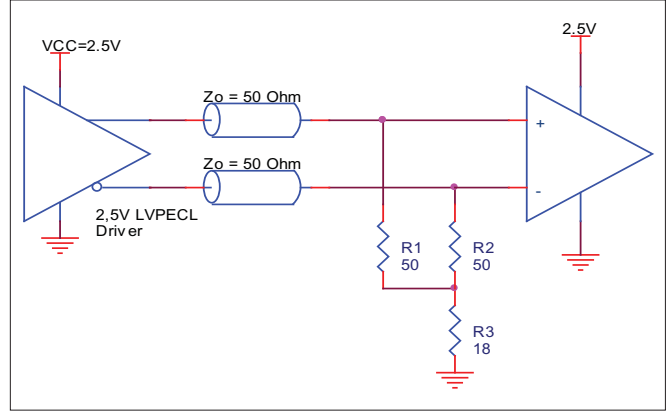


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

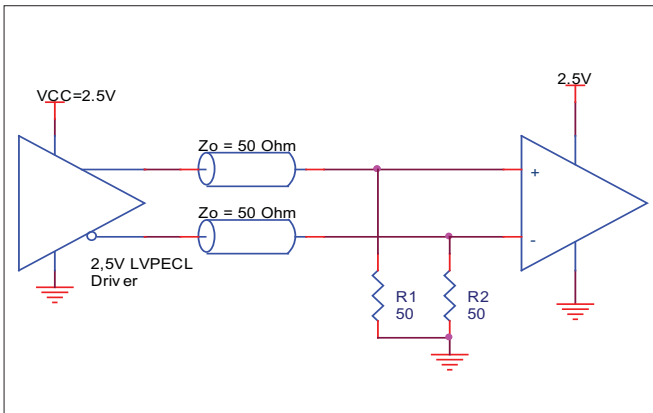


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

# POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843023L. Equations and example calculations are also provided.

## 1. Power Dissipation.

The total power dissipation for the 843023L is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 75mA = 259.87mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) = 259.87mW + 30mW = **389.87mW**

## 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.290W * 90.5^\circ C/W = 111.2^\circ C$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN TSSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5*.

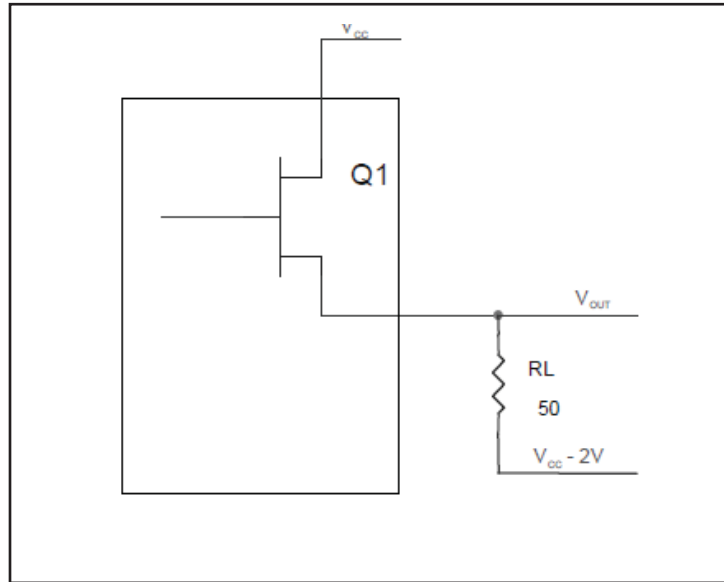


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.9V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30mW$$

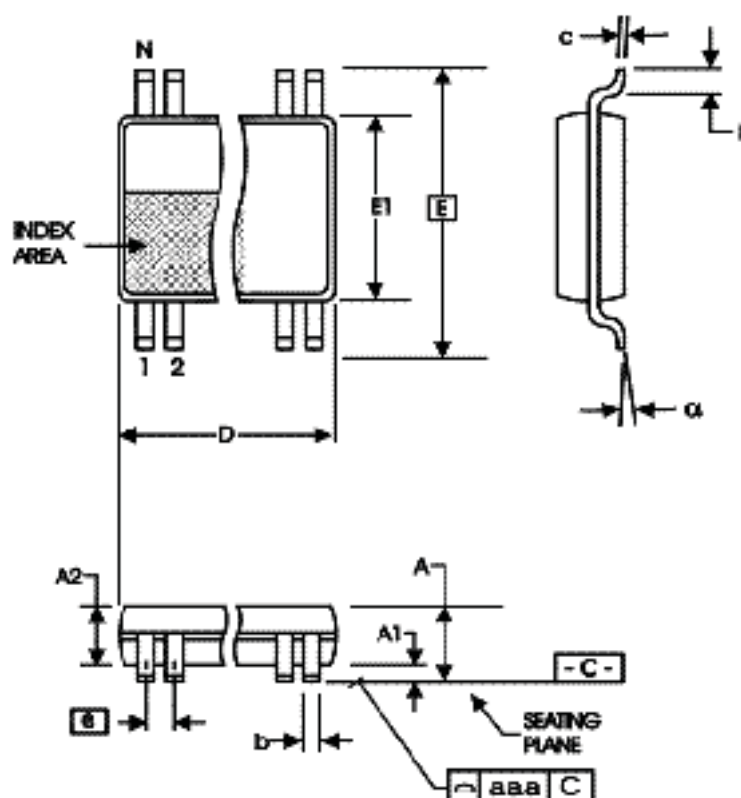
RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for 843023I is: 2360

**PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP**

**TABLE 8. PACKAGE DIMENSIONS**

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

**TABLE 9. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843023AGILF	23AIL	8 lead "Lead Free" TSSOP	Tube	-40°C to +85°C
843023AGILFT	23AIL	8 lead "Lead Free" TSSOP	Tape and Reel	-40°C to +85°C
NOTE: Parts that are ordered with an "LF" suffix to the part number are Pb-Free and RoHS compliant.				

# REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
B	T4 T5A & T5B	1 4 4 7	Features Section - changed minimum output frequency range from 245MHz to 240MHz. Changed minimum VCO range from 490MHz to 480MHz. Crystal Characteristics Table - changed minimum frequency from 24.5MHz to 24MHz. AC Characteristics Tables - changed minimum output frequency from 245MHz to 240MHz. Added LVCMOS to XTAL Interface section.	1/9/07
B	T9	14	Ordering Information - removed leaded devices and added Marking for the Lead Free devices. Updated datasheet format.	1/9/15



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