

## General Description

The 843021 is a Gigabit Ethernet Clock Generator. The ICS843021 uses a 25MHz crystal to synthesize 125MHz. The 843021 has excellent phase jitter performance, over the 1.875MHz – 20MHz integration range. The 843021 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

## Features

- One differential 3.3V LVPECL output
- Crystal oscillator interface designed for 22.4MHz – 28MHz, 18pF parallel resonant crystal
- Output frequency range: 112MHz – 140MHz
- VCO range: 560MHz – 700MHz
- Output duty cycle range: 49% – 51%
- RMS phase jitter at 125MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.650ps (typical)

### Offset Noise Power

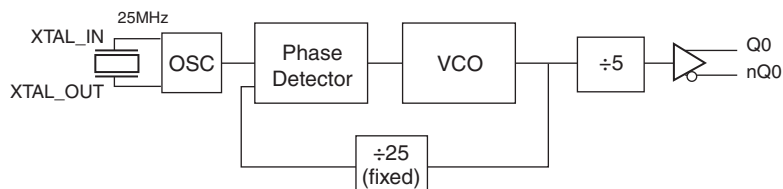
100Hz.....	-94.2 dBc/Hz
1kHz.....	-122.8 dBc/Hz
10kHz.....	-132.2 dBc/Hz
100kHz.....	-131.3 dBc/Hz

- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- Industrial temperature information available upon request

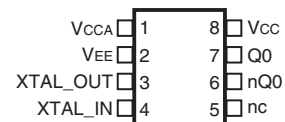
Table 1. Frequency Table - Typical Applications

Inputs	
Crystal Frequency (MHz)	Output Frequency Range (MHz)
25	125
26.6	133

## Block Diagram



## Pin Assignment



**843021**

**8 Lead TSSOP**

**4.40mm x 3.0mm x 0.925 package body**

**G Package**

**Top View**

**Table 2. Pin Descriptions**

Number	Name	Type	Description
1	V <sub>CCA</sub>	Unused	Analog supply pin.
2	V <sub>EE</sub>	Power	Negative supply pin.
3, 4	XTAL_OUT XTAL_IN	Input	Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	nc	Unused	No connect.
6, 7	nQ0, Q0	Output	Differential output pair. LVPECL interface levels.
8	V <sub>CC</sub>	Power	Core supply pin.

**Table 3. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V <sub>CC</sub>	4.6V
Inputs, V <sub>I</sub>	-0.5V to V <sub>CC</sub> + 0.5V
Outputs, I <sub>O</sub> Continuos Current Surge Current	50mA 100mA
Package Thermal Impedance, $\theta_{JA}$	101.7°C/W (0 mps)
Storage Temperature, T <sub>STG</sub>	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics, V<sub>CC</sub> = 3.3V ± 10%, V<sub>EE</sub> = 0V, T<sub>A</sub> = 0°C to 70°C**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>CC</sub>	Core Supply Voltage		2.97	3.3	3.63	V
V <sub>CCA</sub>	Analog Supply Voltage		2.97	3.3	3.63	V
I <sub>EE</sub>	Power Supply Current				85	mA

**Table 4B. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 10\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with  $50\Omega$  to  $V_{CC} - 2V$ .

**Table 5. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency; NOTE 1		14		40	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF

NOTE 1: Input frequency is limited to a range of 22.4MHz – 28MHz due to VCO range.

## AC Electrical Characteristics

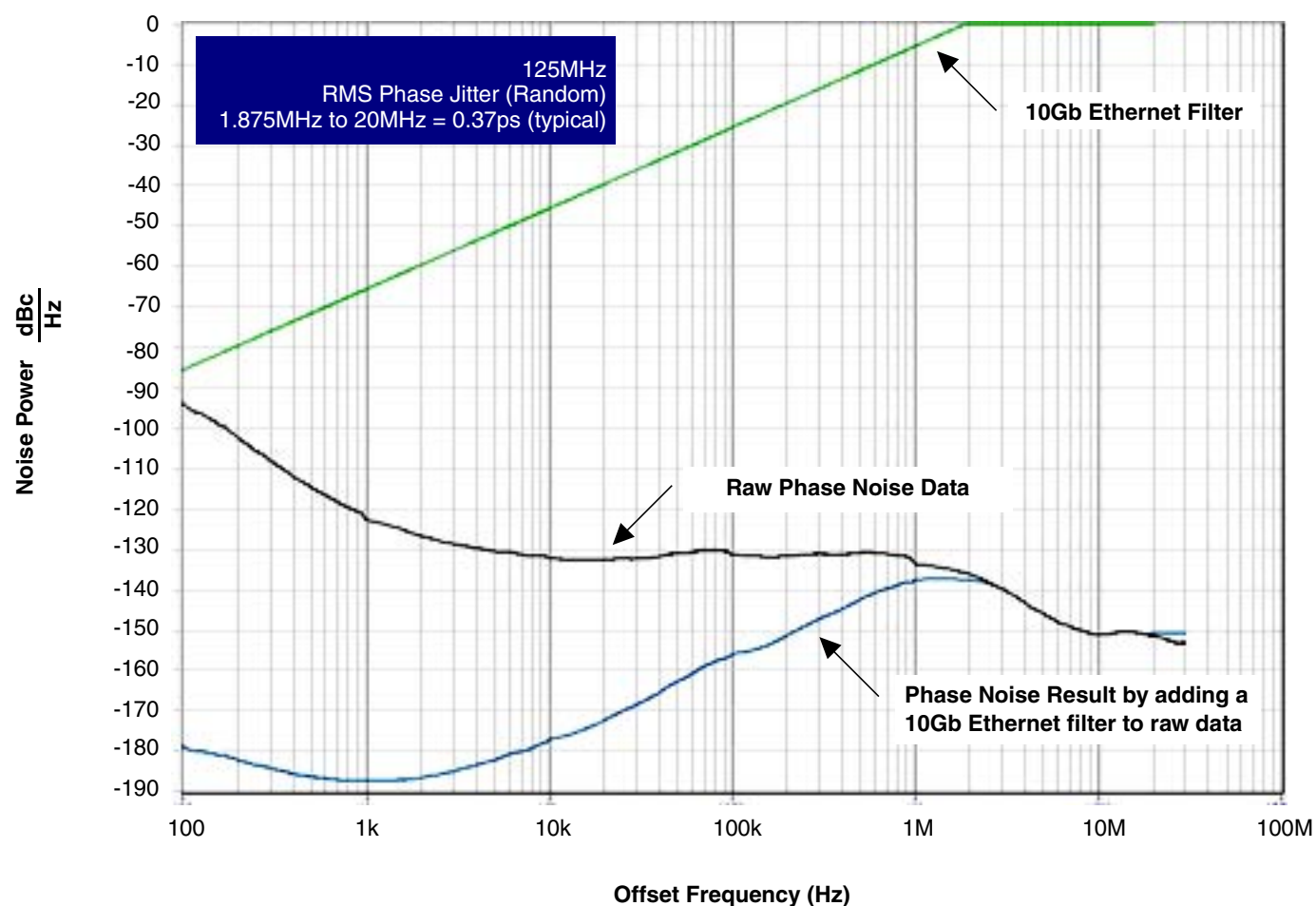
**Table 6. AC Characteristics,  $V_{CC} = 3.3V \pm 10\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		112		140	MHz
$\bar{f}_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 1	125MHz, Integration Range: 1.875MHz – 20MHz		0.37	0.65	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	250		550	ps
odc	Output Duty Cycle		49		51	%

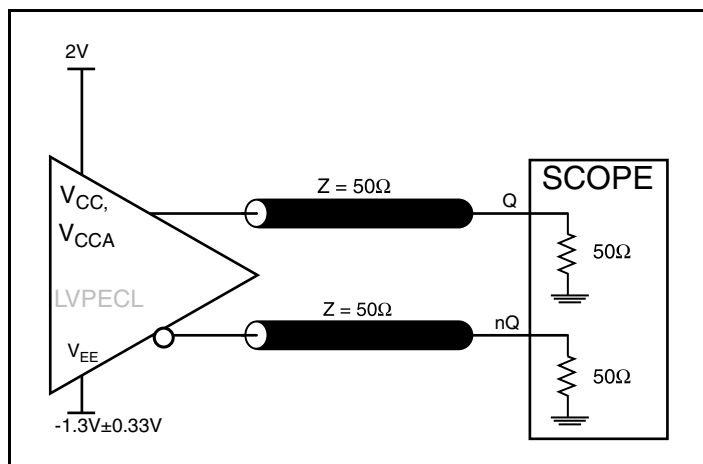
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Refer to Phase Noise Plot.

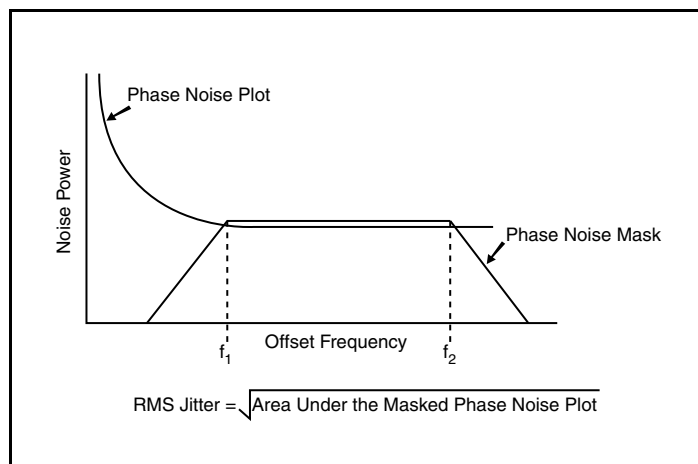
## Typical Phase Noise at 125MHz



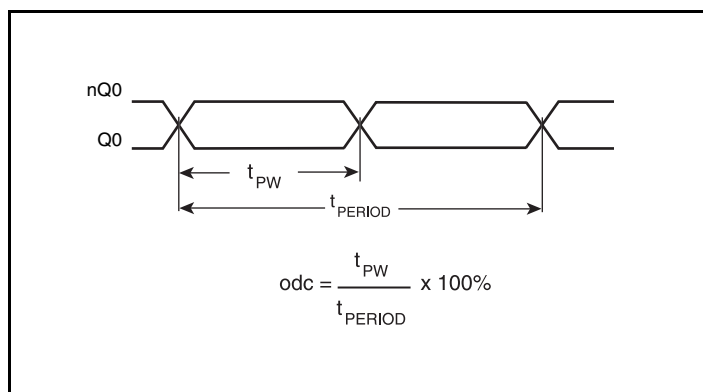
## Parameter Measurement Information



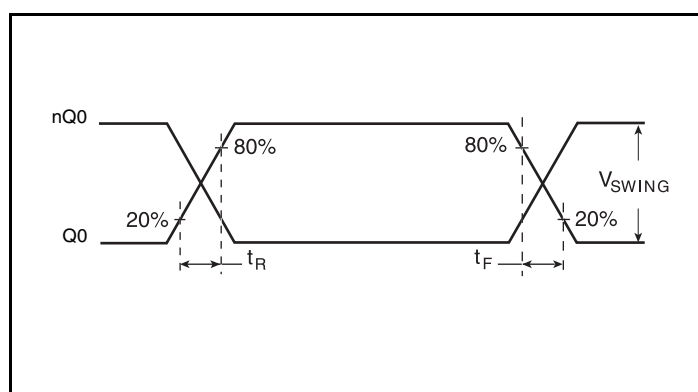
3.3V LVPECL Output Load AC Test Circuit



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

## Applications Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843021 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$  and  $V_{CCA}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{CC}$  pin and also shows that  $V_{CCA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{CCA}$  pin.

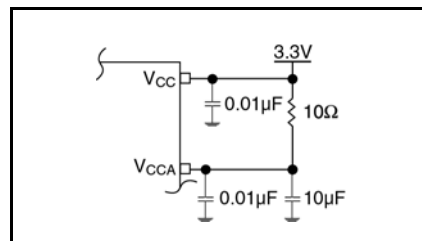


Figure 1. Power Supply Filtering

### Crystal Input Interface

The 843021 has been characterized with  $18\text{pF}$  parallel resonant crystals. The capacitor values,  $C1$  and  $C2$ , shown in *Figure 2* below were determined using a  $25\text{MHz}$ ,  $18\text{pF}$  parallel resonant crystal and

were chosen to minimize the ppm error. The optimum  $C1$  and  $C2$  values can be slightly adjusted for different board layouts.

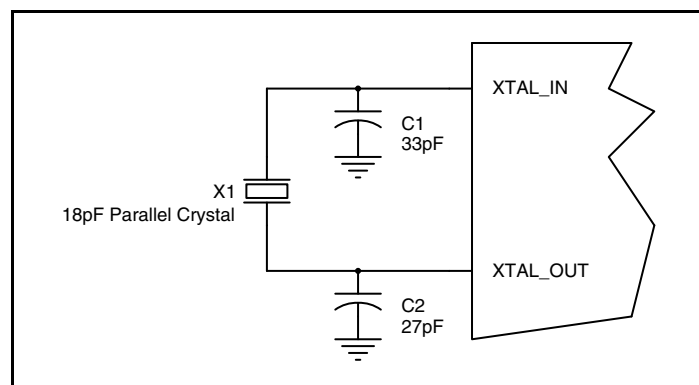
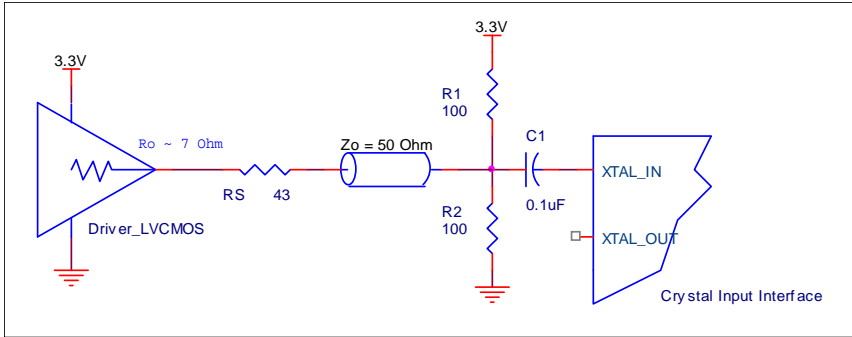


Figure 2. Crystal Input Interface

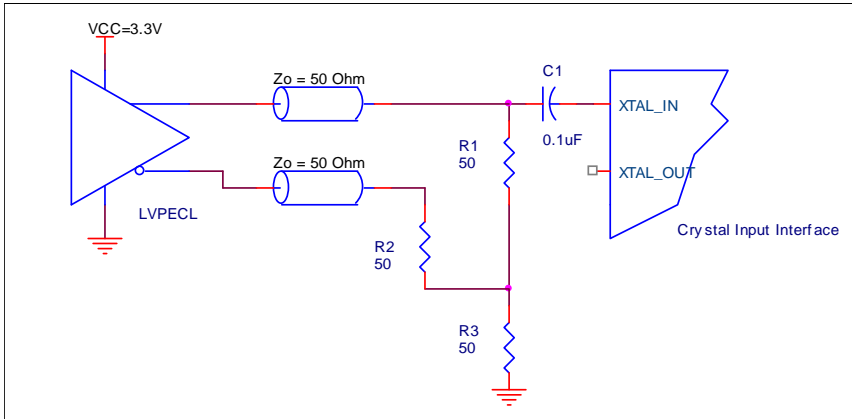
## Overdriving the XTAL Interface

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL\_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.



**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**



**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**





## Schematic Example

Figure 5A shows a schematic example of using an 843021. An example of LVPECL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18pF

parallel resonant crystal is used for generating 125MHz output frequency. The C1 = 27pF and C2 = 33pF are recommended for frequency accuracy. For a different board layout, the C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.

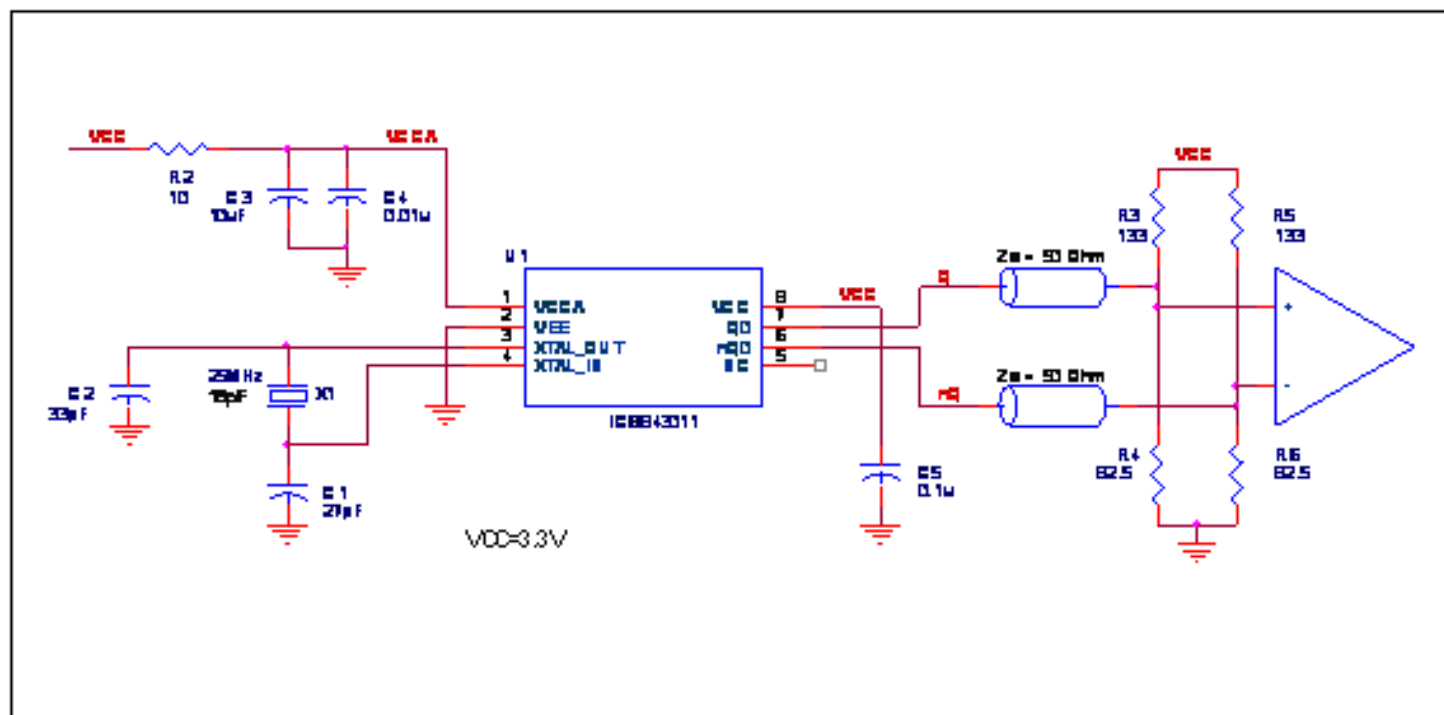


Figure 5. 843021 Schematic Example

## Schematic Example

Figure 5B shows an example of 843021 P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the Table 7. There should be

at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

Table 7. Footprint Table

Reference	Size
C1, C2	0402
C3	0805
C4, C5	0603
R2	0603

NOTE: Table 7 lists component sizes shown in this layout example.

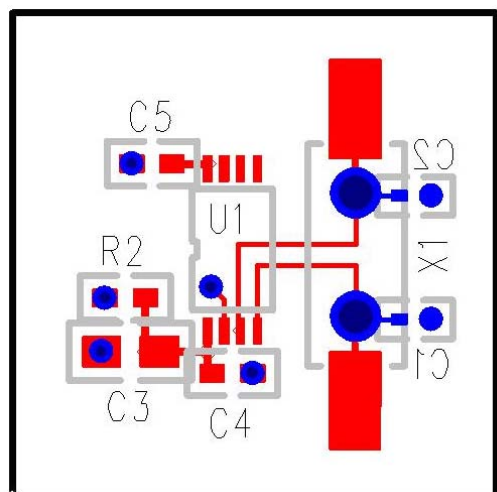


Figure 5B. 843021 PC Board Layout Example

## Power Considerations

This section provides information on power dissipation and junction temperature for the 843021. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 843021 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 10\% = 3.63V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.63V * 85mA = \mathbf{308.6mW}$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**

**Total Power**<sub>MAX</sub> (3.63V, with all outputs switching) =  $308.6mW + 30mW = \mathbf{338.6mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 90.5°C/W per Table 8 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^{\circ}C + 0.339W * 90.5^{\circ}C/W = 100.7^{\circ}C. \text{ This is below the limit of } 125^{\circ}C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

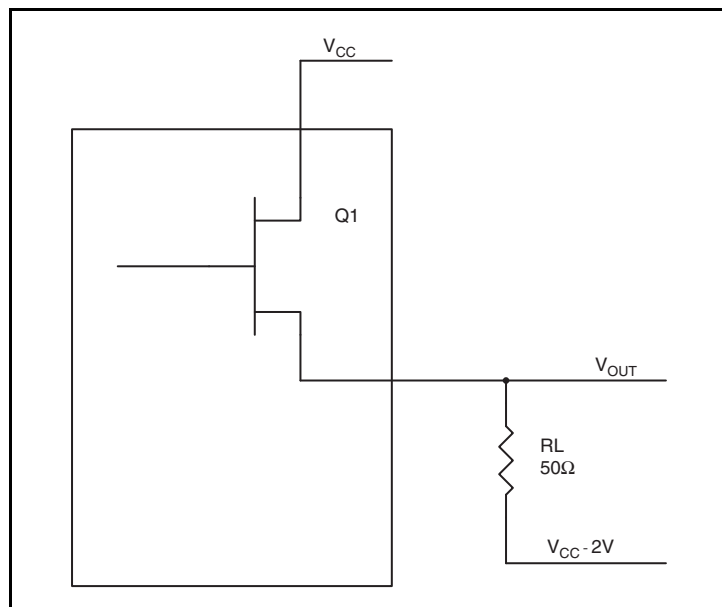
**Table 8. Thermal Resistance  $\theta_{JA}$  for 8 Lead TSSOP, Forced Convection**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 6*.



**Figure 6. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V<sub>CC</sub> - 2V.

- For logic high, V<sub>OUT</sub> = V<sub>OH\_MAX</sub> = V<sub>CC\_MAX</sub> - 0.9V  
(V<sub>CC\_MAX</sub> - V<sub>OH\_MAX</sub>) = 0.9V
- For logic low, V<sub>OUT</sub> = V<sub>OL\_MAX</sub> = V<sub>CC\_MAX</sub> - 1.7V  
(V<sub>CC\_MAX</sub> - V<sub>OL\_MAX</sub>) = 1.7V

Pd\_H is power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{30mW}$$

## Reliability Information

Table 9.  $\theta_{JA}$  vs. Air Flow Table for a 8 Lead TSSOP

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

## Transistor Count

The transistor count for 843021 is: 1928

## Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

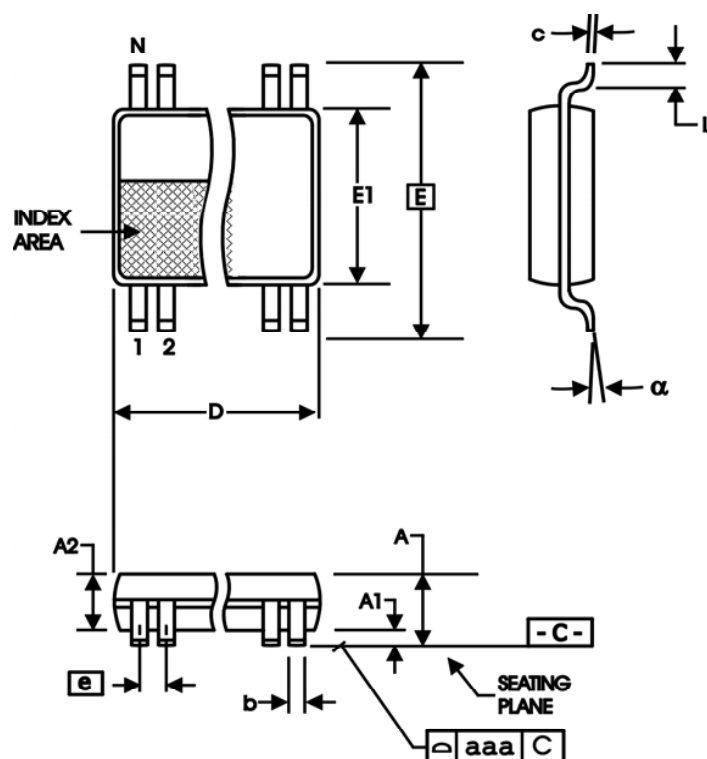


Table 10. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843021AGLF	021AL	"Lead-Free" 8 Lead TSSOP	Tube	0°C to 70°C
843021AGLFT	021AL	"Lead-Free" 8 Lead TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T5 T6	1	Added Function Table.	10/6/04
		3	Features section - updated Crystal, Output Frequency & VCO range bullets.	
		4	Crystal Characteristics Table - changed Frequency from 25MHz typical to 14MHz min. and 40MHz max. Added Note 1.	
B	T6	4	AC Characteristics Table - changed Output Frequency from 125MHz typical to 112MHz min. and 140MHz max.	
B	T11	12	Ordering Information Table - corrected count from 154 per tube to 100	10/15/04
C	T4A	3	Power Supply Table - increased $V_{CC}$ to $3.3V \pm 10\%$ from 5% and is reflected throughout the datasheet.	11/3/04
C	T8 T9 T11	3	Absolute Maximum Ratings - corrected Package Thermal Impedance air flow.	11/30/04
		9	Thermal Resistance Table - corrected air flow.	
		11	Corrected air flow in table.	
		12	Ordering Information Table - corrected marking.	
C	T11	1	Features Section - added Lead-Free bullet.	3/31/05
		12	Ordering Information Table - added Lead-Free part number.	
D	T6	1	Features section - changed RMS phase jitter spec.	11/21/07
		4	AC Characteristics Table - added maximum RMS Phase Jitter spec of 0.65ps.	
		7	Added <i>LVC MOS to XTAL Interface</i> section.	
		7	Added <i>Termination for 3.3V LVPECL Output</i> section.	
D	T4B T6 T11		Updated datasheet to new format.	10/12/10
		3	LVPECL DC Characteristics Table - corrected $V_{OH}/V_{OL}$ parameters from "Current" to "Voltage" and units from "uA" to "V".	
		3	AC Characteristics Table - added thermal note.	
		6	Updated text in "Power Supply Filtering Techniques".	
		7	Updated "Overdriving the Crystal Interface" section.	
D	T11	13	Ordering Information Table - deleted "ICS" prefix for part/order column.	9/25/15
			Updated header/footer.	
D	T11	13	Ordering Information - removed leaded devices.	
			Updated data sheet format.	



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