

3.3V CMOS 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH162374

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in TSSOP package

DRIVE FEATURES:

- Balanced Output Drivers: $\pm 12mA$
- Low switching noise

APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

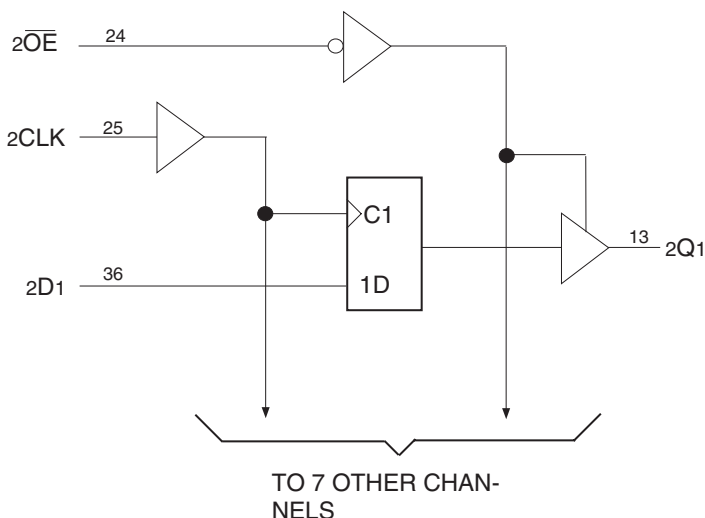
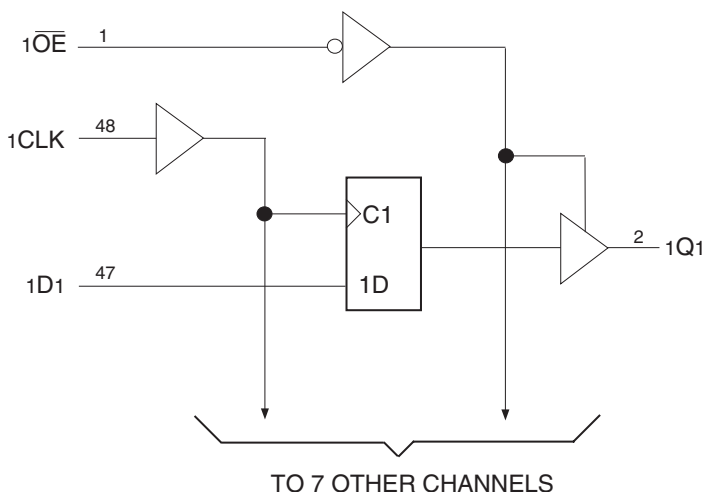
DESCRIPTION:

This 16-bit edge-triggered D-type flip-flop is built using advanced dual metal CMOS technology. The ALVCH162374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs. \overline{OE} can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

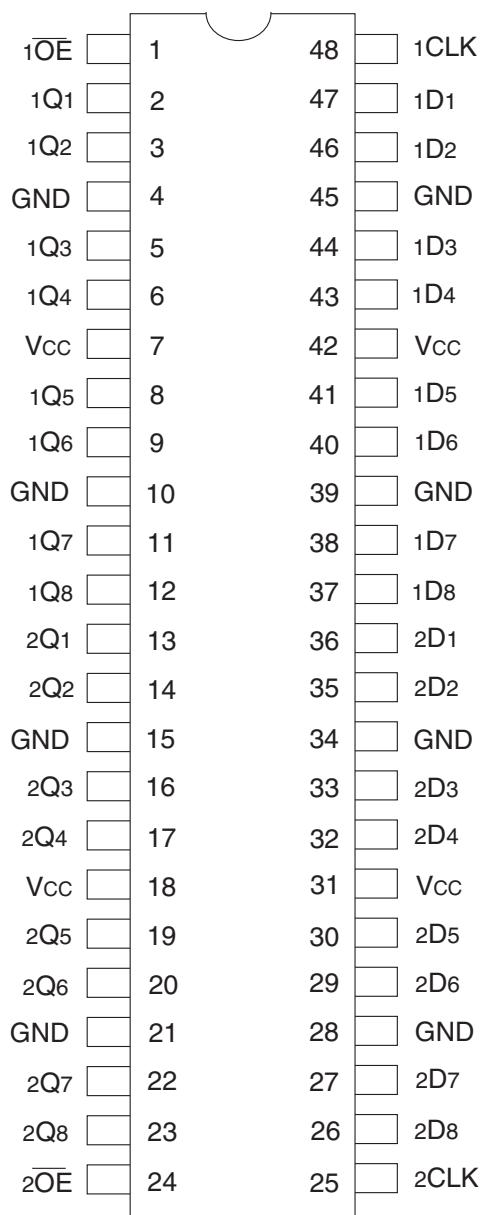
The ALVCH162374 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12mA$ at the designated threshold levels.

The ALVCH162374 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistor.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
IIK	Continuous Clamp Current, VI < 0 or VI > VCC	±50	mA
IOK	Continuous Clamp Current, VO < 0	-50	mA
ICC ISS	Continuous Current through each VCC or GND	±100	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- All terminals except VCC.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	7	pF
COUT	Output Capacitance	VOUT = 0V	7	9	pF
CIO	I/O Port Capacitance	VIN = 0V	7	9	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
x Dx	Data Inputs ⁽¹⁾
x CLK	Clock Inputs
x Qx	3-State Outputs
x OE	3-State Output Enable Input (Active LOW)

NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (EACH FLIP-FLOP)⁽¹⁾

Inputs			Outputs
x OE	x CLK	x Dx	x Qx
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀ ⁽²⁾
H	X	X	Z

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	± 5	μA
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	± 10	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 10	
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.1	40	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	750	μA

NOTE:

1. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 3\text{V}$	$V_I = 2\text{V}$	-75	—	—	μA
			$V_I = 0.8\text{V}$	75	—	—	
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	-45	—	—	μA
			$V_I = 0.7\text{V}$	45	—	—	
I_{BHHO} I_{BHL0}	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 3.6V	—	—	± 500	μA

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 4mA	1.9	—	
			IOH = - 6mA	1.7	—	
		VCC = 2.7V	IOH = - 4mA	2.2	—	
			IOH = - 8mA	2	—	
		VCC = 3V	IOH = - 6mA	2.4	—	
			IOH = - 12mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	—	0.55	
		VCC = 2.7V	IOL = 4mA	—	0.4	
			IOL = 8mA	—	0.6	
		VCC = 3V	IOL = 6mA	—	0.55	
			IOL = 12mA	—	0.8	

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range.
TA = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	28	31	pF
CPD	Power Dissipation Capacitance Outputs disabled		10	11	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	VCC = 2.5V ± 0.2V		VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fMAX		150	—	150	—	150	—	MHz
tPLH tPHL	Propagation Delay xCLK to xQx	1	5.4	—	5.4	1	4.6	ns
tPZH tPZL	Output Enable Time xOE to xQx	1	6.5	—	6.4	1	5.2	ns
tPHZ tPLZ	Output Disable Time xOE to xQx	1	5.6	—	5	1.2	4.5	ns
tSU	Setup Time, data before CLK↑	2.1	—	2.2	—	1.9	—	ns
tH	Hold Time, data after CLK↑	0.6	—	0.5	—	0.5	—	ns
tW	Pulse Duration, LE HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
tsk(0)	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

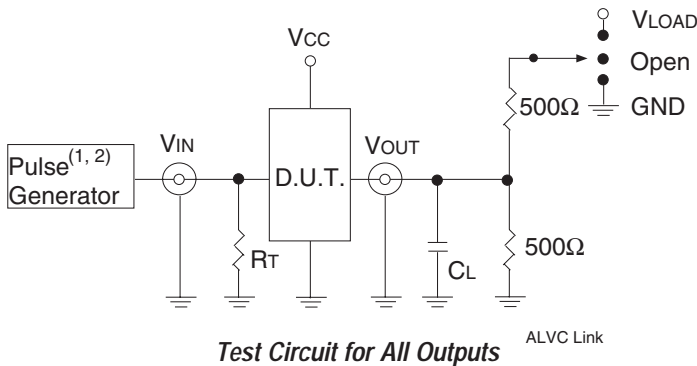
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

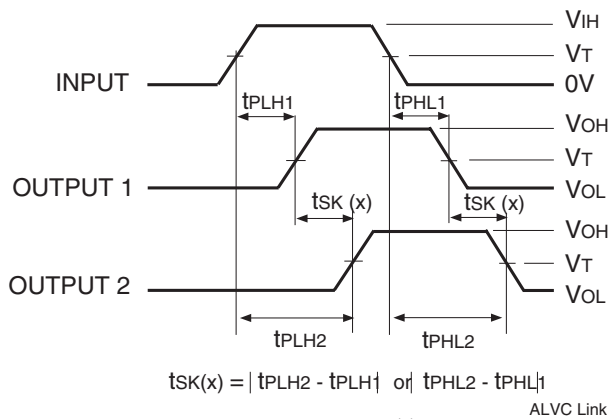
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_r ≤ 2ns.

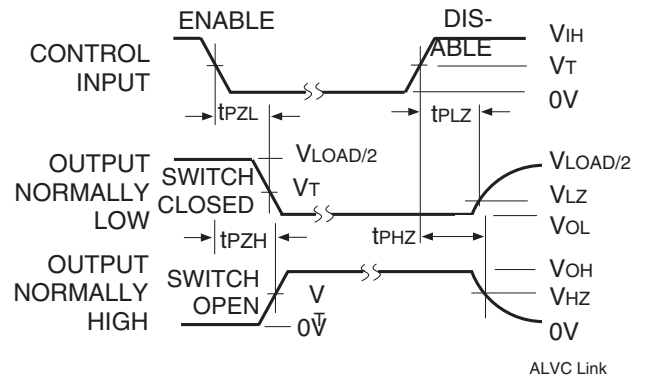
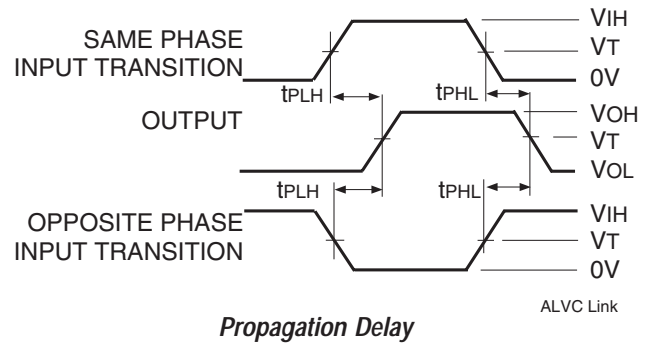
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



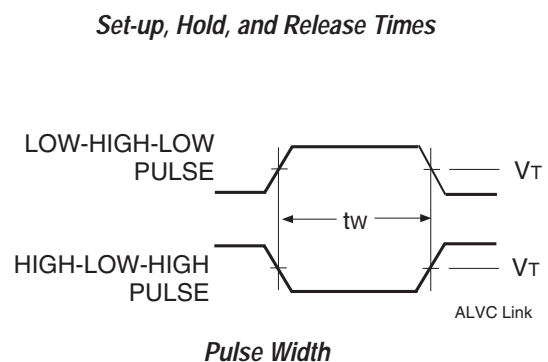
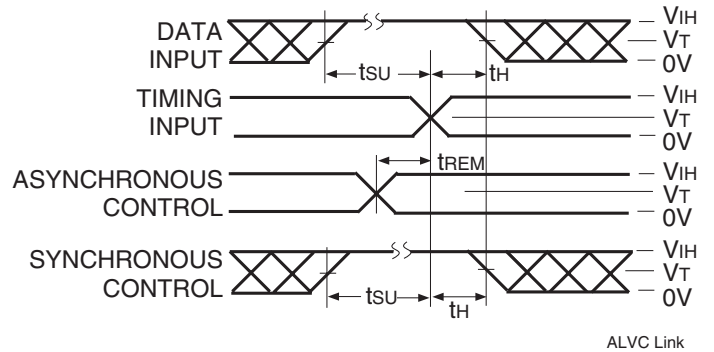
NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



ORDERING INFORMATION

XX	ALVC	X	XX	XXX	XX	
Temp. Range		Bus-Hold	Family	Device Type	Package	
					PAG	Thin Shrink Small Outline Package - Green
				374		16-Bit Edge-Triggered D-Type Flip-Flop with 3-State Outputs
			162			Double-Density with Resistors, ±12mA
		H				Bus-Hold
74						– 40°C to +85°C

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.