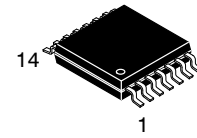


Low Voltage Quad 2-Input AND Gate with 3.6 V Tolerant Inputs and Outputs

74ALVC08



TSSOP-14 WB
CASE 948G

General Description

The ALVC08 contains four 2-input AND gates. This product is designed for low voltage (1.65 V to 3.6 V) V_{CC} applications with I/O compatibility up to 3.6 V.

The ALVC08 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Features

- 1.65 V to 3.6 V V_{CC} Supply Operation
- 3.6 V Tolerant Inputs and Outputs
- t_{PD}
 - ◆ 2.9 ns Max for 3.0 V to 3.6 V V_{CC}
 - ◆ 3.2 ns Max for 2.3 V to 2.7 V V_{CC}
 - ◆ 5.3 ns Max for 1.65 V to 1.95 V V_{CC}
- Power-off High Impedance Inputs and Outputs
- Uses Quiet Series Noise/EMI Reduction Circuitry
- Latchup Conforms to JEDEC JED78
- ESD Performance:
 - ◆ Human Body Model > 2000 V
 - ◆ Machine Model > 250 V
- These Devices are Pb-Free and Halide Free

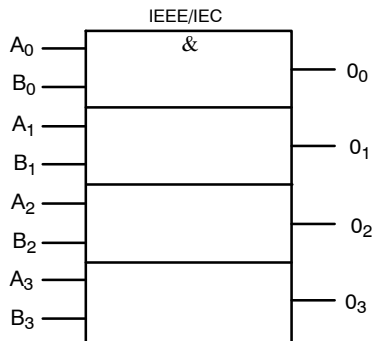
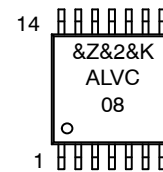


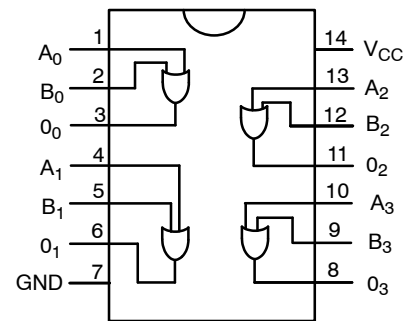
Figure 1. Logic Diagram

MARKING DIAGRAM



- &Z = Assembly Location
- &2 = 2-Digit Date Code (Year & Week)
- &K = Lot Run Traceability Code
- ALVC08 = Specific Device Code

CONNECTION DIAGRAM



ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|--------------------|--------------------|
| 74ALVC08MTCX | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

PIN DESCRIPTION

| Pin | Description |
|------------|-------------|
| A_n, B_n | Inputs |
| O_n | Outputs |

74ALVC08

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|--------------------------|---|------------------------|--------------|
| V_{CC} | Supply Voltage | -0.5 to + 4.6 | V |
| V_I | DC Input Voltage | -0.5 to + 4.6 | V |
| V_O | Output Voltage (Note 1) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | DC Input Diode Current $V_I < 0$ V | -50 | mA |
| I_{OK} | DC Output Diode Current $V_O < 0$ V | -50 | mA |
| I_{OH}/I_{OL} | DC Output Source / Sink Current | ± 50 | mA |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current per Output Pin | ± 100 | mA |
| T_{STG} | Storage Temperature | -65 to +150 | $^{\circ}$ C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS (Note 2)

| Symbol | Parameter | Min | Max | Unit |
|-----------------------|---|------|----------|--------------|
| V_{CC} | Supply Voltage | 1.65 | 3.6 | V |
| V_I | Input Voltage | 0 | V_{CC} | V |
| V_O | Output Voltage | 0 | V_{CC} | V |
| T_A | Free Air Operating Temperature | -40 | +85 | $^{\circ}$ C |
| $\Delta t / \Delta V$ | Input Edge Rate, $V_{IN} = 0.8$ V to 2.0 V, $V_{CC} = 3.0$ V | 0 | 5 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- I_O Absolute Maximum Rating must be observed, limited to 4.6 V.
- Floating or unused control inputs must be held HIGH or LOW.

74ALVC08

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | V _{CC} (V) | Min | Max | Unit |
|--------------------------|---------------------------------------|---|---------------------|------------------------|------------------------|------|
| V _{IH} | HIGH Level Input Voltage | | 1.65 – 1.95 | 0.65 × V _{CC} | – | V |
| | | | 2.3 – 2.7 | 1.7 | – | |
| | | | 2.7 – 3.6 | 2.0 | – | |
| V _{IL} | LOW Level Input Voltage | | 1.65 – 1.95 | – | 0.35 × V _{CC} | V |
| | | | 2.3 – 2.7 | – | 0.7 | |
| | | | 2.7 – 3.6 | – | 0.8 | |
| V _{OH} | HIGH Level Output Voltage | I _{OH} = –100 μA | 1.65 – 3.6 | V _{CC} – 0.2 | – | V |
| | | I _{OH} = –4 mA | 1.65 | 1.2 | – | |
| | | I _{OH} = –6 mA | 2.3 | 2.0 | – | |
| | | I _{OH} = –12 mA | 2.3 | 1.7 | – | |
| | | | 2.7 3.0 | 2.2 2.4 | – | |
| I _{OH} = –24 mA | 3.0 | 2 | – | | | |
| V _{OL} | LOW Level Output Voltage | I _{OL} = 100 μA | 1.65 – 3.6 | – | 0.2 | V |
| | | I _{OL} = 4 mA | 1.65 | – | 0.45 | |
| | | I _{OL} = 6 mA | 2.3 | – | 0.4 | |
| | | I _{OL} = 12 mA | 2.3 | – | 0.7 | |
| | | | 2.7 | – | 0.4 | |
| I _{OL} = 24 mA | 3.0 | – | 0.55 | | | |
| I _I | Input Leakage Current | 0 ≤ V _I ≤ 3.6 V | 3.6 | – | ±5.0 | μA |
| I _{CC} | Quiescent Supply Current | V _I = V _{CC} or GND, I _O = 0 | 3.6 | – | 40 | μA |
| ΔI _{CC} | Increase in I _{CC} per Input | V _{IH} = V _{CC} – 0.6 V | 3 – 3.6 | – | 750 | μA |

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | T _A = –40°C to +85°C, R _L = 500 Ω | | | | | | | | Unit |
|-------------------------------------|-------------------|---|------|-------------------------|------|--------------------------------|------|---------------------------------|------|------|
| | | C _L = 50 pF | | | | C _L = 30 pF | | | | |
| | | V _{CC} = 3.3 V ±0.3 V | | V _{CC} = 2.7 V | | V _{CC} = 2.5 V ±0.2 V | | V _{CC} = 1.8 V ±0.15 V | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{PHL} , t _{PLH} | Propagation Delay | 1.2 | 2.9 | – | 3.0 | 1.0 | 3.2 | 1.2 | 5.3 | ns |

CAPACITANCE

| Symbol | Parameter | Conditions | T _A = +25°C | | Unit |
|-----------------|-------------------------------|---|------------------------|-----|------|
| | | | V _{CC} | Typ | |
| C _{IN} | Input Capacitance | V _I = 0 V or V _{CC} | 3.3 | 4.5 | pF |
| C _{PD} | Power Dissipation Capacitance | f = 10 MHz, C _L = 50 pF | 3.3 | 26 | pF |
| | | | 2.5 | 25 | |
| | | | 1.8 | 24 | |

74ALVC08

AC LOADING AND WAVEFORMS

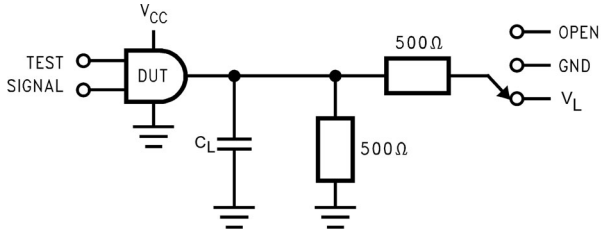


Figure 2. AC Test Circuit

Table 1. VALUES FOR FIGURE 2

| Test | Switch |
|-----------------------|--------|
| t_{PLH} , t_{PHL} | Open |

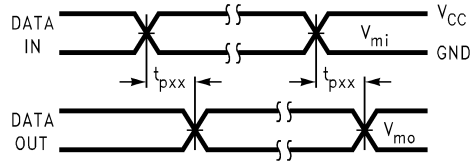


Figure 3. Waveform for Inverting and Non-Inverting Functions

Table 2. VARIABLE MATRIX (Input Characteristics; $f = 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$; $Z_0 = 5 \Omega$)

| Symbol | V_{CC} | | | |
|----------|-----------------------------------|-----------------|-----------------------------------|------------------------------------|
| | $3.3 \text{ V} \pm 0.3 \text{ V}$ | 2.7 V | $2.5 \text{ V} \pm 0.2 \text{ V}$ | $1.8 \text{ V} \pm 0.15 \text{ V}$ |
| V_{mi} | 1.5 V | 1.5 V | $V_{CC}/2$ | $V_{CC}/2$ |
| V_{mo} | 1.5 V | 1.5 V | $V_{CC}/2$ | $V_{CC}/2$ |

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*

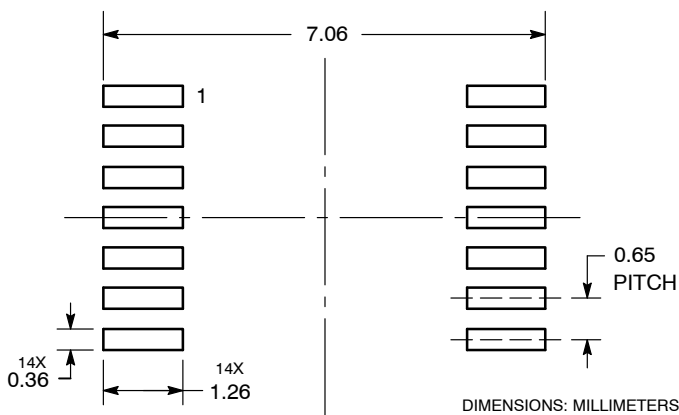


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT



| | | |
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