

74LVC2G06-Q100

Inverters with open-drain outputs

Rev. 4 — 15 August 2023

Product data sheet

1. General description

The 74LVC2G06-Q100 is a dual inverter with open-drain outputs. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- -24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
 - JESD36 (4.5 V to 5.5 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|----------------------------------|-------------------|--------------|--|--------------------------|
| | Temperature range | Name | Description | |
| 74LVC2G06GW-Q100 | -40 °C to +125 °C | TSSOP6 | plastic thin shrink small outline package; 6 leads; body width 1.25 mm | SOT363-2 |
| 74LVC2G06GV-Q100 | -40 °C to +125 °C | SC-74; TSOP6 | plastic surface-mounted package; 6 leads | SOT457 |

4. Marking

Table 2. Marking

| Type number | Marking code[1] |
|------------------|-----------------|
| 74LVC2G06GW-Q100 | V6 |
| 74LVC2G06GV-Q100 | V06 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Logic diagram (one inverter)

6. Pinning information

6.1. Pinning

GW package
SOT363-2 (TSSOP6)

aaa-035770

GV package
SOT457 (SC-74; TSOP6)

aaa-035922

6.2. Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|-----------------|-----|----------------|
| 1A | 1 | data input |
| GND | 2 | ground (0 V) |
| 2A | 3 | data input |
| 2Y | 4 | data output |
| V _{CC} | 5 | supply voltage |
| 1Y | 6 | data output |

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

| Input nA | Output nY |
|----------|-----------|
| L | Z |
| H | L |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--|------|------|------|
| V _{CC} | supply voltage | | -0.5 | +6.5 | V |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA |
| V _I | input voltage | [1] | -0.5 | +6.5 | V |
| I _{OK} | output clamping current | V _O < 0 V | -50 | - | mA |
| V _O | output voltage | Active mode [1] | -0.5 | +6.5 | V |
| | | Power-down mode; V _{CC} = 0 V [1] | -0.5 | +6.5 | V |
| I _O | output current | V _O = 0 V to 6.5 V | - | 50 | mA |
| I _{CC} | supply current | | - | 100 | mA |
| I _{GND} | ground current | | -100 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C [2] | - | 250 | mW |

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.

For SOT457 (SC-74; TSOP6) package: P_{tot} derates linearly with 4.1 mW/K above 89 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---------------------------------|------|-----|------|------|
| V_{CC} | supply voltage | | 1.65 | - | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | Active mode | 0 | - | 5.5 | V |
| | | Power-down mode; $V_{CC} = 0$ V | 0 | - | 5.5 | V |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to 2.7 V | - | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 5.5 V | - | - | 10 | ns/V |

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---------------------------------|---------------------------|---|----------------------|-----------|----------------------|---------|
| $T_{amb} = -40$ °C to +85 °C | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | $0.65 \times V_{CC}$ | - | - | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | 1.7 | - | - | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 2.0 | - | - | V |
| | | $V_{CC} = 4.5$ V to 5.5 V | $0.7 \times V_{CC}$ | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | - | - | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | - | - | 0.7 | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | - | - | 0.8 | V |
| | | $V_{CC} = 4.5$ V to 5.5 V | - | - | $0.3 \times V_{CC}$ | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $I_O = 100$ μ A; $V_{CC} = 1.65$ V to 5.5 V | - | - | 0.1 | V |
| | | $I_O = 4$ mA; $V_{CC} = 1.65$ V | - | - | 0.45 | V |
| | | $I_O = 8$ mA; $V_{CC} = 2.3$ V | - | - | 0.3 | V |
| | | $I_O = 12$ mA; $V_{CC} = 2.7$ V | - | - | 0.4 | V |
| | | $I_O = 24$ mA; $V_{CC} = 3.0$ V | - | - | 0.55 | V |
| $I_O = 32$ mA; $V_{CC} = 4.5$ V | - | - | 0.55 | V | | |
| I_I | input leakage current | $V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V [2] | - | ± 0.1 | ± 1 | μ A |
| I_{OZ} | OFF-state output current | $V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5$ V | - | ± 0.1 | ± 2 | μ A |
| I_{OFF} | power-off leakage current | V_I or $V_O = 5.5$ V; $V_{CC} = 0$ V | - | ± 0.1 | ± 2 | μ A |
| I_{CC} | supply current | $V_I = 5.5$ V or GND; $I_O = 0$ A; $V_{CC} = 1.65$ V to 5.5 V | - | 0.1 | 4 | μ A |
| ΔI_{CC} | additional supply current | per pin; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.3$ V to 5.5 V [2] | - | 5 | 500 | μ A |
| C_I | input capacitance | | - | 2.5 | - | pF |

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|--|---------------------------|--|------------------------|--------|------------------------|------|
| T_{amb} = -40 °C to +125 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | - | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | V |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | V |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 0.3 × V _{CC} | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V | - | - | 0.10 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | - | 0.70 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | - | 0.45 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | - | 0.60 | V |
| | | I _O = 24 mA; V _{CC} = 3.0 V | - | - | 0.80 | V |
| | | I _O = 32 mA; V _{CC} = 4.5 V | - | - | 0.80 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | ±1 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±2 | μA |
| I _{OFF} | power-off leakage current | V _I or V _O = 5.5 V; V _{CC} = 0 V | - | - | ±2 | μA |
| I _{CC} | supply current | V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V | - | - | 4 | μA |
| ΔI _{CC} | additional supply current | per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V | - | - | 500 | μA |

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 5.

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|---|------------------|--------|-----|-------------------|-----|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| t _{pd} | propagation delay | nA to nY; see Fig. 4 [2] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.0 | 3.2 | 6.5 | 1.0 | 8.2 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.5 | 2.0 | 3.9 | 0.5 | 4.9 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 2.6 | 4.2 | 1.0 | 5.3 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 0.5 | 2.3 | 3.4 | 0.5 | 4.3 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 0.5 | 1.6 | 2.9 | 0.5 | 3.7 | ns |
| C _{PD} | power dissipation capacitance | V _I = GND to V _{CC} ; V _{CC} = 3.3 V [3] | - | 5.9 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLZ} and t_{PZL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

∑(C_L × V_{CC}² × f_o) = sum of outputs.

11.1. Waveform and test circuit

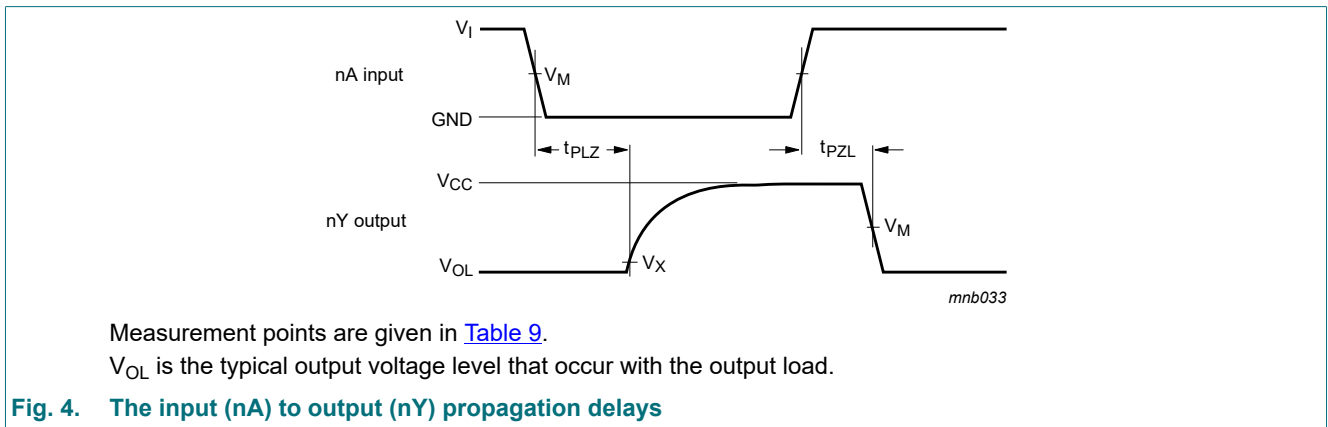
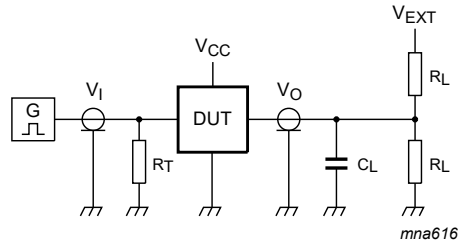


Table 9. Measurement points

| Supply voltage | Input | Output | |
|------------------|-----------------------|-----------------------|--------------------------|
| V _{CC} | V _M | V _M | V _X |
| 1.65 V to 1.95 V | 0.5 × V _{CC} | 0.5 × V _{CC} | V _{OL} + 0.15 V |
| 2.3 V to 2.7 V | 0.5 × V _{CC} | 0.5 × V _{CC} | V _{OL} + 0.15 V |
| 2.7 V | 1.5 V | 1.5 V | V _{OL} + 0.3 V |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V | V _{OL} + 0.3 V |
| 4.5 V to 5.5 V | 0.5 × V _{CC} | 0.5 × V _{CC} | V _{OL} + 0.3 V |



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 5. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | | Load | | V_{EXT} |
|------------------|----------|---------------|-------|--------------|--------------------|
| V_{CC} | V_I | t_r, t_f | C_L | R_L | t_{PZL}, t_{PLZ} |
| 1.65 V to 1.95 V | V_{CC} | ≤ 2.0 ns | 30 pF | 1 k Ω | $2 \times V_{CC}$ |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2.0 ns | 30 pF | 500 Ω | $2 \times V_{CC}$ |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | 6 V |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | 6 V |
| 4.5 V to 5.5 V | V_{CC} | ≤ 2.5 ns | 50 pF | 500 Ω | $2 \times V_{CC}$ |

12. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm

SOT363-2

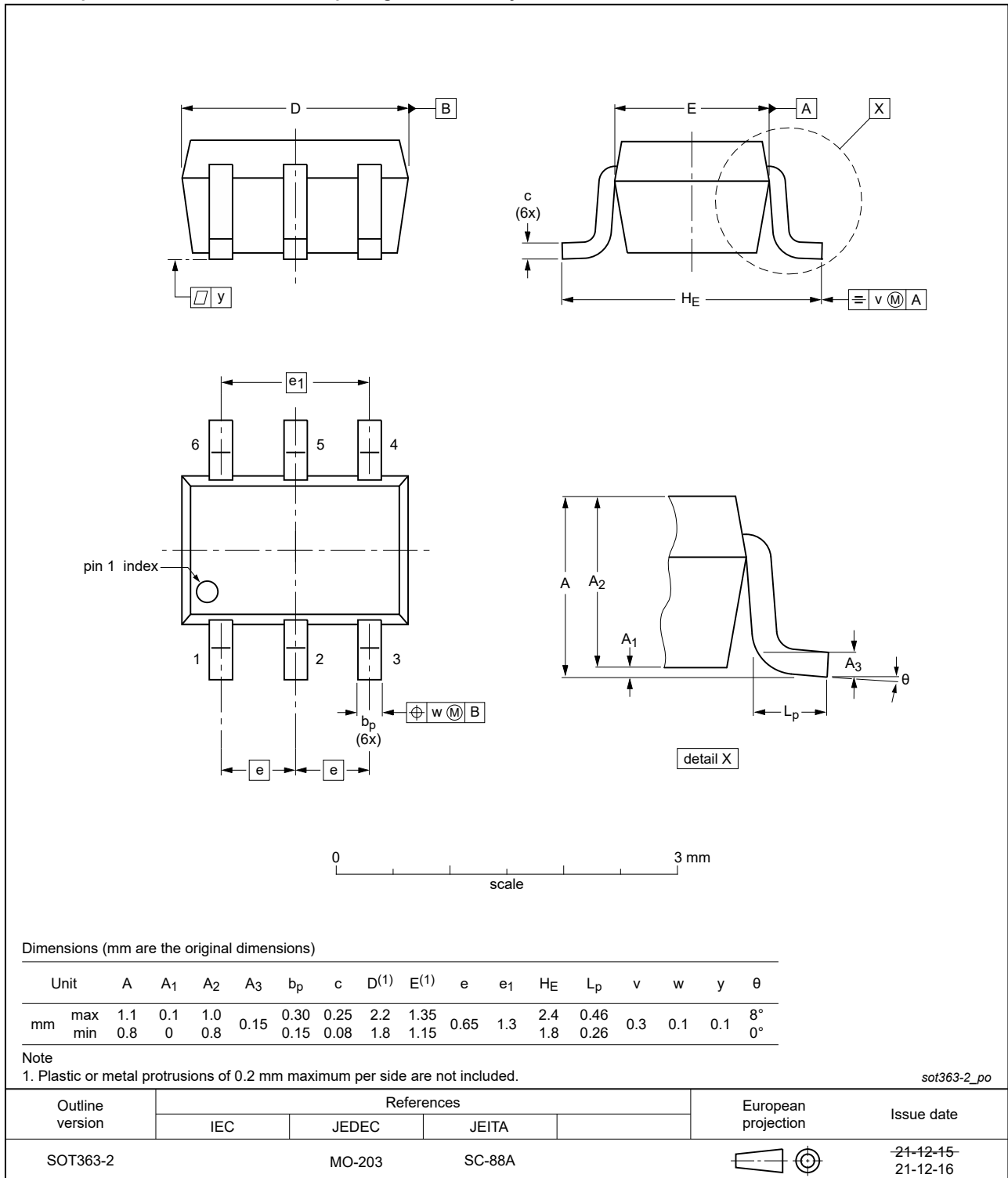


Fig. 6. Package outline SOT363-2 (TSSOP6)

Plastic, surface-mounted package (SC-74; TSOP6); 6 leads

SOT457

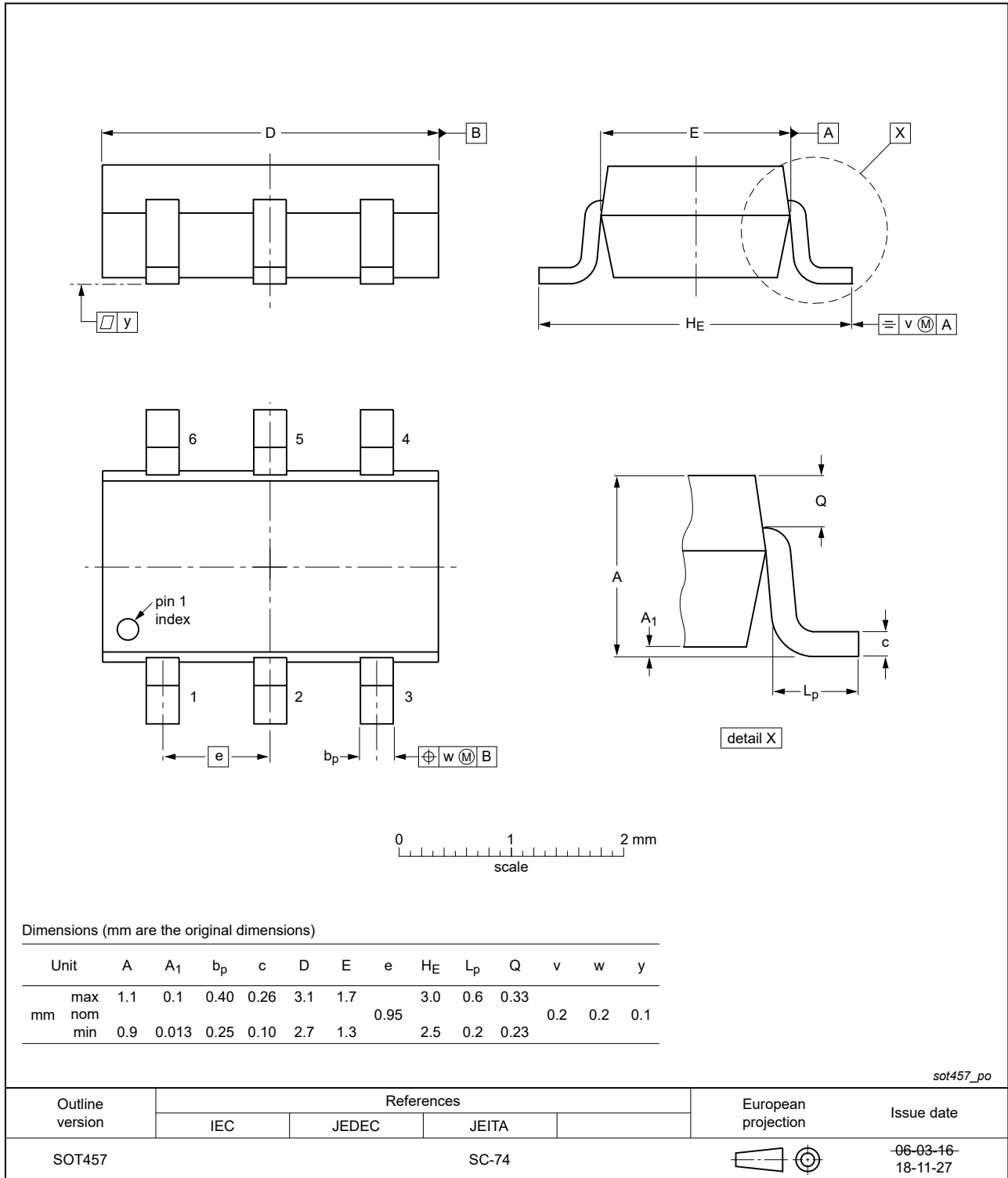


Fig. 7. Package outline SOT457 (SC-74; TSOP6)

13. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------|--|--------------------|---------------|--------------------|
| 74LVC2G06_Q100 v.4 | 20230815 | Product data sheet | - | 74LVC2G06_Q100 v.3 |
| Modifications: | <ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. | | | |
| 74LVC2G06_Q100 v.3 | 20220124 | Product data sheet | - | 74LVC2G06_Q100 v.2 |
| Modifications: | <ul style="list-style-type: none"> • Section 1 updated. • Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6). • Fig. 7: Package outline drawing for SOT457 (SC-74; TSOP6) has changed. • Table 5: Derating values for P_{tot} total power dissipation updated. | | | |
| 74LVC2G06_Q100 v.2 | 20161213 | Product data sheet | - | 74LVC2G06_Q100 v.1 |
| Modifications: | <ul style="list-style-type: none"> • Table 7: The maximum limits for leakage current and supply current have changed. | | | |
| 74LVC2G06_Q100 v.1 | 20120807 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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