74LVC1G08-Q100

Single 2-input AND gate

Rev. 5 — 4 August 2023 Product data sheet

1. General description

The 74LVC1G08-Q100 is a single 2-input AND gate. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

Schmitt trigger action at all inputs makes the circuit tolerant of slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power dissipation
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance ≤ 250 mA
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G08GW-Q100	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G08GV-Q100	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G08GM-Q100	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886

4. Marking

Table 2. Marking

Type number	Marking code [1]
74LVC1G08GW-Q100	VE
74LVC1G08GV-Q100	V08
74LVC1G08GM-Q100	VE

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

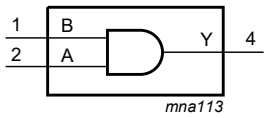


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

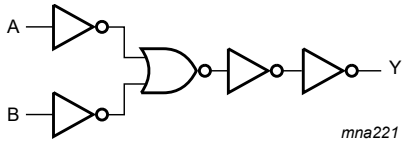


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning

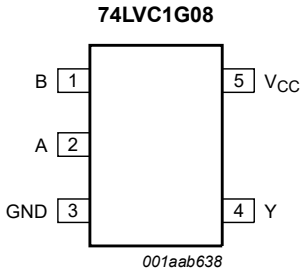
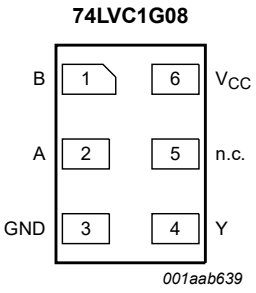


Fig. 4. Pin configuration SOT353-1 (TSSOP5) and SOT753 (SC-74A)



Transparent top view

Fig. 5. Pin configuration SOT886 (XSON6)

6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5 and SC-74A	XSON6	
B	1	1	data input
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V_{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode	[1]	-0.5	V_{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V	[1]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW
T_{stg}	storage temperature			-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.
For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65V_{CC}$	-	-	$0.65V_{CC}$	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} - 0.1	-	-	V_{CC} - 0.1	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2	-	-	0.95	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	1.9	-	-	1.7	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2	-	-	1.9	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.3	-	-	2.0	-	V
		I_O = -32 mA; V_{CC} = 4.5 V	3.8	-	-	3.4	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.10	-	0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.30	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.40	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	-	0.80	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	±0.1	±2	-	±2	µA
I_{CC}	supply current	V_I = 5.5 V or GND; I_O = 0 A; V_{CC} = 1.65 V to 5.5 V	-	0.1	4	-	4	µA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	5	500	-	500	µA
C_I	input capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}	-	5	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

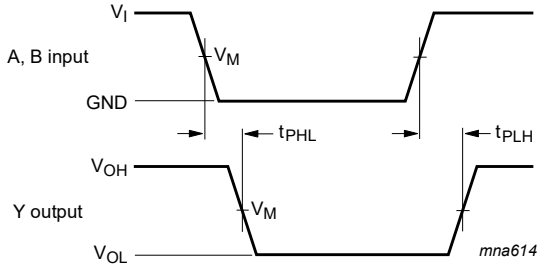
Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	A, B to Y; see Fig. 6 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.0	3.4	8.0	1.0	10.5	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	2.2	5.5	0.5	7.0	ns
		V_{CC} = 2.7 V	0.5	2.5	5.5	0.5	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	2.1	4.5	0.5	6.0	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	1.7	4.0	0.5	5.5	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V [3]	-	16	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
[2] t_{pd} is the same as t_{PLZ} and t_{PZL}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit

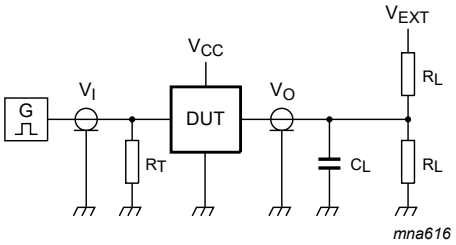


Measurement points are given in Table 9.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. The input A, B to output Y propagation delays

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

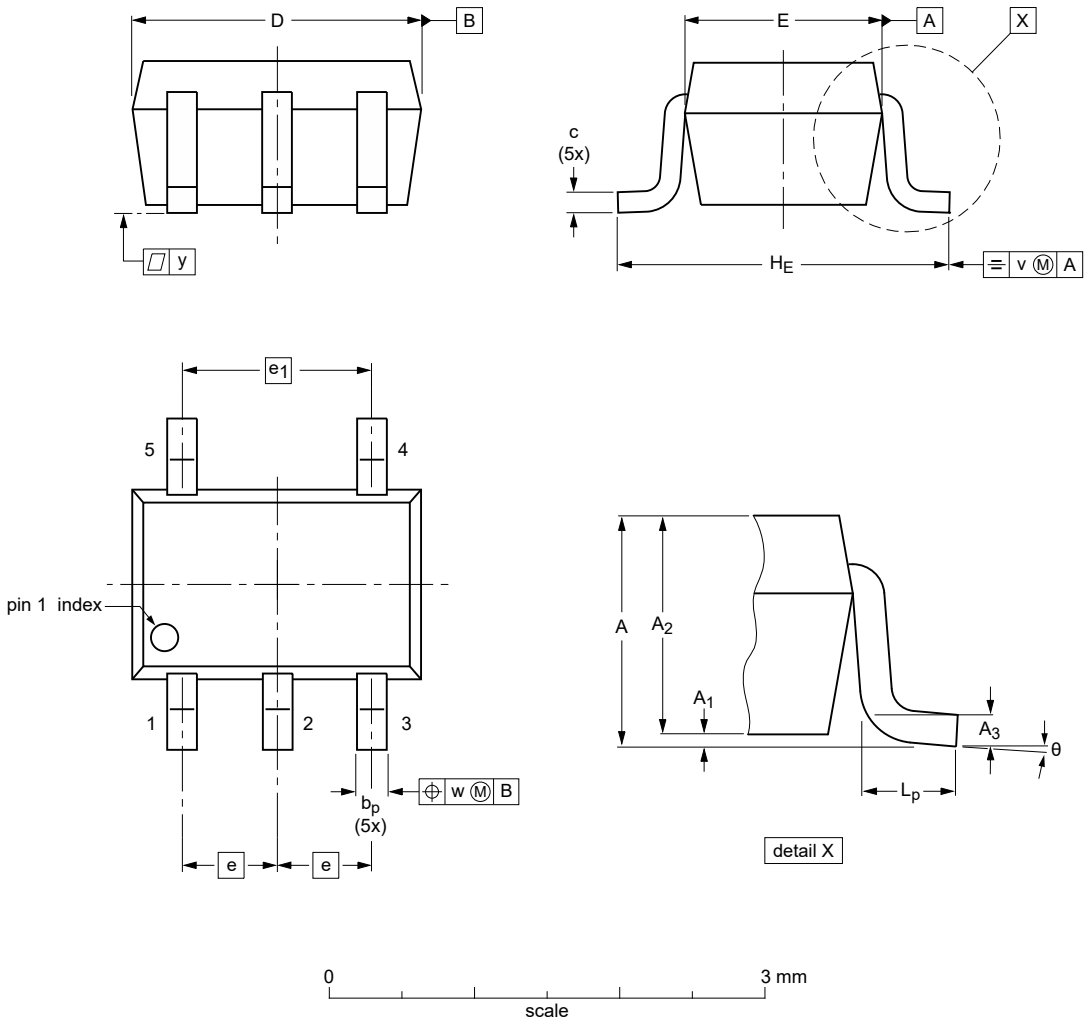
Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note

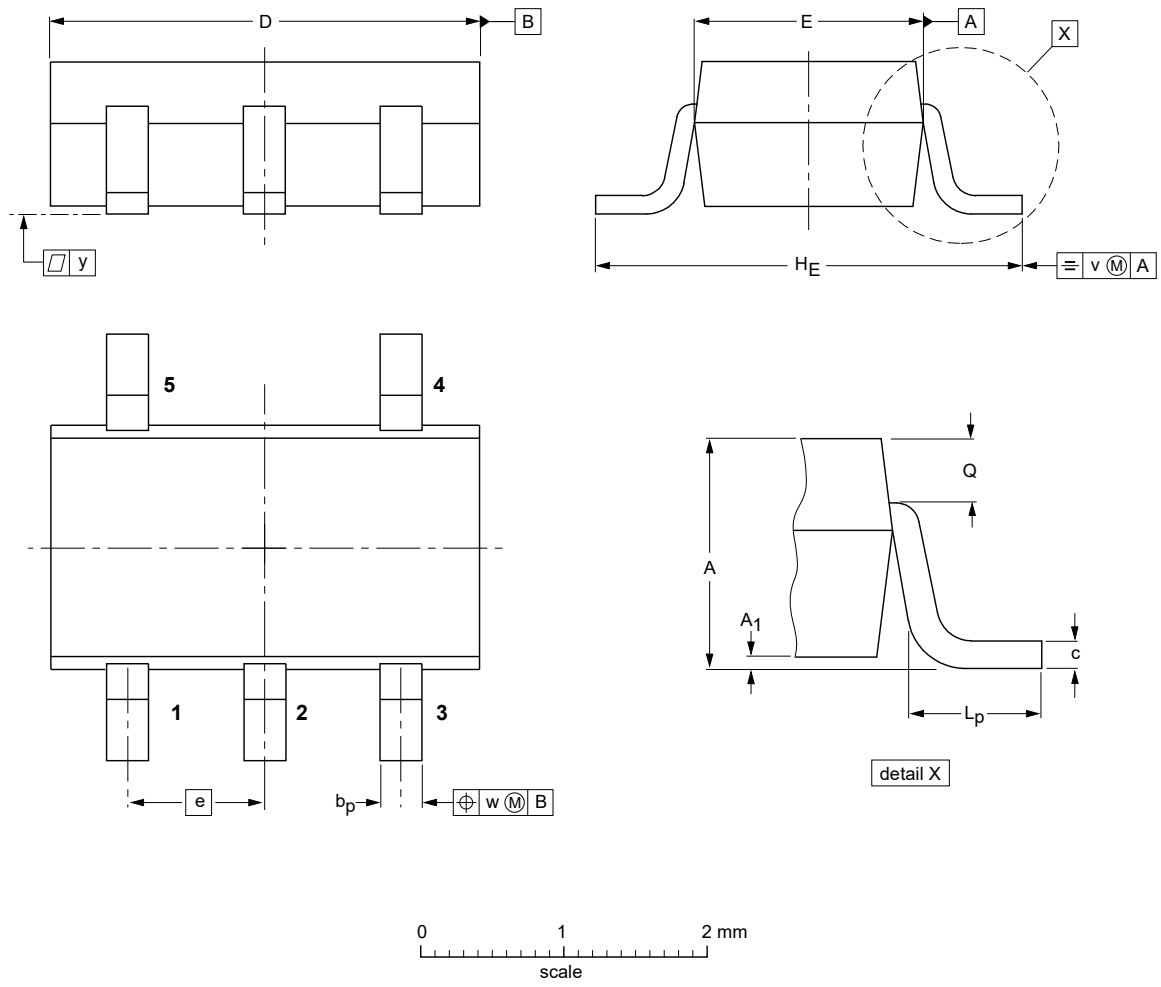
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot353-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 8. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads **SOT753**



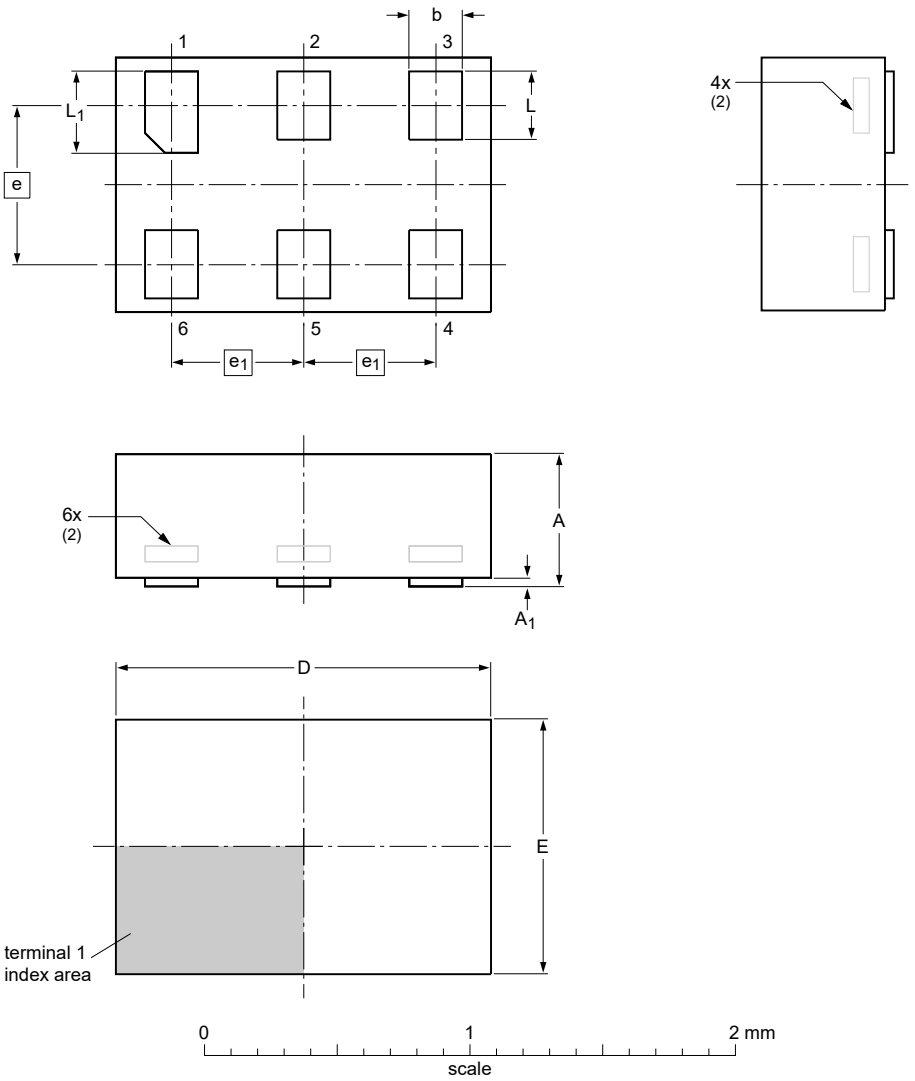
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig. 9. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm SOT886



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Fig. 10. Package outline SOT886 (XSON6)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G08_Q100 v.5	20230804	Product data sheet	-	74LVC1G08_Q100 v.4
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC1G08_Q100 v.4	20211115	Product data sheet	-	74LVC1G08_Q100 v.3
Modifications:	• Table 5: Derating values for P_{tot} total power dissipation updated. • Fig. 8: Package outline drawing for SOT353-1 (TSSOP5) has changed. • Section 1 and Section 2 updated.			
74LVC1G08_Q100 v.3	20190125	Product data sheet	-	74LVC1G08_Q100 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74LVC1G08GM-Q100 (SOT886) added.			
74LVC1G08_Q100 v.2	20161207	Product data sheet	-	74LVC1G08_Q100 v.1
Modifications:	• Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC1G08_Q100 v.1	20120709	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 4 August 2023