74LV1T04-Q100

Single supply translating inverter

Rev. 2 — 7 February 2022 Product data sheet

1. General description

The 74LV1T04-Q100 is a single, level translating inverting buffer. The low threshold inputs support 1.8 V input logic at V_{CC} = 3.3 V and can be used in 1.8 V to 3.3 V level up translation. In addition, the 5 V tolerant input pins enable level down translation (3.3 V to 2.5 V output at V_{CC} = 2.5 V). The output level is referenced to the supply voltage and supports 1.8 V, 2.5 V, 3.3 V and 5.0 V CMOS levels. The wide V_{CC} range permits the generation of output levels to connect to controllers or processors.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Single supply voltage translator at 1.8 V, 2.5 V, 3.3 V and 5.0 V
- Up translation
  - 1.2 V to 1.8 V at V_{CC} = 1.8 V
  - 1.5 V to 2.5 V at V_{CC} = 2.5 V
  - 1.8 V to 3.3 V at V_{CC} = 3.3 V
  - 3.3 V to 5.0 V at V_{CC} = 5.0 V
- Down translation
  - 3.3 V to 1.8 V at V_{CC} = 1.8 V
  - 3.3 V to 2.5 V at V_{CC} = 2.5 V
  - 5.0 V to 3.3 V at V_{CC} = 3.3 V
- 5 V tolerant inputs
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - CDM JESD22-C101 exceeds 1 kV

3. Applications

- Portable applications
- PC and notebooks
- Industrial controller
- Telecom

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV1T04GW-Q100	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1

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5. Marking

Table 2. Marking

Type number	Marking code[1]
74LV1T04GW-Q100	SG

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

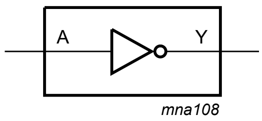


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

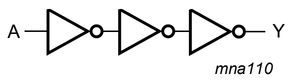


Fig. 3. Logic diagram

7. Pinning information

7.1. Pinning

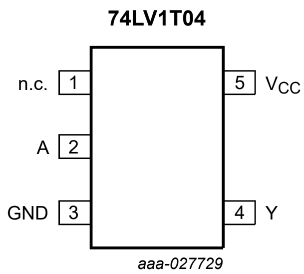


Fig. 4. Pin configuration SOT353-1 (TSSOP5)

7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V_{CC}	5	supply voltage

8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
A	**Y**
L	H
H	L

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage		[1]	-0.5	+7.0	V
V_O	output voltage	output HIGH or LOW state	[2][3]	-0.5	V_{CC} + 0.5	V
		output in power-off state	[2]	-0.5	4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-20	-	mA
I_{OK}	output clamping current	$V_O < 0$ V or $V_O > V_{CC}$		-	±20	mA
I_O	output current	$V_O = 0$ V to V_{CC}		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[4]	-	250	mW

[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.
[2] If the output current ratings are observed, the output voltage ratings may be exceeded.
[3] This value is limited to 7 V maximum.
[4] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.6	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.8 V to 5.0 V	-	-	20	ns/V

11. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.8 V	0.94	-	1.0	-	1.0	-	V
		V_{CC} = 2.0 V	0.99	-	1.03	-	1.03	-	V
		V_{CC} = 2.25 V to 2.5 V	1.135	-	1.18	-	1.18	-	V
		V_{CC} = 2.75 V	1.21	-	1.23	-	1.23	-	V
		V_{CC} = 3.0 V to 3.3 V	1.35	-	1.37	-	1.37	-	V
		V_{CC} = 3.6 V	1.47	-	1.48	-	1.48	-	V
		V_{CC} = 4.5 V to 5.0 V	2.02	-	2.03	-	2.03	-	V
		V_{CC} = 5.5 V	2.10	-	2.11	-	2.11	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 2.0 V	-	0.58	-	0.55	-	0.55	V
		V_{CC} = 2.25 V to 2.75 V	-	0.75	-	0.71	-	0.71	V
		V_{CC} = 3.0 V to 3.6 V	-	0.80	-	0.65	-	0.65	V
		V_{CC} = 4.5 V to 5.5 V	-	0.80	-	0.80	-	0.80	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL};							
		V_{CC} = 1.65 V to 5.5 V; I_O = -20 μA	V_{CC} - 0.1	-	V_{CC} - 0.1	-	V_{CC} - 0.1	-	V
		V_{CC} = 1.65 V; I_O = -2 mA	1.28	-	1.21	-	1.21	-	V
		V_{CC} = 1.8 V; I_O = -2 mA	1.5	-	1.45	-	1.45	-	V
		V_{CC} = 2.3 V; I_O = -2.3 mA	2.0	-	2.0	-	2.0	-	V
		V_{CC} = 2.3 V; I_O = -3 mA	2.0	-	1.93	-	1.93	-	V
		V_{CC} = 2.5 V; I_O = -3 mA	2.25	-	2.15	-	2.15	-	V
		V_{CC} = 3.0 V; I_O = -3 mA	2.78	-	2.7	-	2.7	-	V
		V_{CC} = 3.0 V; I_O = -5.5 mA	2.6	-	2.49	-	2.49	-	V
		V_{CC} = 3.3 V; I_O = -5.5 mA	2.9	-	2.8	-	2.8	-	V
		V_{CC} = 4.5 V; I_O = -4 mA	4.2	-	4.1	-	4.1	-	V
		V_{CC} = 4.5 V; I_O = -8 mA	4.1	-	3.95	-	3.95	-	V
		V_{CC} = 5.0 V; I_O = -8 mA	4.6	-	4.5	-	4.5	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}							
		V_{CC} = 1.65 V to 5.5 V; I_O = 20 μA	-	0.1	-	0.1	-	0.1	V
		V_{CC} = 1.65 V; I_O = 2 mA	-	0.2	-	0.25	-	0.25	V
		V_{CC} = 2.3 V; I_O = 2.3 mA	-	0.1	-	0.15	-	0.15	V
		V_{CC} = 2.3 V; I_O = 3 mA	-	0.15	-	0.2	-	0.2	V
		V_{CC} = 3.0 V; I_O = 3 mA	-	0.1	-	0.15	-	0.15	V
		V_{CC} = 3.0 V; I_O = 5.5 mA	-	0.2	-	0.252	-	0.252	V
		V_{CC} = 4.5 V; I_O = 4 mA	-	0.15	-	0.2	-	0.2	V
		V_{CC} = 4.5 V; I_O = 8 mA	-	0.3	-	0.35	-	0.35	V

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	Min	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 0 V to 5.5 V	-	±0.1	-	±1	-	±1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 1.8 V, 2.5 V, 3.3 V, 5.0 V	-	1	-	10	-	10	μA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 1.8 V; V_I = 0.3 V or 1.1 V; I_O = 0 A; other pins at V_{CC} or GND	-	10	-	10	-	10	μA
		per input pin; V_{CC} = 5.5 V; V_I = 0.3 V or 3.4 V; I_O = 0 A; other pins at V_{CC} or GND	-	1.35	-	1.5	-	1.5	mA

12. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V. For test circuit, see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	A, B to Y; see Fig. 5 [1]								
		V_{CC} = 1.8 V; C_L = 15 pF	-	6.2	9.6	-	10.7	-	11.5	ns
		V_{CC} = 1.8 V; C_L = 30 pF	-	7.3	11.3	-	12.7	-	13.5	ns
		V_{CC} = 2.5 V; C_L = 15 pF	-	4.4	6.5	-	7.4	-	7.9	ns
		V_{CC} = 2.5 V; C_L = 30 pF	-	5.2	7.6	-	8.6	-	9.1	ns
		V_{CC} = 3.3 V; C_L = 15 pF	-	3.7	5.3	-	5.9	-	6.3	ns
		V_{CC} = 3.3 V; C_L = 30 pF	-	4.3	6.1	-	6.8	-	7.2	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	3.1	4.1	-	4.4	-	4.6	ns
		V_{CC} = 5.0 V; C_L = 30 pF	-	3.6	4.6	-	5.0	-	5.2	ns
C_I	input capacitance	$V_I = V_{CC}$ or GND; V_{CC} = 3.3 V	-	1.5	10	-	10	-	10	pF
C_O	output capacitance	$V_O = V_{CC}$ or GND; V_{CC} = 3.3 V	-	2.5	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}; C_L = 30 pF; f = 10 MHz [2]								
		V_{CC} = 1.8 V	-	4.1	-	-	-	-	-	pF
		V_{CC} = 2.5 V	-	5.5	-	-	-	-	-	pF
		V_{CC} = 3.3 V	-	7.5	-	-	-	-	-	pF
		V_{CC} = 5.0 V	-	11.7	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \sum(C_L \times V_{CC}{}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

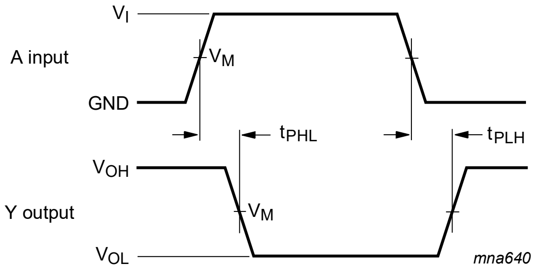
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs.

12.1. Waveforms and test circuit



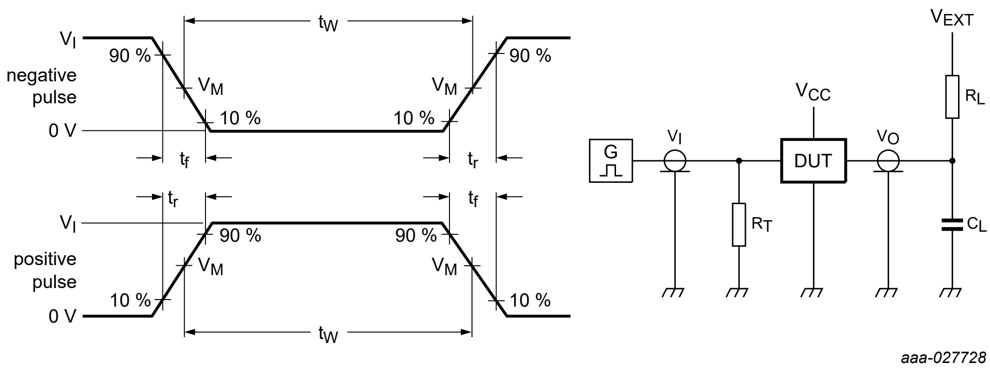
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. The input A to output Y propagation delays

Table 9. Measurement points

Input	**Output**
V_M	V_M
$0.5V_I$	$0.5 \times V_{CC}$



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

V_{EXT} = External voltage for measuring switching times.

Fig. 6. Test circuit for measuring switching times

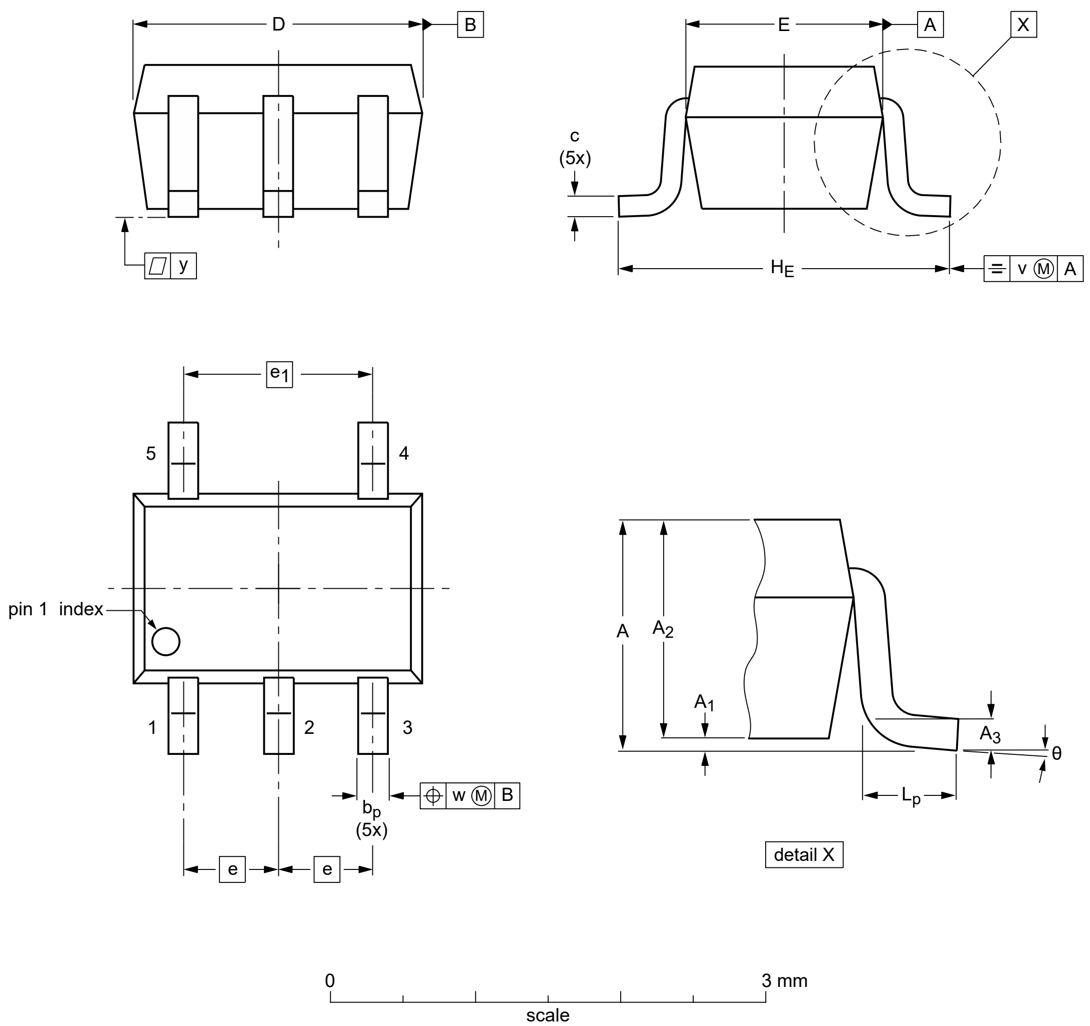
Table 10. Test data

Supply voltage	Input			Load		V_{EXT}		
V_{CC}	V_I	Δt/ΔV [1]	f_{max}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.8 V	V_{CC}	≤ 1.0 ns/V	15 MHz	15 pF, 30 pF	1 kΩ	open	GND	V_{CC}
2.5 V	V_{CC}	≤ 1.0 ns/V	25 MHz	15 pF, 30 pF	1 kΩ	open	GND	V_{CC}
3.3 V	3 V	≤ 1.0 ns/V	50 MHz	15 pF, 30 pF	1 kΩ	open	GND	V_{CC}
5.0 V	3 V	≤ 1.0 ns/V	50 MHz	15 pF, 30 pF	1 kΩ	open	GND	V_{CC}

[1] dV/dt ≥ 1.0 V/ns

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot353-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 7. Package outline SOT353-1 (TSSOP5)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV1T04_Q100 v.2	20220207	Product data sheet	-	74LV1T04_Q100 v.1
Modifications	Fig. 7: Package outline drawing for SOT353-1 has changed.			
74LV1T04_Q100 v.1	20200717	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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