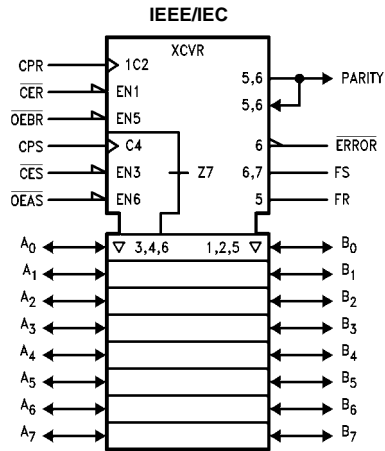
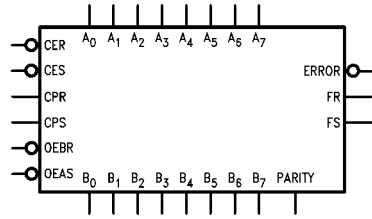


Logic Symbols



Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
A ₀ -A ₇	A-to-B Port Data Inputs or B-to-A 3-STATE	3.5/1.083 150/40 (33.3)	70 μA/-0.65 mA -3 mA/24 mA (20 mA)
B ₀ -B ₇	B-to-A Transceiver Inputs or A-to-B 3-STATE Output	3.5/1.083 600/106.6 (80)	70 μA/-0.65 mA -12 mA/64 mA (48 mA)
FR	B Port Flag Output	50/33.3	-1 mA/20 mA
FS	A Port Flag Output	50/33.3	-1 mA/20 mA
PARITY	Parity Bit Transceiver Input or Output	3.5/1.083 600/106.6 (50)	70 μA/-0.65 mA -12 mA/64 mA (48 mA)
$\overline{\text{ERROR}}$	Parity Check Output (Active LOW)	50/33.3	-1 mA/20 mA
$\overline{\text{CER}}$	R Registers Clock Enable Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA
$\overline{\text{CES}}$	S Registers Clock Enable Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA
CPR	R Registers Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/-0.6 mA
CPS	S Registers Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/-0.6 mA
$\overline{\text{OEBR}}$	B Port and PARITY Output Enable (Active LOW) and Clear FR Input (Active Rising Edge)	1.0/2.0	20 μA/-1.2 mA
$\overline{\text{OEAS}}$	A Port Output Enable (Active LOW) and Clear FS Input (Active Rising Edge)	1.0/2.0	20 μA/-1.2 mA

Functional Description

Data applied to the A-inputs are entered and stored in the R register on the rising edge of the CPR Clock Pulse, provided that the Clock Enable ($\overline{\text{CER}}$) is LOW; simultaneously, the status flip-flop is set and the flag (FR) output goes HIGH. As the Clock Enable ($\overline{\text{CER}}$) returns to HIGH, the data will be held in the R register. These data entered from the A-inputs will appear at the B Port I/O pins after the Output Enable ($\overline{\text{OEBR}}$) has gone LOW. When $\overline{\text{OEBR}}$ is LOW, a parity bit appears at the PARITY pin, which will be set HIGH when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR by changing the signal at the $\overline{\text{OEBR}}$ pin from LOW-to-HIGH.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A LOW at the $\overline{\text{CES}}$ pin and a LOW-to-HIGH transition at CPS pin enters the B-input data and the parity-input data into the S registers and the parity register respectively and set the flag output FS to HIGH. A LOW signal at the $\overline{\text{OEAS}}$ pin enables the A Port I/O pins and a LOW-to-HIGH transition of the $\overline{\text{OEAS}}$ signal clears the FS flag. When $\overline{\text{OEAS}}$ is LOW, the parity check output ERROR will be HIGH if there is an odd number of 1s at the Q outputs of the S registers and the parity register. The flag FS can be cleared by a LOW-to-HIGH transition of the $\overline{\text{OEAS}}$ signal.

Register Function Table

(Applies to R or S Register)

Inputs			Internal Q	Function
D	CP	$\overline{\text{CE}}$		
X	X	H	NC	Hold Data
L	↗	L	L	Load Data
H	↗	L	H	
X	↑	L	NC	Keep Old Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

↗ = LOW-to-HIGH Transition
↑ = Not LOW-to-HIGH Transition
NC = No Change

Flag Flip-Flop Function Table

(Applies to R or S Flag Flip-Flop)

Inputs			Flag Output	Function
$\overline{\text{CE}}$	CP	$\overline{\text{OE}}$		
H	X	↑	NC	Hold Flag
L	↗	↑	H	Set Flag
X	X	↗	L	Clear Flag

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

↗ = LOW-to-HIGH Transition
↑ = Not LOW-to-HIGH Transition
NC = No Change

Output Control

$\overline{\text{OE}}$	Internal Q	A or B Outputs	Function
H	X	Z	Disable Output
L	L	L	Enable Output
L	H	H	Enable Output

H = HIGH Voltage Level
L = LOW Voltage Level

X = Immaterial
Z = High Impedance

Parity Generation Function

$\overline{\text{OEBR}}$	Number of HIGHS in the Q Outputs of the R Register	Parity Output
H	X	Z
L	0, 2, 4, 6, 8	H
L	1, 3, 5, 7	L

H = HIGH Voltage Level
L = LOW Voltage Level

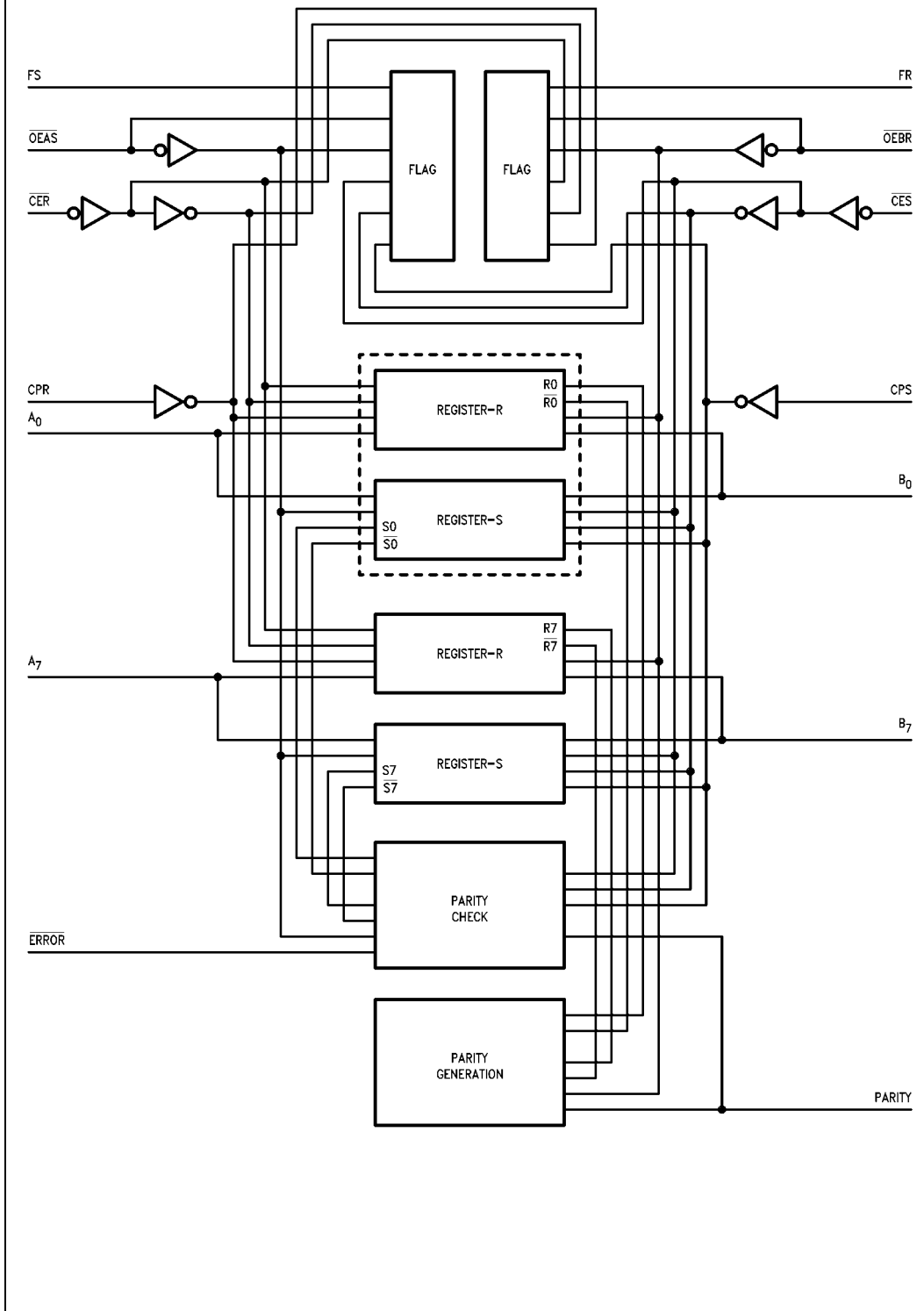
X = Immaterial
Z = High Impedance

Parity Check Function

$\overline{\text{OEAS}}$	Number of HIGHS in the Q Outputs of the S Register	Parity Input	ERROR Output
H	X	X	H
L	0, 2, 4, 6, 8	L	L
L	1, 3, 5, 7	L	H
L	0, 2, 4, 6, 8	H	H
L	1, 3, 5, 7	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

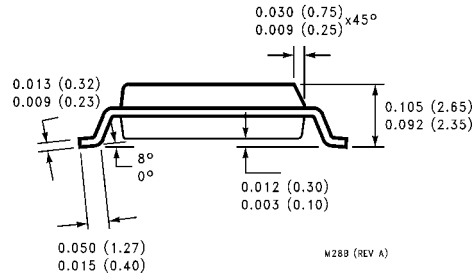
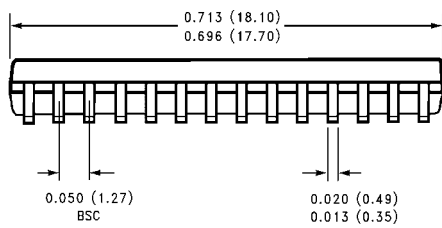
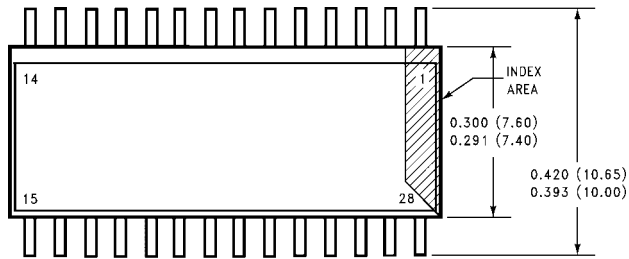
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA ($\overline{\text{CER}}$, $\overline{\text{CES}}$, CPR, CPS, $\overline{\text{OEBR}}$, $\overline{\text{OEAS}}$)
V _{OH}	Output HIGH Voltage	10% V _{CC} 2.5 10% V _{CC} 2.4 10% V _{CC} 2.0 5% V _{CC} 2.7 5% V _{CC} 2.7			V	Min	I _{OH} = -1 mA (FR, FS, $\overline{\text{ERROR}}$, A _n) I _{OH} = -3 mA (A _n , B _n PARITY) I _{OH} = -15 mA (B _n , PARITY) I _{OH} = -1 mA (FR, FS, $\overline{\text{ERROR}}$, A _n) I _{OH} = -3 mA (A _n , B _n , PARITY)
V _{OL}	Output LOW Voltage	10% V _{CC} 10% V _{CC} 10% V _{CC}		0.5 0.5 0.55	V	Min	I _{OL} = 20 mA (FR, FS, $\overline{\text{ERROR}}$) I _{OL} = 24 mA (A _n) I _{OL} = 64 mA (B _n , PARITY)
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V ($\overline{\text{CER}}$, $\overline{\text{CES}}$, CPR, CPS, $\overline{\text{OEBR}}$, $\overline{\text{OEAS}}$)
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V ($\overline{\text{CER}}$, $\overline{\text{CES}}$, CPR, CPS, $\overline{\text{OEBR}}$, $\overline{\text{OEAS}}$)
I _{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V _{IN} = 5.5V (A _n , B _n , PARITY)
I _{CEx}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC} (FR, FS, $\overline{\text{ERROR}}$, A _n , B _n , PARITY)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All other pins grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All other pins grounded
I _{IL}	Input LOW Current			-0.6 -1.2	mA	Max	V _{IN} = 0.5V ($\overline{\text{CER}}$, $\overline{\text{CES}}$, CPR, CPS) V _{IN} = 0.5V ($\overline{\text{OEBR}}$, $\overline{\text{OEAS}}$)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (A _n , B _n , PARITY)
I _{IL} + I _{OZL}	Output Leakage Current			-650	μA	Max	V _{OUT} = 0.5V (A _n , B _n , PARITY)
I _{OS}	Output Short-Circuit Current	-60 -100		-175 -250	mA	Max	V _{OUT} = 0V (FR, FS, $\overline{\text{ERROR}}$, A _n) V _{OUT} = 0V (B _n , PARITY)
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V (A _n , B _n , PARITY)
I _{CC} H	Power Supply Current		100	150	mA	Max	V _O = HIGH
I _{CC} L	Power Supply Current		100	150	mA	Max	V _O = LOW
I _{CC} Z	Power Supply Current		110	165	mA	Max	V _O = HIGH Z

AC Electrical Characteristics							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	3.5	6.0	8.0	3.0	9.0	ns
t _{PHL}	CPS or CPR to A _n or B _n	4.0	7.0	9.5	3.5	10.5	
t _{PLH}	Propagation Delay	3.0	5.5	7.5	2.5	8.5	ns
t _{PHL}	Propagation Delay	3.5	6.0	8.0	3.0	9.0	ns
t _{PLH}	Propagation Delay	8.0	14.0	18.0	7.0	20.0	ns
t _{PHL}	CPR to Parity	8.5	14.5	18.5	7.5	20.5	
t _{PLH}	Propagation Delay	8.0	13.5	17.5	7.0	19.5	ns
t _{PHL}	CPS to ERROR	7.5	13.0	16.5	6.5	18.5	
t _{PLH}	Propagation Delay	3.5	6.0	8.0	3.0	9.0	ns
t _{PHL}	OEAS to ERROR	3.0	5.0	7.0	2.5	8.0	
t _{PZH}	Enable Time OEAS	3.0	5.5	7.5	2.5	8.5	ns
t _{PZL}	or OEBR to B _n or A _n	3.5	7.0	9.5	3.0	10.5	
t _{PHZ}	Disable Time OEAS	3.0	6.5	8.5	2.5	9.5	ns
t _{PLZ}	or OEBR to B _n or A _n	3.0	5.5	7.5	2.5	8.5	
t _{PZH}	Enable Time	3.0	4.5	7.5	2.5	8.5	ns
t _{PZL}	OEBR to Parity	3.5	6.0	9.5	3.0	10.5	
t _{PHZ}	Disable Time	3.0	5.5	8.5	2.5	9.5	ns
t _{PLZ}	OEBR to Parity	3.0	6.5	7.5	2.5	8.5	

AC Operating Requirements						
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	7.5		8.5		ns
t _S (L)	A _n or B _n or Parity to CPS or CPR	4.5		5.0		
t _H (H)	Hold Time, HIGH or LOW	0		0		ns
t _H (L)	A _n or B _n or Parity to CPS or CPR	0		0		
t _S (H)	Setup, Time HIGH or LOW	6.0		7.0		ns
t _S (L)	CES or CER to CPS or CPR	10.0		11.5		
t _H (H)	Hold Time, HIGH or LOW	0		0		ns
t _H (L)	CES or CER to CPS or CPR	0		0		
t _W (H)	Pulse Width, HIGH or LOW	4.0		4.5		ns
t _W (L)	CPS or CPR	6.0		7.0		

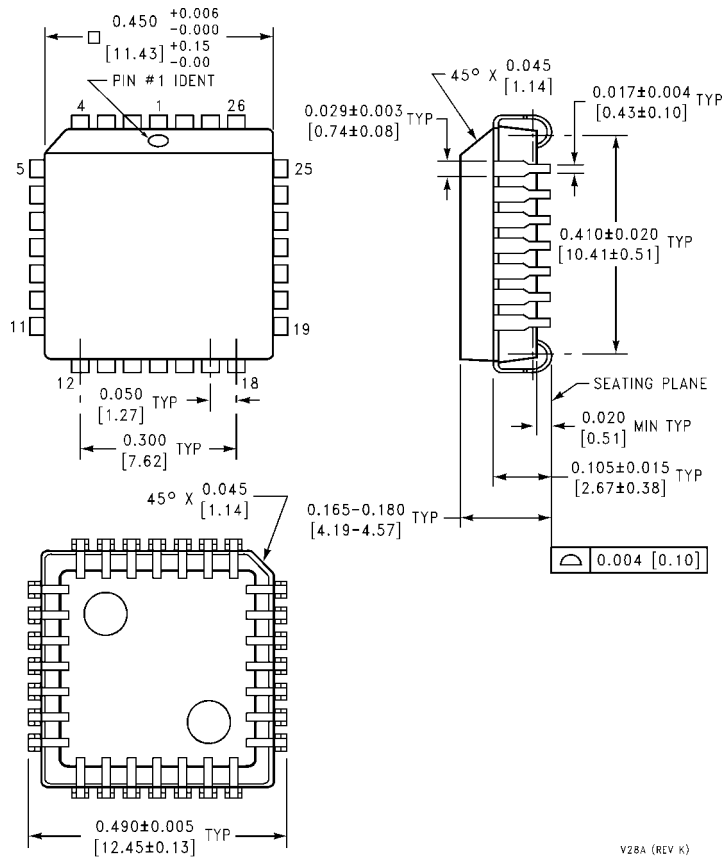
Physical Dimensions inches (millimeters) unless otherwise noted



M289 (REV A)

**28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M28B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A

V28A (REV K)

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