NXP's AUP1Z04 Demo board

Low-power crystal driver with enable and internal bias resistor

The 74AUP1Z04 combines the functions of the 74AUP1GU04 and 74AUP1G04 with enable circuitry and an internal bias resistor to provide a device optimized for use in crystal oscillator applications.

When not in use the $\overline{EN}$ input can be driven HIGH, pulling up the X1 input and putting the device in a low power disable mode. Schmitt trigger action at the $\overline{EN}$ input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} at output Y. The I_{OFF} circuitry disables the output Y, preventing the damaging backflow current through the device when it is powered down. The integration of the two devices into the 74AUP1Z04 produces the benefits of a compact footprint, lower power dissipation and stable operation over a wide range of frequency and temperature.

Key Features and Benefits

- Low power crystal driver with integrated output enable function to save power
- The integrated bias resistor provides negative feedback and sets a bias point of inverter near mid-supply, eliminating the need of external resister
- Stable operation over wide range of supply voltage, frequency and temperature
- I_{OFF} circuitry provides partial power-down mode operation at output Y
- Over supply voltage tolerant inputs up to 3.6V
- Demo board is available which can be optimized for different system loads and evaluate the part under different test conditions
- Very small footprint and availability in leadless MicroPak packages

NXP founded by Philips

Key Features and Benefits

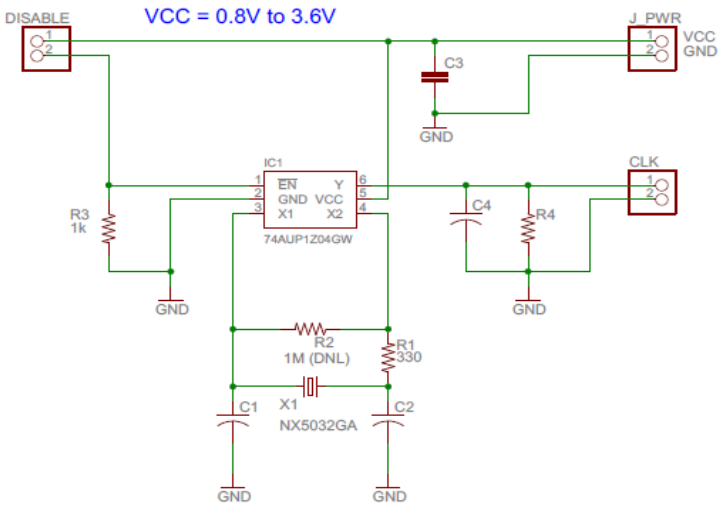
- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Low noise overshoot and undershoot < 10 % of V_{CC}
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

Schematics of AUP1Z04 demo board are shown in figure below. A supply voltage of 0.8V to 3.6V can be used for the board. Values of C1 and C2 are calculated so that a parallel combination of C1 and C2 is equal to recommended load capacitance of crystal (C_L), specified in the crystal data sheet. Crystal with different frequencies can be used on the board with out changing C1 and C2, as long as the load capacitance and foot print are same. Reference board uses a 25MHz crystal (NX5032GA) from NDK with 8pF load capacitance. NX5032GA is also available in same foot print (5mm x 3.2mm) and 8pF load capacitance in frequency range of 8MHz to 25MHz.

$$C_L = \frac{C1 \times C2}{(C1 + C2)}$$

R1 isolates the output of the inverter from the crystal and prevents spurious high-frequency oscillation, so that a clean waveform can be obtained. The optimum value of R1 depends on the frequency of operation and the required stability. The minimum value of R1 depends on the recommended power consumption of the crystal. Crystal manufacturers usually specify a recommended value of R1 in the crystal data sheet.

Using a R1 value lower than that in the crystal data sheet may cause overdriving of the crystal and result in damage to the crystal or shorten the crystal life.



Demo board circuit schematics

Acceptable results can be accomplished by choosing the value to be approximately equal to the capacitive reactance, i.e., $R1 = X_{C2}$, provided X_{C2} is greater than or equal to the manufacturer's recommended value.

R1 and C2 form a low-pass filter and reduce spurious oscillation. The value can be adjusted, based on the desired cutoff frequency. Another factor in choosing C2 is the start-up time. For a low-gain amplifier, sometimes C2 is increased over C1 to increase the phase-shift and help in start-up, but C1 should be within a limit such that the load capacitance introduced to the crystal does not exceed the manufacturer's recommended value of C_L. Values of R4 and C4 can be adjusted to see the effect of different loads on edge rate and shape of output clock. $\overline{EN}$ pin is normally pulled down by R3, when jumper 'DISABLE' is open. When the 'DISABLE' jumper is closed, $\overline{EN}$ pin is pulled up to Vcc and clock output is turned off. Value of R3 can be increased or decreased to control the enable and disable time of output clock. With lower R3, clock can be enabled and disabled faster and vice versa.

Test Results

Fig. 1 shows the output of 25MHz crystal at a supply voltage of 3.3V. Fig. 2 shows the output at pin 'Y' when clock is enabled i.e. DISABLE jumper is open. Fig. 3 shows the output waveform at 1.8V supply, when clock is enabled. Load used for testing is R4= 1M Ohms and C4 = 6 pF. Sinusoidal waveform of crystal is converted into a square wave by using the buffered inverter channel of AUP1Z04. Fig. 4 shows the output, when clock is disabled i.e. DISABLE jumper is closed and $\overline{EN}$ pin is pulled up to Vcc.

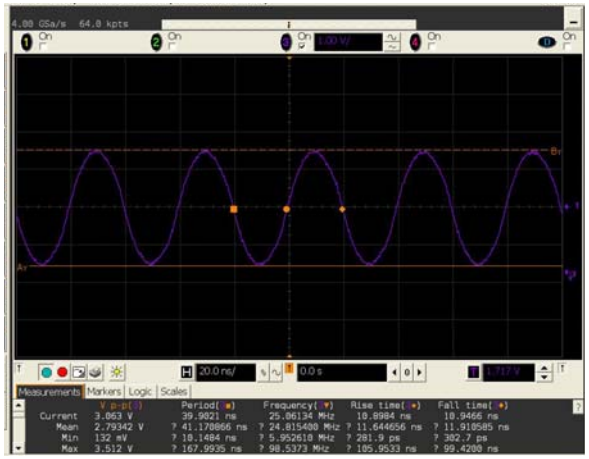


Fig. 1

Fig. 2

Fig. 3

Fig. 4

Packages

74AUP1Z04 is available in 6 pin SC88, and leadless XSON packages.

Package suffix	GW	GM	GF
	 SOT 363	 SOT 886	 SOT 891
	6-pin	6-pin	6-pin
Width (mm)	2.1	1	1
Length (mm)	2	1.45	1
Pitch (mm)	0.65	0.5	0.35

Ordering Information

Part Number	**Package**				
	Temp. Range	Name	Type	Marking	Material
74AUP1Z04GW	-40C to 125C	SC-88	Surface Mount	a4	Plastic
74AUP1Z04GM	-40C to 125C	XSON6	Thin Small Outline; no leads	a4	Plastic
74AUP1Z04GF	-40C to 125C	XSON6	Thin Small Outline; no leads	a4	Plastic

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