

N- and P-Channel 60-V (D-S) MOSFET

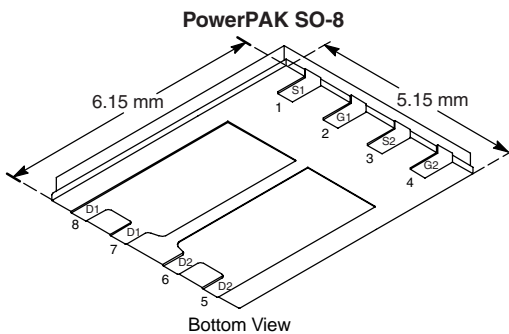
PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
N-Ch	60	0.075 at V _{GS} = 10 V	4.6	12 nC
		0.100 at V _{GS} = 4.5 V	4.0	
P-Ch	- 60	0.064 at V _{GS} = - 10 V	- 5.0	47
		0.080 at V _{GS} = - 4.5 V	- 4.5	

FEATURES

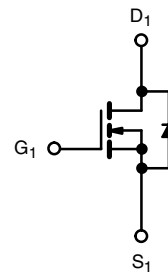
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- 100 % R_g Tested



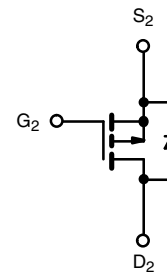
RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si7530DP-T1-E3 (Lead (Pb)-free)
Si7530DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		10 s	Steady	10 s	Steady		
Drain-Source Voltage	V _{DS}	60		- 60		V	
Gate-Source Voltage	V _{GS}	± 20					
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25°C	4.6	3.0	- 5.0	- 3.2	A
		T _A = 70°C	3.6	2.4	- 4.0	- 2.6	
Pulsed Drain Current	I _{DM}	15		- 25		A	
Continuous Source Current (Diode Conduction) ^a	I _S	2.7	1.2	- 2.9	- 1.2		
Single Pulse Avalanche Current	I _{AS}	15		- 22		mJ	
Single Pulse Repetitive Avalanche Energy ^b	E _{AS}	11		24.2			
Maximum Power Dissipation ^a	P _D	T _A = 25°C	3.3	1.4	3.5	1.5	W
		T _A = 70°C	2.1	0.9	2.2	0.94	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150				°C	
Soldering Recommendations (Peak Temperature) ^{c, d}		260					

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typical	Maximum	Typical	Maximum		
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	29	38	27	36	°C/W
		Steady State	60	85	60	85	
Maximum Junction-to-Case (Drain)	R _{thJC}	4.0	5.2	3.3	4.3		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Duty Cycle ≤ 1 %.

c. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

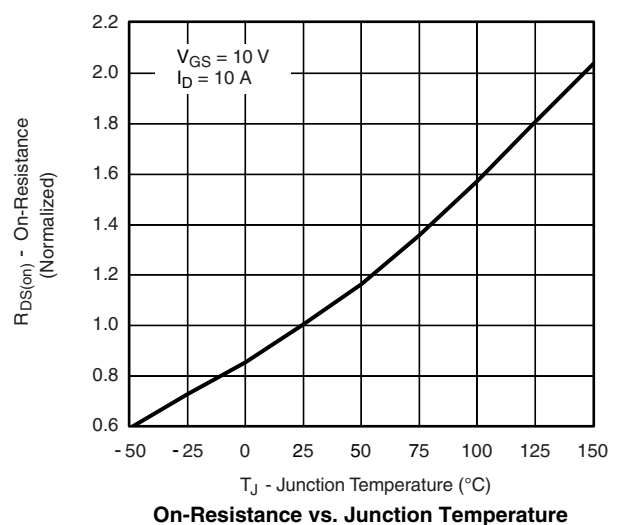
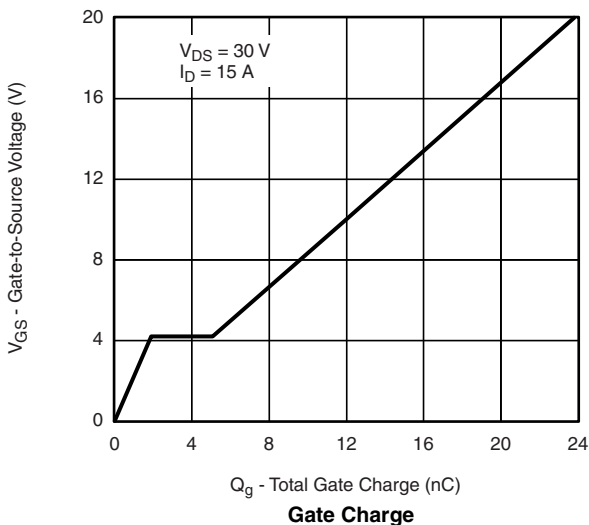
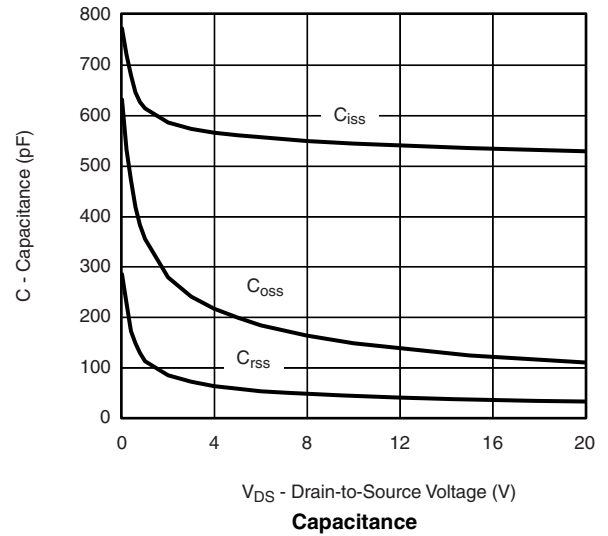
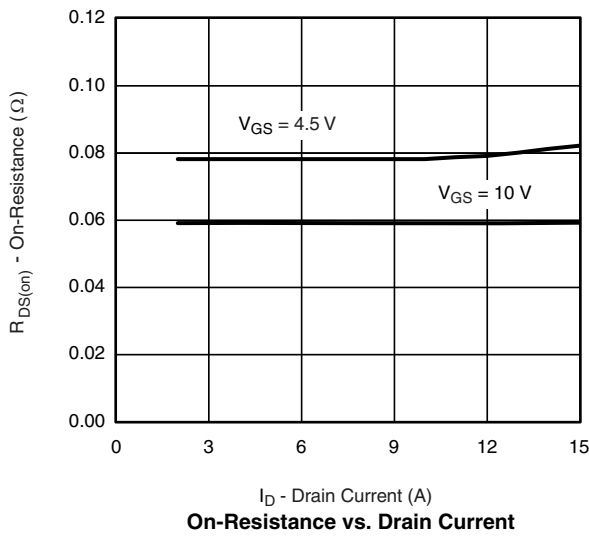
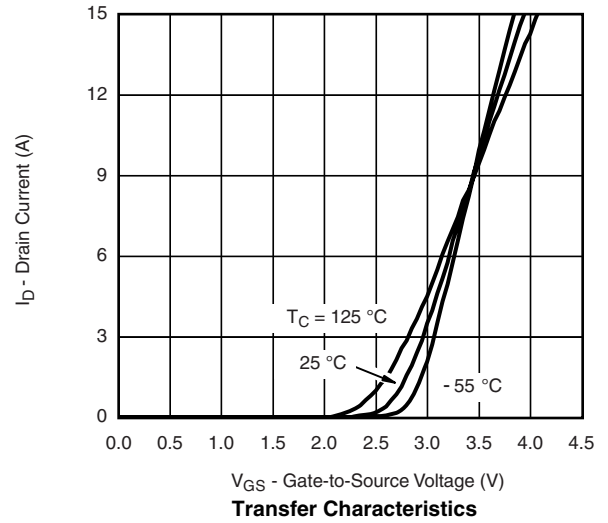
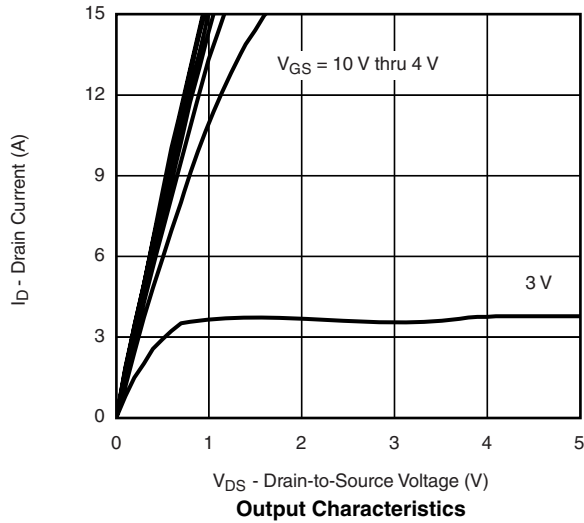
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	N-Ch	1		3	V
		$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	P-Ch	-1		-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$	N-Ch P-Ch			± 100 ± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\ \text{V}, V_{GS} = 0\ \text{V}$	N-Ch			1	μA
		$V_{DS} = -60\ \text{V}, V_{GS} = 0\ \text{V}$	P-Ch			-1	
		$V_{DS} = 60\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$	N-Ch			5	
		$V_{DS} = -60\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$	P-Ch			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	N-Ch	15			A
		$V_{DS} \leq -5\ \text{V}, V_{GS} = -10\ \text{V}$	P-Ch	-25			
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 4.6\ \text{A}$	N-Ch		0.060	0.075	Ω
		$V_{GS} = -10\ \text{V}, I_D = -5.0\ \text{A}$	P-Ch		0.051	0.064	
		$V_{GS} = 4.5\ \text{V}, I_D = 4.0\ \text{A}$	N-Ch		0.080	0.100	
		$V_{GS} = -4.5\ \text{V}, I_D = -4.5\ \text{A}$	P-Ch		0.064	0.080	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 4.6\ \text{A}$	N-Ch		6		S
		$V_{DS} = -15\ \text{V}, I_D = -5.0\ \text{A}$	P-Ch		16		
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.7\ \text{A}, V_{GS} = 0\ \text{V}$	N-Ch		0.85	1.2	V
		$I_S = -2.9\ \text{A}, V_{GS} = 0\ \text{V}$	P-Ch		-0.85	-1.2	
Dynamic^b							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 30\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 15\ \text{A}$	N-Ch		12	20	nC
Gate-Source Charge	Q_{gs}		P-Ch		26	40	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -30\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -5.0\ \text{A}$	N-Ch		2		nC
			P-Ch		4.5		
Gate Resistance	R_g	$f = 1.0\ \text{MHz}$	N-Ch	0.6	1.5	2.5	Ω
			P-Ch	3.5	7	11	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 30\ \text{V}, R_L = 30\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_g = 6\ \Omega$	N-Ch		7	15	ns
Rise Time	t_r		P-Ch		8	15	
		Turn-Off Delay Time	$t_{d(off)}$	N-Ch		8	
P-Ch				9	15		
Fall Time	t_f	P-Channel $V_{DD} = -30\ \text{V}, R_L = 30\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_g = 6\ \Omega$	N-Ch		15	25	
			P-Ch		65	100	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.7\ \text{A}, dI/dt = 100\ \text{A}/\mu\text{s}$	N-Ch		30	60	pC
		$I_F = -5\ \text{A}, dI/dt = 100\ \text{A}/\mu\text{s}$	P-Ch		40	80	
Reverse Recovery Energy	Q_{rr}	$I_F = 2.7\ \text{A}, dI/dt = 100\ \text{A}/\mu\text{s}$	N-Ch		33	66	pC
		$I_F = -5\ \text{A}, dI/dt = 100\ \text{A}/\mu\text{s}$	P-Ch		57	115	

Notes:

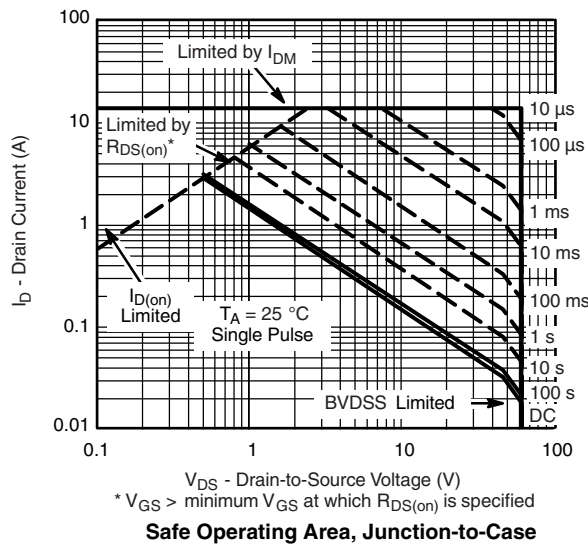
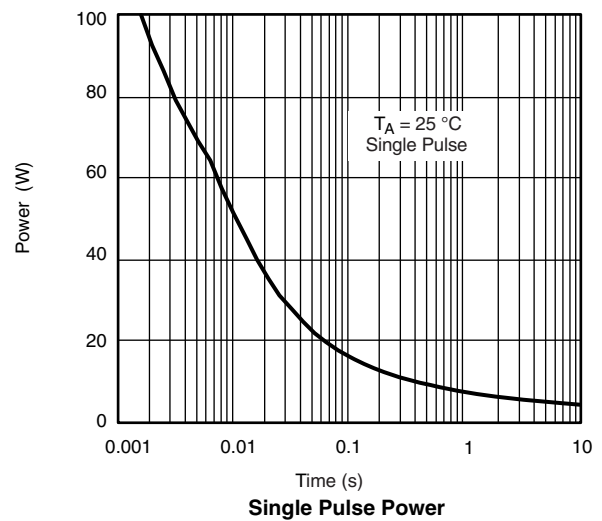
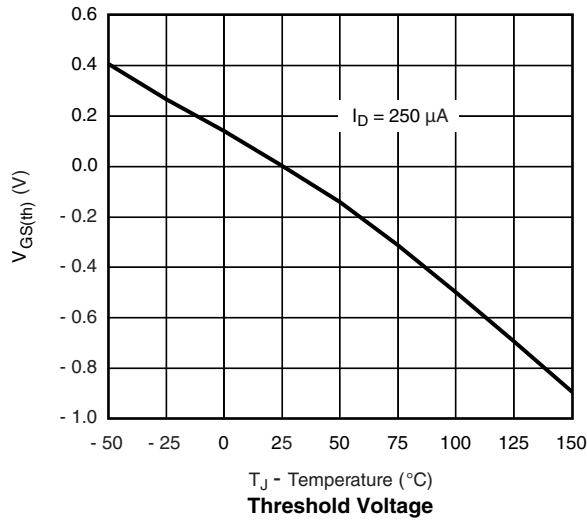
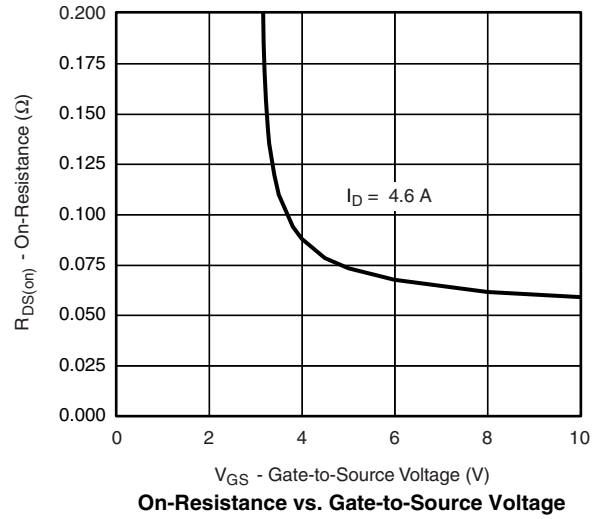
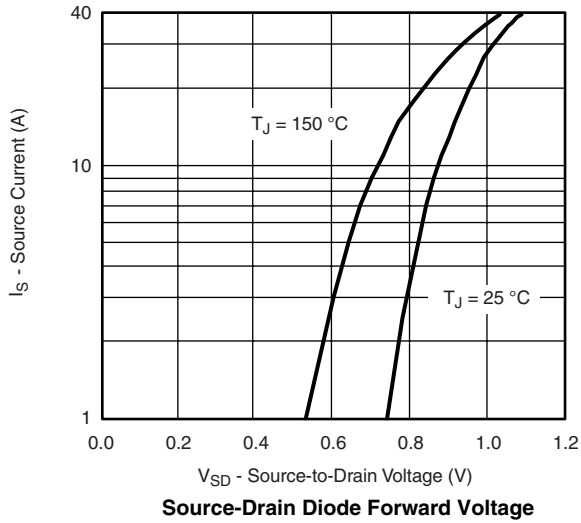
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

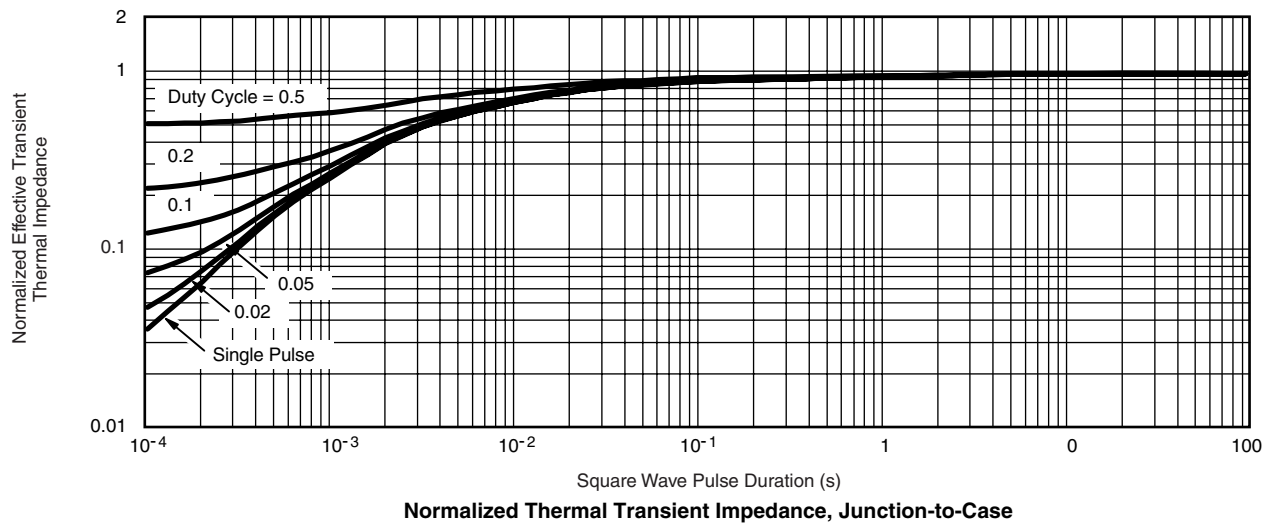
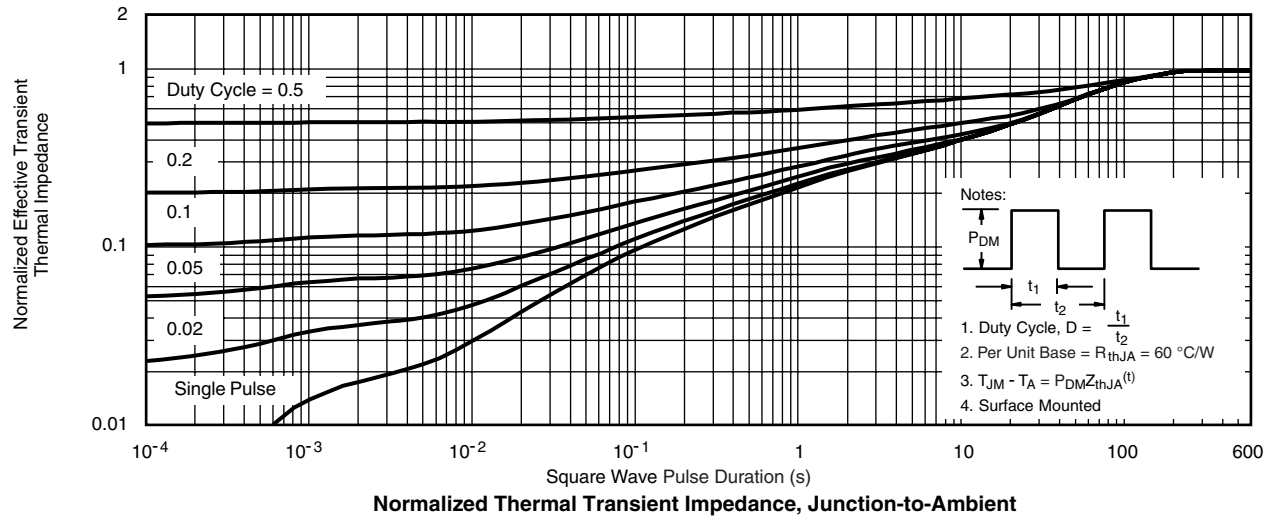
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



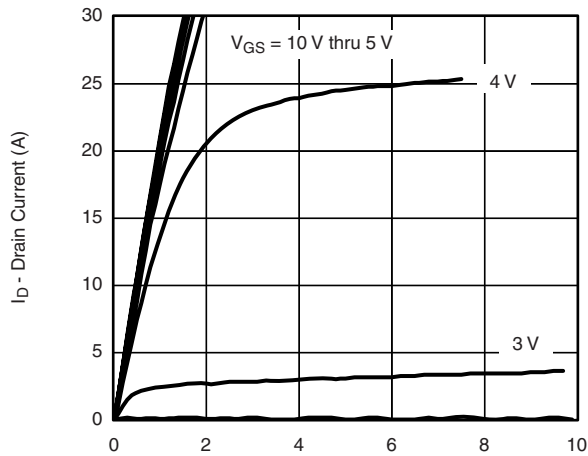
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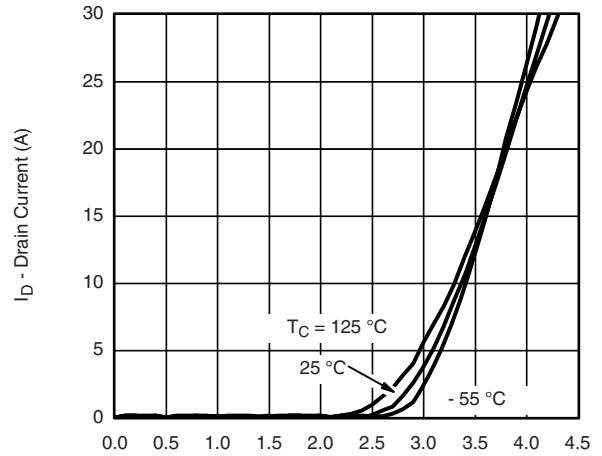
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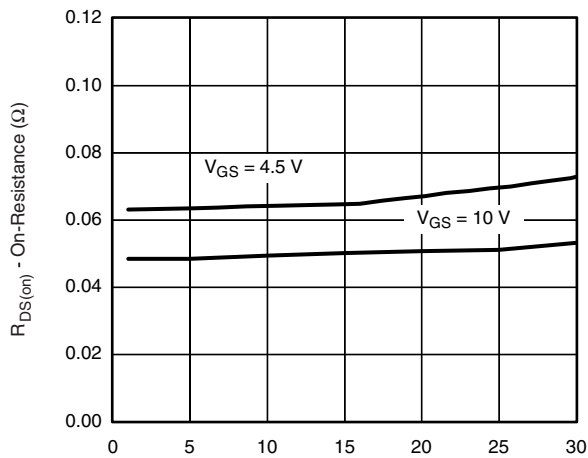
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



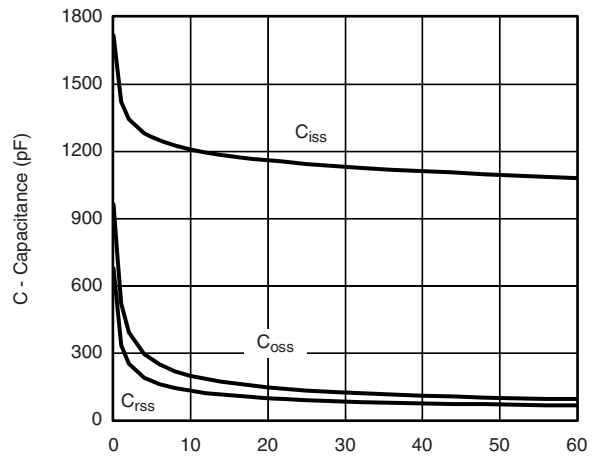
V_{DS} - Drain-to-Source Voltage (V)
Output Characteristics



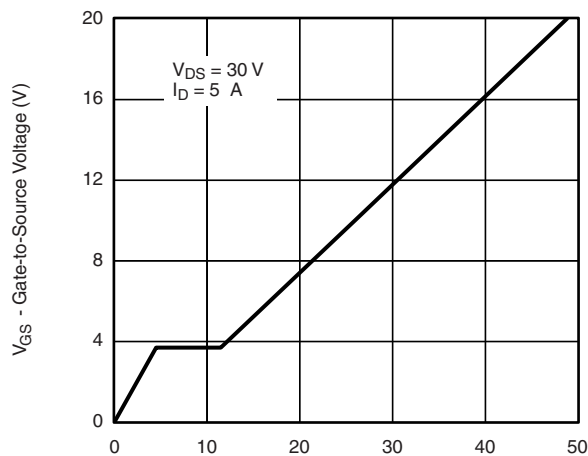
V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



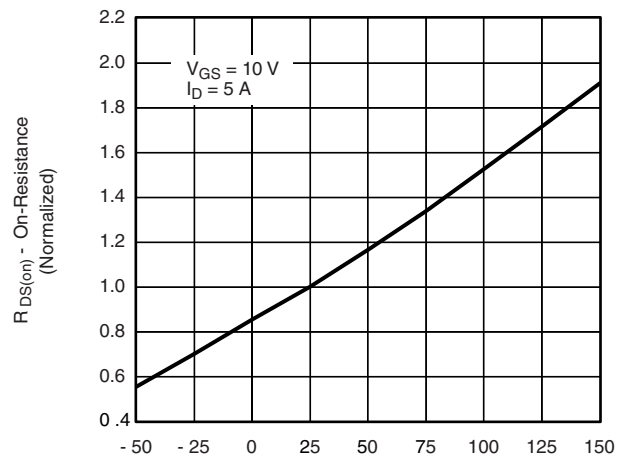
I_D - Drain Current (A)
On-Resistance vs. Drain Current



V_{DS} - Drain-to-Source Voltage (V)
Capacitance

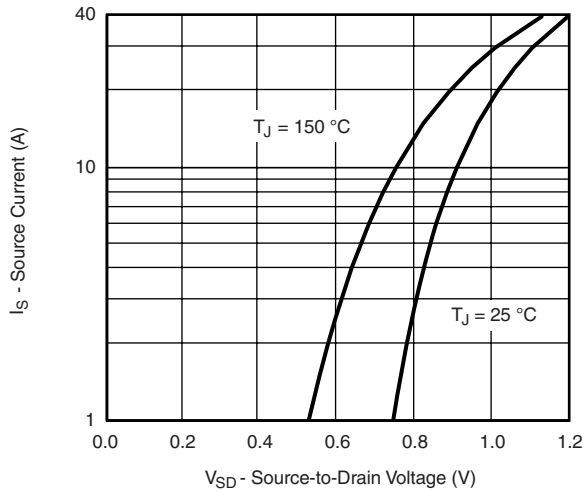


Q_g - Total Gate Charge (nC)
Gate Charge

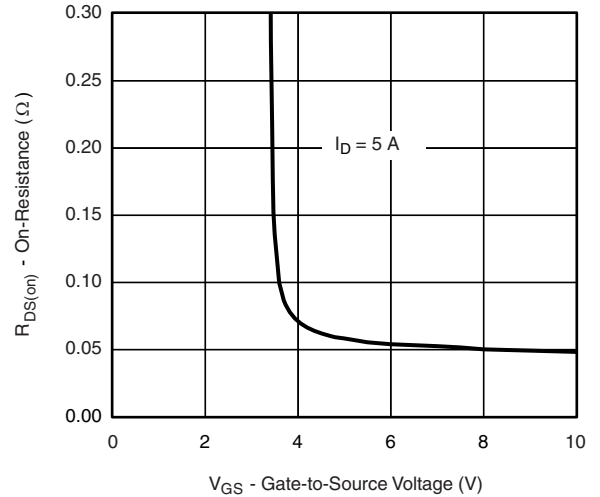


T_J - Junction Temperature ($^{\circ}\text{C}$)
On-Resistance vs. Junction Temperature

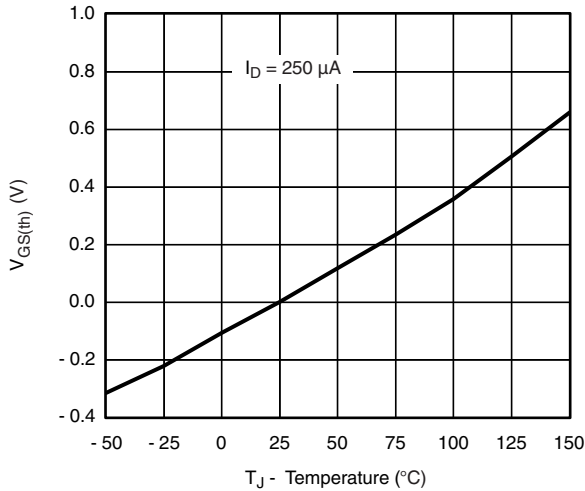
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



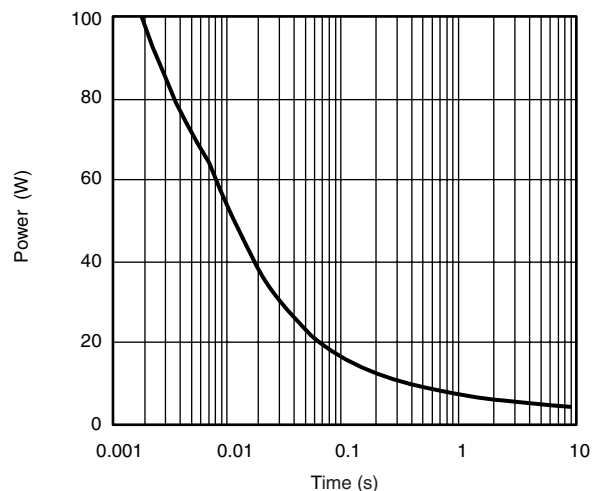
Source-Drain Diode Forward Voltage



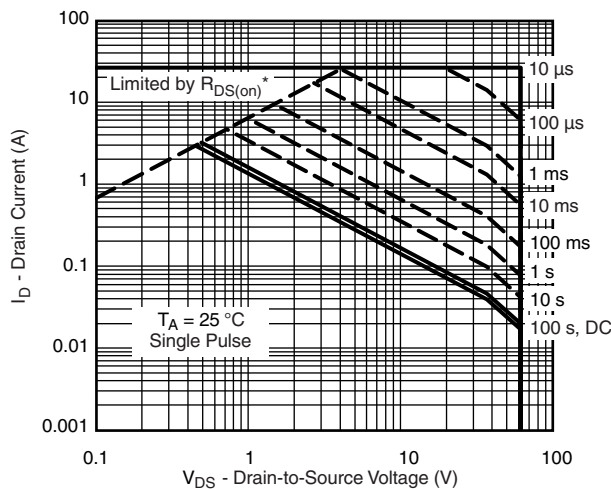
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



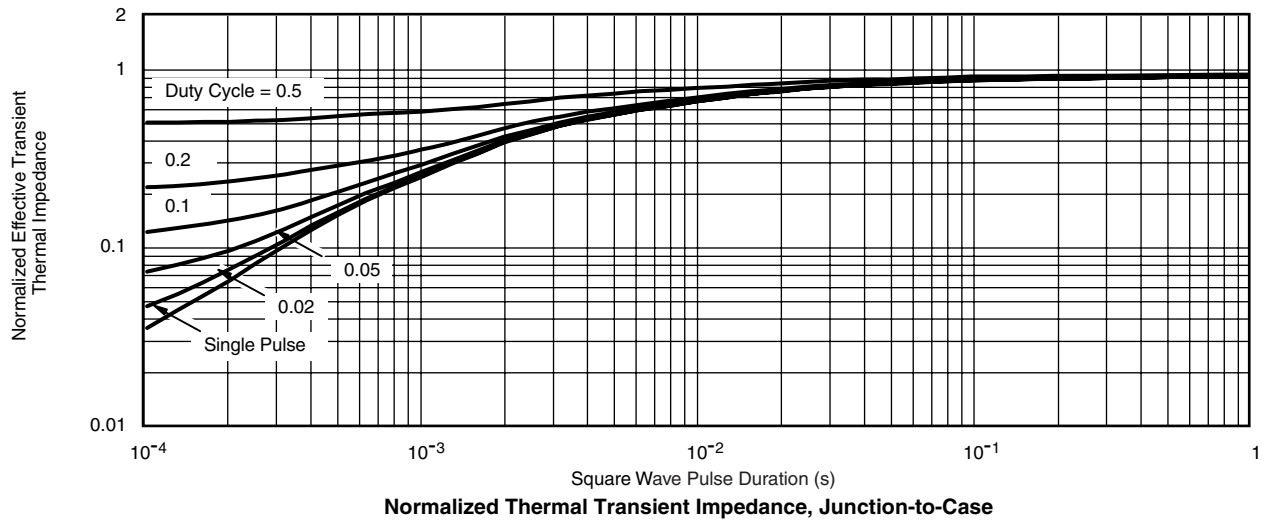
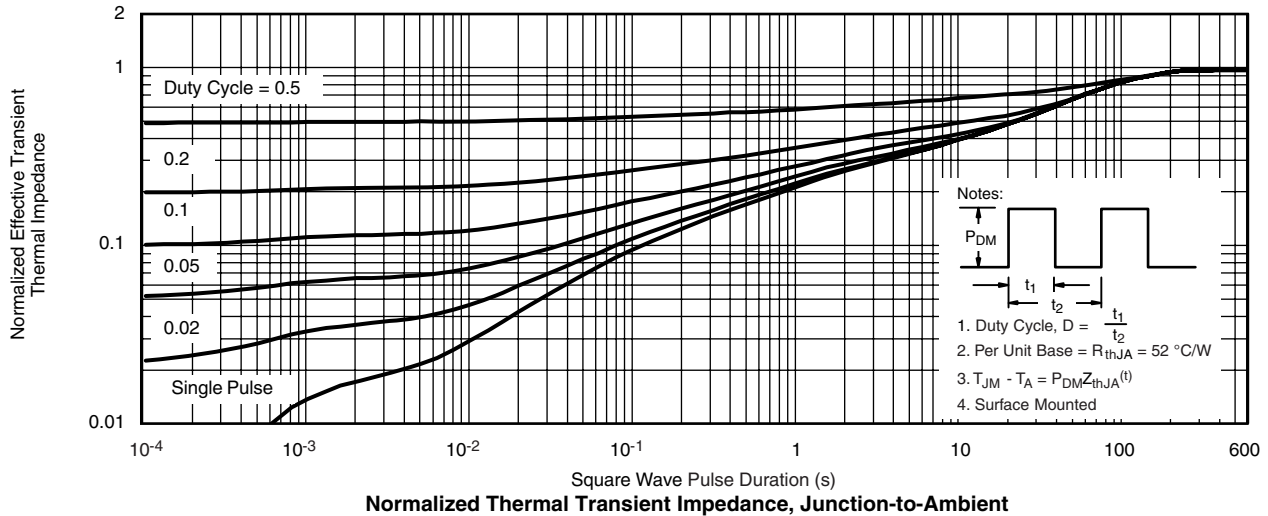
Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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