

RoHS

COMPLIANT HALOGEN

FREE

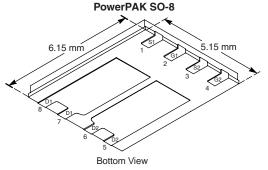
Vishay Siliconix

Dual N-Channel 40-V (D-S) MOSFET

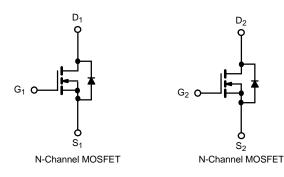
PRODUCT SUMMARY					
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)		
40	0.017 at V_{GS} = 10 V	11.1	46.2		

FEATURES

- Halogen-free According to IEC 61249-2-21
 Available
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK[®]
 Package
- Dual MOSFET for Space Savings
- 100 % R_g Tested
- High Threshold Voltage at High Temperature



Ordering Information: Si7962DP-T1-E3 (Lead (Pb)-free) Si7962DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	40		V
Gate-Source Voltage		V _{GS}	± 20		v
Continuous Drain Current (T 150 °C)ª	T _A = 25 °C	I _D	11.1	7.1	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		8.9	5.7	
Pulsed Drain Current		I _{DM}	40		А
Continuous Source Current (Diode Conduction) ^a		۱ _S	2.9	1.2	
Single Avalanche Current	L = 0.1 mH	I _{AS}	30		
Single Avalanche Energy	L = 0.1 min	E _{AS}	45		mJ
	T _A = 25 °C	Pa	3.5	1.4	W
Maximum Power Dissipation ^a	T _A = 70 °C		2.2	0.9	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}		0		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Mauina huratian ta Anchianta	t ≤ 10 s	R _{thJA}	26	35	
Maximum Junction-to-Ambient ^a	Steady State		60	85	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	2.2	2.7	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (<u>http://www.vishay.com/ppg?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			-				
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	3.4		4.5	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zara Cata Valtaga Drain Current	I _{DSS}	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current		V_{DS} = 40 V, V_{GS} = 0 V, T_{J} = 55 °C			5	μA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5$ V, $V_{GS} = 10$ V	30			Α	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 11.1 A		0.0135	0.017	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 11.1 A		31		S	
Diode Forward Voltage ^a	V _{SD}	$I_{\rm S}$ = 2.9 A, $V_{\rm GS}$ = 0 V		0.8	1.2	V	
Dynamic ^b							
Total Gate Charge	Qg			46.2	70	nC	
Gate-Source Charge	Q _{gs}	V_{DS} = 20 V, V_{GS} = 10 V, I_{D} = 11.1 A		1.6			
Gate-Drain Charge	Q _{gd}			9.6			
Gate Resistance	Rg	f = 1 MHz	1.1	2.3	3.5	Ω	
Turn-On Delay Time	t _{d(on)}			22	35		
Rise Time	t _r	V_{DD} = 20 V, R_L = 20 Ω		15	25	ns	
Turn-Off Delay Time	t _{d(off)}	$I_{D}\cong$ 1 A, V_{GEN} = 10 V, R_{g} = 6 Ω		55	70		
Fall Time	t _f			15	25		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.9 A, dl/dt = 100 A/μs		35	60		

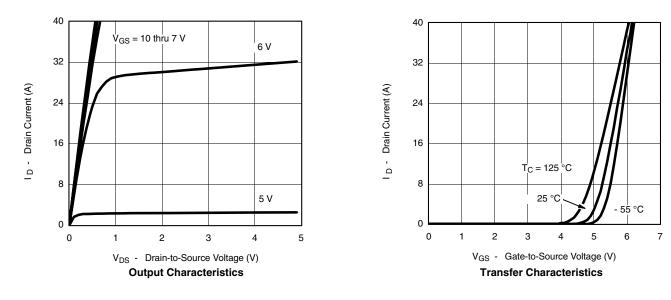
Notes:

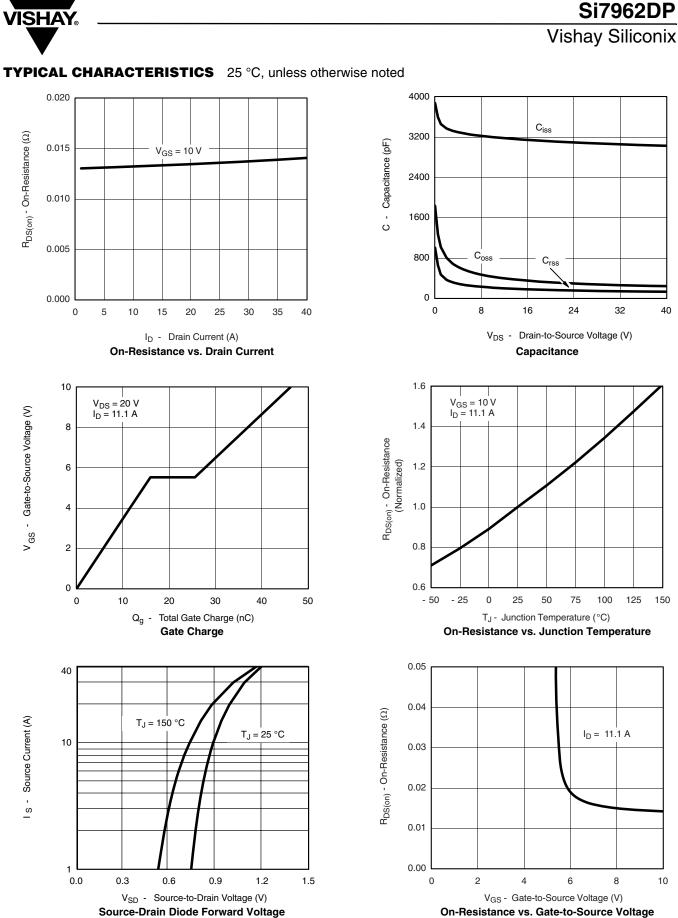
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



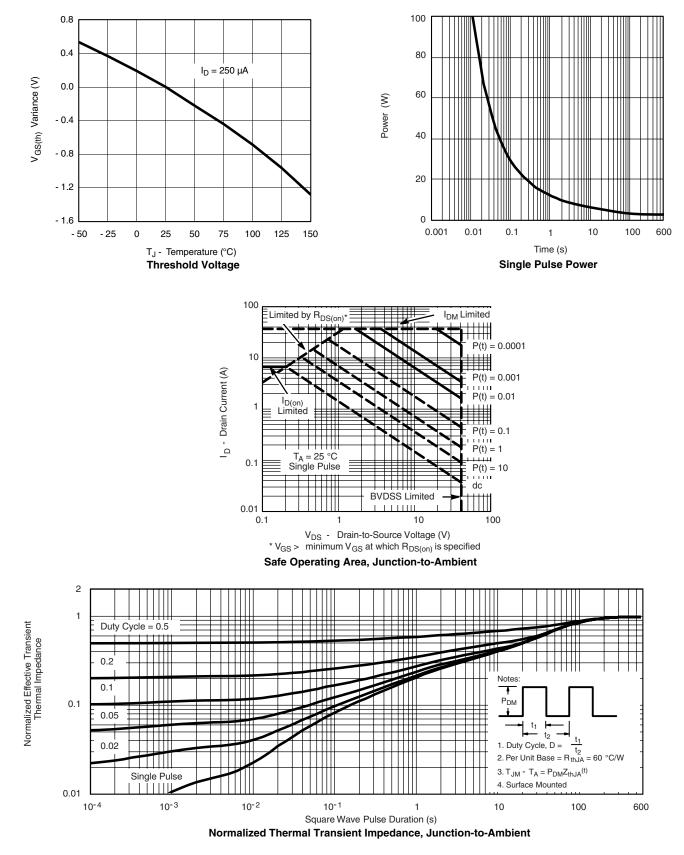


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Si7962DP

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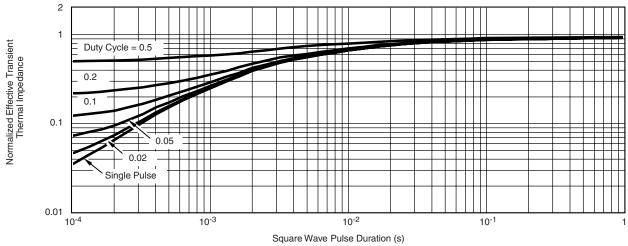




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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72914.



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