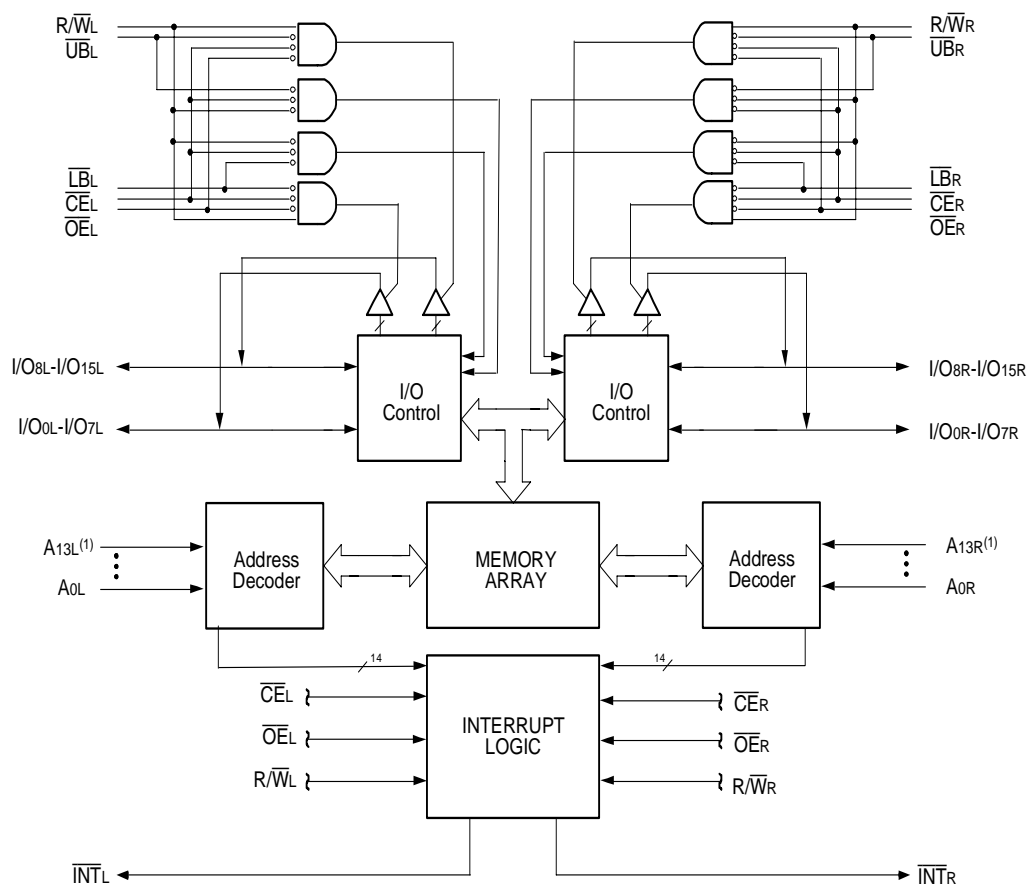


## Features

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - Industrial: 40/55ns (max.)
- Low-power operation
  - IDT70P264/254/244L
  - Active: 27mW (typ.)
  - Standby: 3.6μW (typ.)
- On-chip port interrupt logic which supports level shift output
- Fully asynchronous operation from either port
- Power supply isolation functionality to aid system power management
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- Left port is selectable 3.0V, 2.5V or 1.8V
- Right port is 1.8V I/O
- LVTTL-compatible, single 1.8V (±100mV) power supply
- Available in 81 Ball 0.5mm-pitch BGA
- Industrial temperature range (-40°C to +85°C)
- Green parts available, see ordering information

## Functional Block Diagram



7148 drw 01

### NOTE:

- A13x is a NC for IDT70P254. A13x and A12x are NC for IDT70P244.

## Description

The IDT70P264/254/244 is a very low power 16K/8K/4K x 16 Dual-Port Static RAM. The IDT70P264/254/244 is designed to be used as a stand-alone 256/128/64K-bit Dual-Port SRAM.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down

feature controlled by  $\overline{CE}$  permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 27mW of power.

The IDT70P264/254/244 is packaged in a 81 ball 0.5mm-pitch Ball Grid Array. The package is a 1mm thick and designed to fit in wireless handset applications.

## Pin Configurations

### 70P264/254/244BY BY-81

#### 81-Ball 0.5mm Pitch BGA Top View

	1	2	3	4	5	6	7	8	9	
A	A <sub>2R</sub>	A <sub>5R</sub>	A <sub>11R</sub>	$\overline{CE}_R$	V <sub>SS</sub>	I/O <sub>14R</sub>	I/O <sub>12R</sub>	I/O <sub>10R</sub>	I/O <sub>8R</sub>	A
B	A <sub>1R</sub>	A <sub>7R</sub>	A <sub>9R</sub>	A <sub>12R</sub> <sup>(1)</sup>	A <sub>13R</sub> <sup>(1)</sup>	I/O <sub>13R</sub>	I/O <sub>11R</sub>	V <sub>SS</sub>	I/O <sub>7R</sub>	B
C	A <sub>0R</sub>	A <sub>6R</sub>	A <sub>8R</sub>	A <sub>10R</sub>	R/ $\overline{W}_R$	I/O <sub>15R</sub>	V <sub>DD</sub>	I/O <sub>9R</sub>	I/O <sub>6R</sub>	C
D	$\overline{UB}_R$	A <sub>3R</sub>	A <sub>4R</sub>	$\overline{INT}_R$	$\overline{OE}_R$	I/O <sub>5R</sub>	I/O <sub>2R</sub>	I/O <sub>4R</sub>	I/O <sub>3R</sub>	D
E	V <sub>SS</sub>	$\overline{LB}_L$	$\overline{INT}_L$	$\overline{LB}_R$	V <sub>DD</sub>	I/O <sub>13L</sub>	I/O <sub>15L</sub>	I/O <sub>0R</sub>	I/O <sub>1R</sub>	E
F	$\overline{UB}_L$	A <sub>4L</sub>	A <sub>2L</sub>	A <sub>3L</sub>	I/O <sub>3L</sub>	I/O <sub>5L</sub>	I/O <sub>12L</sub>	V <sub>DDQL</sub>	I/O <sub>14L</sub>	F
G	A <sub>0L</sub>	A <sub>1L</sub>	A <sub>11L</sub>	A <sub>12L</sub> <sup>(1)</sup>	$\overline{OE}_L$	I/O <sub>4L</sub>	I/O <sub>9L</sub>	I/O <sub>11L</sub>	I/O <sub>10L</sub>	G
H	A <sub>6L</sub>	A <sub>8L</sub>	A <sub>9L</sub>	A <sub>13L</sub> <sup>(1)</sup>	$\overline{CE}_L$	I/O <sub>0L</sub>	I/O <sub>2L</sub>	V <sub>SS</sub>	I/O <sub>8L</sub>	H
J	A <sub>5L</sub>	A <sub>7L</sub>	A <sub>10L</sub>	R/ $\overline{W}_L$	V <sub>SS</sub>	I/O <sub>1L</sub>	V <sub>DDQL</sub>	I/O <sub>6L</sub>	I/O <sub>7L</sub>	J
	1	2	3	4	5	6	7	8	9	

7148 drw 02

#### NOTE:

1. A<sub>13x</sub> is a NC for IDT70P254. A<sub>13x</sub> and A<sub>12x</sub> are NC for IDT70P244.

## Pin Names

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable (Input)
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable (Input)
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable (Input)
A0L - A13L <sup>(1)</sup>	A0R - A13R <sup>(1)</sup>	Address (Input)
I/O0L - I/O15L	I/O0R - I/O15R	Data Input/Output
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select (Input)
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select (Input)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag (Output)
VDD		Power for Core + Right Port I/O (1.8V) (Input)
VDDOL		Left Port I/O Supply Voltage (1.8V, 2.5V or 3.0V) (Input)
VSS		Ground (0V) (Input)

7148 tbl 01

### NOTE:

1. A13x is a NC for IDT70P254. A13x and A12x are NC for IDT70P244.

## Truth Table I: Non-Contention Read/Write Control

Inputs					Outputs		Mode
$\overline{CE}$	$R/\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O8-15	I/O0-7	
H	X	X	X	X	High-Z	High-Z	Deselected: Power Down
X	X	X	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	DATA <sub>IN</sub>	High-Z	Write to Upper Byte Only <sup>(1)</sup>
L	L	X	H	L	High-Z	DATA <sub>IN</sub>	Write to Lower Byte Only <sup>(1)</sup>
L	L	X	L	L	DATA <sub>IN</sub>	DATA <sub>IN</sub>	Write to Both Bytes <sup>(1)</sup>
L	H	L	L	H	DATA <sub>OUT</sub>	High-Z	Read Upper Byte Only
L	H	L	H	L	High-Z	DATA <sub>OUT</sub>	Read Lower Byte Only
L	H	L	L	L	DATA <sub>OUT</sub>	DATA <sub>OUT</sub>	Read Both Bytes
X	X	H	X	X	High-Z	High-Z	Outputs Disabled

7148 tbl 02

### NOTE:

1. A0L — A13L ≠ A0R — A13R

## Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Industrial	Unit
V <sub>TERM</sub>	Supply Voltage on V <sub>DD</sub> with Respect to GND	-0.5 to +2.9	V
V <sub>TERM</sub>	Supply Voltage on V <sub>DDQL</sub> with Respect to GND	-0.5 to +3.6	V
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>DD</sub> + 0.3 <sup>(4)</sup>	V
T <sub>BIAS</sub> <sup>(3)</sup>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>JN</sub>	Junction Temperature	+150	°C
I <sub>OUT</sub> (for V <sub>DDQL</sub> = 3.0V)	DC Output Current	20	mA
I <sub>OUT</sub> (for V <sub>DDQL</sub> = 2.5V)	DC Output Current	20	mA

7148 tbl 03

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period over V<sub>TERM</sub> = V<sub>DD</sub> + 0.3V.
- Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.
- V<sub>DDQL</sub> + 0.3V for left port.

## Capacitance

(T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	9	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 3dV	10	pF

7148 tbl 07

### NOTES:

- This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

## Maximum Operating Temperature and Supply Voltage<sup>(1)</sup>

Grade	Ambient Temperature	GND	V <sub>DD</sub>
Industrial	-40°C to +85°C	0V	1.8V ± 100mV

7148 tbl 04

### NOTE:

- This is the parameter T<sub>A</sub>. This is the "instant on" case temperature.

### Recommended DC Operating Conditions ( $V_{DDQL} = 3.0V \pm 300mV$ )

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	1.7	1.8	1.9	V
V <sub>DDQL</sub>	Left Port Supply Voltage	2.7	3.0	3.3	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IHL</sub>	Input High Voltage ( $V_{DDQL} = 3.0V$ )	2.0	—	$V_{DDQL} + 0.2$	V
V <sub>ILL</sub>	Input Low Voltage ( $V_{DDQL} = 3.0V$ )	-0.2	—	0.7	V
V <sub>IHR</sub>	Input High Voltage	1.2	—	$V_{DD} + 0.2$	V
V <sub>ILR</sub>	Input Low Voltage	-0.2	—	0.4	V

7148 tbl 05

### Recommended DC Operating Conditions ( $V_{DDQL} = 2.5V \pm 100mV$ )

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	1.7	1.8	1.9	V
V <sub>DDQL</sub>	Left Port Supply Voltage	2.4	2.5	2.6	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IHL</sub>	Input High Voltage ( $V_{DDQL} = 2.5V$ )	1.7	—	$V_{DDQL} + 0.3$	V
V <sub>ILL</sub>	Input Low Voltage ( $V_{DDQL} = 2.5V$ )	-0.3	—	0.6	V
V <sub>IHR</sub>	Input High Voltage	1.2	—	$V_{DD} + 0.2$	V
V <sub>ILR</sub>	Input Low Voltage	-0.2	—	0.4	V

7148 tbl 06

### Recommended DC Operating Conditions ( $V_{DDQL} = 1.8V \pm 100mV$ )

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	1.7	1.8	1.9	V
V <sub>DDQL</sub>	Left Port Supply Voltage	1.7	1.8	1.9	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IHL</sub>	Input High Voltage ( $V_{DDQL} = 1.8V$ )	1.2	—	$V_{DDQL} + 0.2$	V
V <sub>ILL</sub>	Input Low Voltage ( $V_{DDQL} = 1.8V$ )	-0.2	—	0.4	V
V <sub>IHR</sub>	Input High Voltage	1.2	—	$V_{DD} + 0.2$	V
V <sub>ILR</sub>	Input Low Voltage	-0.2	—	0.4	V

7148 tbl 06\_5

#### NOTES:

1.  $V_{IL} \geq -1.5V$  for pulse width less than 10ns.
2.  $V_{TERM}$  must not exceed  $V_{DD} + 0.3V$ .

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ( $V_{DD} = 1.8V \pm 100mV$ )

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I <sub>LI</sub>	Input Leakage Current	$V_{DD} = 1.8V, V_{IN} = 0V \text{ to } V_{DD}$	-1	1	$\mu A$
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}, V_{OUT} = 0V \text{ to } V_{DD}$	-1	1	$\mu A$
V <sub>OLL</sub>	Output Low Voltage ( $V_{DDQL} = 3.0V$ )	I <sub>OLL</sub> = +2mA	—	0.4	V
V <sub>OHL</sub>	Output High Voltage ( $V_{DDQL} = 3.0V$ )	I <sub>OHL</sub> = -2mA	2.1	—	V
V <sub>OLL</sub>	Output Low Voltage ( $V_{DDQL} = 2.5V$ )	I <sub>OLL</sub> = +2mA	—	0.4	V
V <sub>OHL</sub>	Output High Voltage ( $V_{DDQL} = 2.5V$ )	I <sub>OHL</sub> = -2mA	2.0	—	V
V <sub>OLL</sub>	Output Low Voltage ( $V_{DDQL} = 1.8V$ )	I <sub>OLL</sub> = +0.1mA	—	0.2	V
V <sub>OHL</sub>	Output High Voltage ( $V_{DDQL} = 1.8V$ )	I <sub>OHL</sub> = -0.1mA	$V_{DDQL} - 0.2V$	—	V
V <sub>OLR</sub>	Output Low Voltage	I <sub>OLR</sub> = +0.1mA	—	0.2	V
V <sub>OHR</sub>	Output High Voltage	I <sub>OHR</sub> = -0.1mA	$V_{DD} - 0.2V$	—	V
V <sub>OLINT</sub> <sup>(1,2)</sup>	Output Low Voltage Interrupt	I <sub>OL</sub> = +2mA	—	0.4	V

### NOTES:

7148 tbl 08

- Interrupt can be level shifted to a higher voltage by tying a resistor (R3) to an external power supply (VDDINTx). The value of R3 is a trade off between I<sub>INX</sub> and power.
- $V_{DDINT_R} \geq V_{DD}$ ,  $V_{DDINT_L} \geq V_{DDQL}$

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ( $V_{DD} = 1.8V \pm 100mV$ )

Symbol	Parameter	Test Condition	Version	70P264/254/244 Ind'l Only				Unit
				40ns		55ns		
				Typ. <sup>(1)</sup>	Max.	Typ. <sup>(1)</sup>	Max.	
I <sub>DD</sub>	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_R$ and $\overline{CE}_L = V_{IL}$ , Outputs Open $f = f_{MAX}^{(2)}$	IND'L L	25	40	15	25	mA
ISB1	Standby Current (Both Ports Inactive)	$\overline{CE}_R = V_{DD} - 0.2V$ and $\overline{CE}_L = V_{DDQL} - 0.2V$ , $f = f_{MAX}^{(2)}$	IND'L L	2	6	2	6	μA
ISB2	Standby Current (One Port Inactive, One Port Active)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(3)}$ , Active Port Outputs Open $f = f_{MAX}^{(2)}$	IND'L L	8.5	18	8.5	14	mA
ISB3	Full Standby Current (Both Ports Inactive - CMOS Level Inputs)	$\overline{CE}_L \geq V_{DDQL} - 0.2V$ and $\overline{CE}_R \geq V_{DD} - 0.2V$ , $f = 0$	IND'L L	2	6	2	6	μA
ISB4	Standby Current (One Port Inactive, One Port Active - CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DDQ} - 0.2V^{(3)}$ , Active Port Outputs Open $f = f_{MAX}^{(2)}$	IND'L L	8.5	18	8.5	14	mA

7148 tbl 09

### NOTES:

- $V_{DD} = 1.8V$ ,  $T_A = +25^\circ C$ , and are not production tested. I<sub>DD</sub> = 15mA (typ.)
- At  $f = f_{MAX}$ , address and control lines are cycling at the maximum frequency read cycle of 1/t<sub>rc</sub>, and using "AC Test Conditions".
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".

## AC Test Conditions

Input Pulse Levels	GND to 3.0V/GND to 2.5V/GND to 1.8V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V/1.25V/0.9V
Output Reference Levels	1.5V/1.25V/0.9V
Output Load	Figure 1A

7148 tbl 10

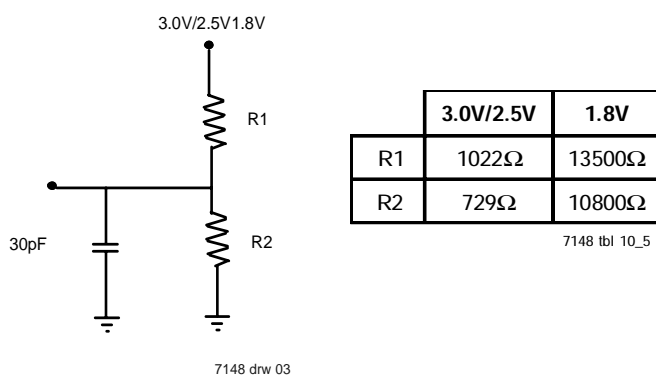


Figure 1A. AC Output Test Load  
(5pF for tLZ, tHZ, tWZ, tOW)

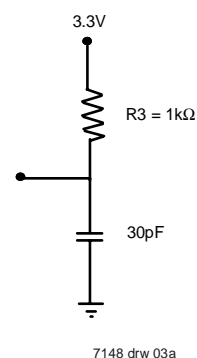
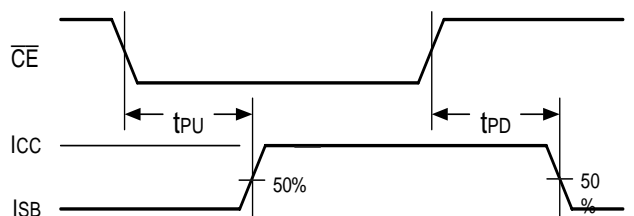


Figure 1B. AC Output Test Load for Interrupt

## Timing of Power-Up Power-Down



7148 drw 04

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(2)</sup>

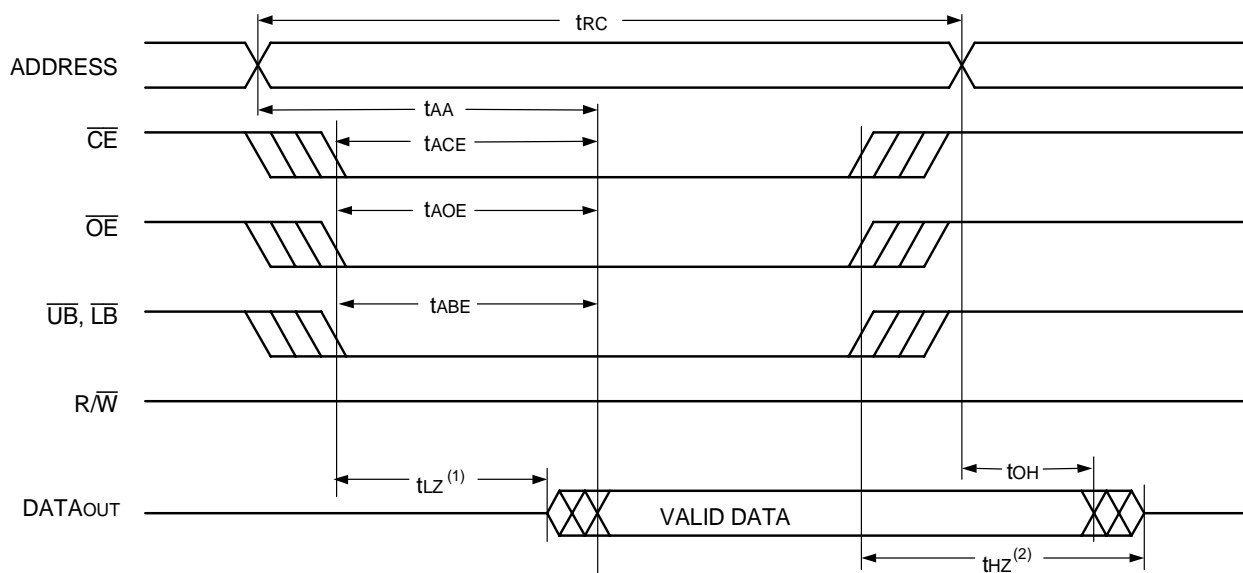
Symbol	Parameter	70P264/254/244 Ind'l Only				Unit
		40ns		55ns		
		Min.	Max.	Min.	Max.	
READ CYCLE						
t <sub>RC</sub>	Read Cycle Time	40	—	55	—	ns
t <sub>AA</sub>	Address Access Time	—	40	—	55	ns
t <sub>ACE</sub>	Chip Enable Access Time	—	40	—	55	ns
t <sub>ABE</sub>	Byte Enable Access Time	—	40	—	55	ns
t <sub>AOE</sub>	Output Enable Access Time	—	25	—	30	ns
t <sub>OH</sub>	Output Hold from Address Change	5	—	5	—	ns
t <sub>LZ</sub>	Output Low-Z Time <sup>(1,3)</sup>	5	—	5	—	ns
t <sub>HZ</sub>	Output High-Z Time <sup>(1,3)</sup>	—	10	—	25	ns
t <sub>PU</sub>	Chip Enable to Power Up Time <sup>(1)</sup>	0	—	0	—	ns
t <sub>PD</sub>	Chip Disable to Power Down Time <sup>(1)</sup>	—	40	—	55	ns

### NOTES:

7148 tbl 11

1. This parameter is guaranteed by device characterization, but is not production tested.
2. The specification for t<sub>OH</sub> must be met by the device supplying write data to the SRAM under all operating conditions. Although t<sub>OH</sub> and t<sub>OW</sub> values will vary over voltage and temperature, the actual t<sub>OH</sub> will always be smaller than the actual t<sub>OW</sub>.
3. At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.

## Waveform of Read Cycles



7148 drw 05

### NOTES:

1. Timing depends on which signal is asserted last,  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{LB}$ , or  $\overline{UB}$ .
2. Timing depends on which signal is de-asserted first  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{LB}$ , or  $\overline{UB}$ .

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(3)</sup>

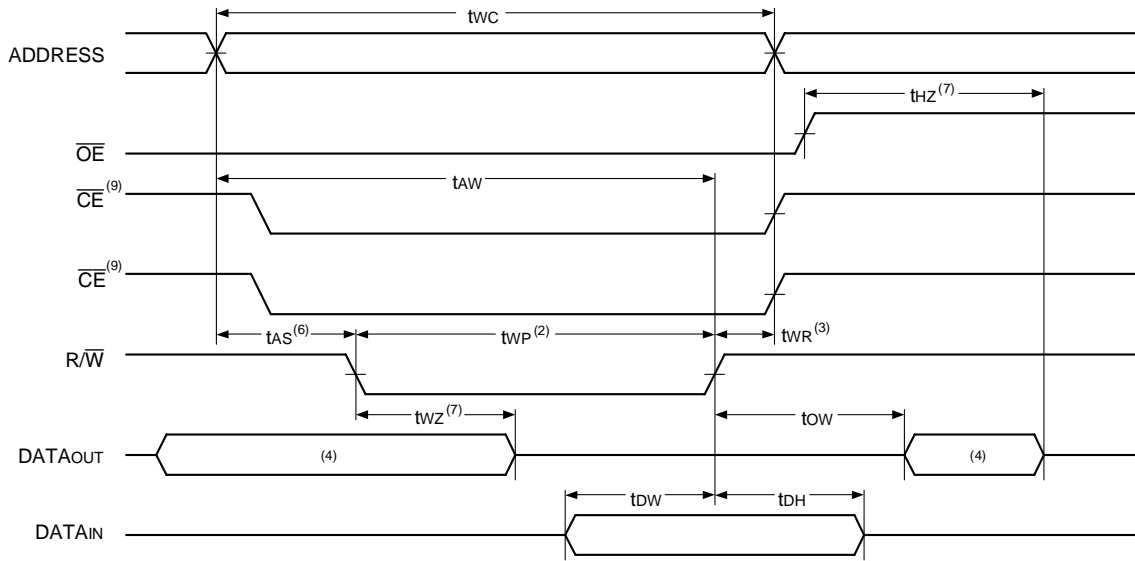
Operating Temperature and Supply Voltage						
Symbol	Parameter	70P264/254/244 Ind'l Only				Unit
		40ns		55ns		
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t <sub>WC</sub>	Write Cycle Time	40	—	55	—	ns
t <sub>EW</sub>	Chip Enable to End-of-Write <sup>(2)</sup>	30	—	45	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	30	—	45	—	ns
t <sub>AS</sub>	Address Set-up Time <sup>(2)</sup>	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	25	—	40	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	ns
t <sub>DW</sub>	Data Valid to End-of-Write	20	—	30	—	ns
t <sub>DH</sub>	Data Hold Time <sup>(3)</sup>	0	—	0	—	ns
t <sub>WZ</sub>	Write Enable to Output in High-Z <sup>(1)</sup>	—	15	—	25	ns
t <sub>OW</sub>	Output Active from End-of-Write <sup>(1,3)</sup>	0	—	0	—	ns

7148 tbl 12

### NOTES:

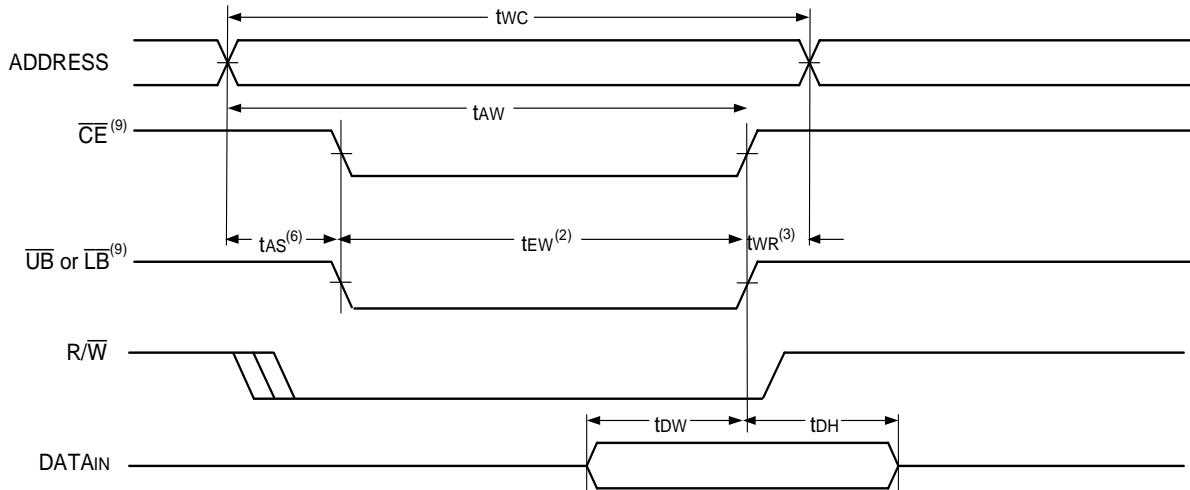
1. This parameter is guaranteed by device characterization, but is not production tested.
2. To access SRAM, CE = V<sub>IL</sub>, UB or LB = V<sub>IL</sub>.
3. The specification for t<sub>DH</sub> must be met by the device supplying write data to the SRAM under all operating conditions. Although t<sub>DH</sub> and t<sub>OW</sub> values will vary over voltage and temperature, the actual t<sub>DH</sub> will always be smaller than the actual t<sub>OW</sub>.

## Timing Waveform of Write Cycle No. 1, $R/\overline{W}$ Controlled Timing<sup>(1,5,8)</sup>



7148 drw 06

## Timing Waveform of Write Cycle No. 2, $\overline{CE}$ , $\overline{UB}$ , $\overline{LB}$ Controlled Timing<sup>(1,5)</sup>



7148 drw 07

### NOTES:

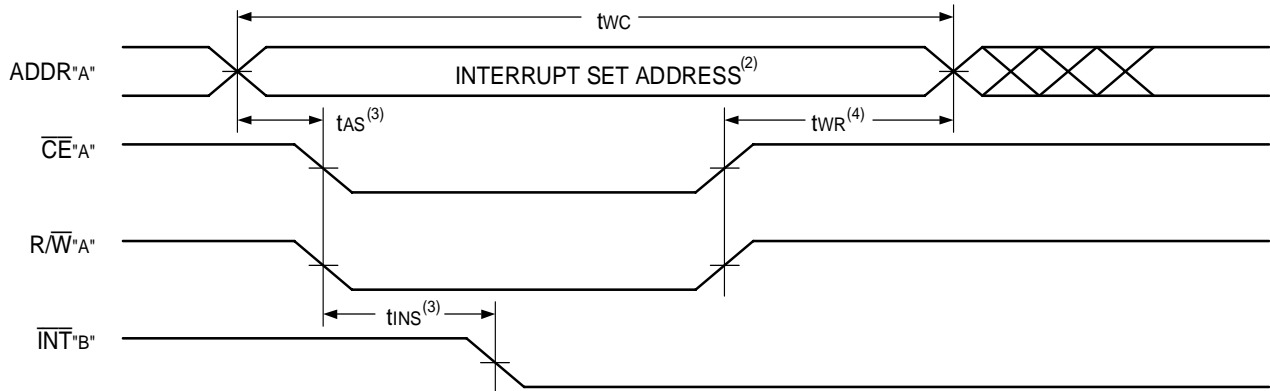
1.  $R/\overline{W}$  or  $\overline{CE}$  or  $\overline{UB}$  &  $\overline{LB}$  must be high during all address transitions.
2. A write occurs during the overlap ( $t_{EW}$  or  $t_{WP}$ ) of a low  $\overline{UB}$  or  $\overline{LB}$  and a LOW  $\overline{CE}$  and a LOW  $R/\overline{W}$  for memory array writing cycle.
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $R/\overline{W}$  going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after the  $R/\overline{W}$  LOW transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal is asserted last,  $\overline{CE}$ ,  $R/\overline{W}$  or byte control.
7. This parameter is guaranteed by device characterization, but is not production tested.
8. If  $\overline{OE}$  is LOW during  $R/\overline{W}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or ( $t_{WZ} + t_{OW}$ ) to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE}$  is HIGH during an  $R/\overline{W}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .
9. To access SRAM,  $\overline{CE} = V_{IL}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ .

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

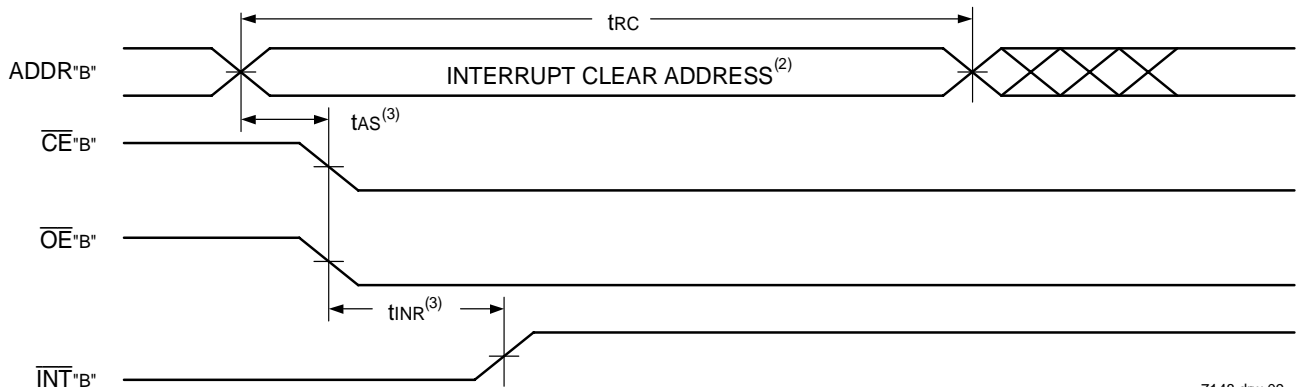
Symbol	Parameter	70P264/254/244 Ind'l Only				Unit
		40ns		55ns		
		Min.	Max.	Min.	Max.	
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	35	—	45	ns
tINR	Interrupt Reset Time	—	45	—	45	ns

7148 tbl 13

### Waveform of Interrupt Timing<sup>(1)</sup>



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#### NOTES:

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt Truth Table II.
3. Timing depends on which enable signal ( $\overline{CE}$  or  $\overline{R/W}$ ) is asserted last.
4. Timing depends on which enable signal ( $\overline{CE}$  or  $\overline{R/W}$ ) is de-asserted first.

Truth Table II — Interrupt Flag<sup>(1)</sup>

Left Port					Right Port					Function
R/W <sub>L</sub>	C <sub>E</sub> <sub>L</sub>	O <sub>E</sub> <sub>L</sub>	A <sub>13L</sub> -A <sub>0L</sub> <sup>(1)</sup>	INT <sub>L</sub>	R/W <sub>R</sub>	C <sub>E</sub> <sub>R</sub>	O <sub>E</sub> <sub>R</sub>	A <sub>13R</sub> -A <sub>0R</sub> <sup>(1)</sup>	INT <sub>R</sub>	
L	L	X	3FFF	X	X	X	X	X	L	Set Right INT <sub>R</sub> Flag
X	X	X	X	X	X	L	L	3FFF	H	Reset Right INT <sub>R</sub> Flag
X	X	X	X	L	L	L	X	3FFE	X	Set Left INT <sub>L</sub> Flag
X	L	L	3FFE	H	X	X	X	X	X	Reset Left INT <sub>L</sub> Flag

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NOTES:

1. A<sub>13x</sub> is a NC for IDT70P254. A<sub>13x</sub> and A<sub>12x</sub> are NC for IDT70P244. Interrupt Addresses are 1FFF and 1FFE for IDT70P254 and FFF and FFE for IDT70P244.

## Functional Description

The IDT70P264/254/244 provides two ports with separate control, address and I/O pins that permit independent access to any location in memory. The IDT70P264/254/244 has an automatic power down feature controlled by C<sub>E</sub>. The C<sub>E</sub> controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected (C<sub>E</sub> HIGH). When a port is enabled, access to the entire memory array is permitted.

## Power Supply

Each port can operate on independent I/O voltages. This is determined by what is connected to the V<sub>DDIOL</sub> and V<sub>DD</sub> pins. The supported I/O standards are 1.8V/2.5V LVCMOS and 3.0V LVTTTL.

The IDT70P264/254/244 includes power supply isolation functionality which aids system power management. V<sub>DD</sub> and V<sub>DDIOL</sub> can be independently powered up/down which allows the left port or the right port and core to be powered down when not in use. If V<sub>DDIOL</sub> is powered down, but V<sub>DD</sub> remains powered up all inputs to the core from the left port will be forced to deasserted states at full swing DC values to minimize leakage current and active power consumption. If V<sub>DD</sub> is powered down but V<sub>DDIOL</sub> remain powered up, all outputs for the left port will remain in the state they were in prior to power down.

## Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag (INT<sub>L</sub>) is asserted when the right port writes to memory location 3FFE (HEX) (1FFE for IDT70P254, FFE for IDT70P244), where a write is defined as the C<sub>E</sub>=R/W=V<sub>IL</sub> per Truth Table II. The left port clears the interrupt by accessing address location 3FFE (1FFE for IDT70P254, FFE for IDT70P244) when C<sub>E</sub>=O<sub>E</sub>=V<sub>IL</sub>, R/W is a "don't care". Likewise, the right port interrupt flag (INT<sub>R</sub>) is asserted when the left port writes to memory location 3FFF (HEX) (1FFF for IDT70P254, FFF for IDT70P244) and to clear the interrupt flag (INT<sub>R</sub>), the right port must read the memory location 3FFF. The message (16 bits) at 3FFE or 3FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table II for the interrupt operation.

The interrupt outputs of the IDT70P264/254/244 should be connected to an interrupt power supply (V<sub>DDINTx</sub>) through an external pull-up resistor. As long as V<sub>DDINTx</sub> ≥ V<sub>DD</sub> and V<sub>DDINTx</sub> ≥ V<sub>DDQL</sub>, there will be no current flowing between V<sub>DDINTx</sub> and V<sub>DD</sub>/V<sub>DDQL</sub>.

## Ordering Information

XXXXX	A	999	A	A	A	
Device Type	Power	Speed	Package		Process/ Temperature Range	
					I	Industrial (-40°C to +85°C)
					G	Green
					BY	81 Ball 0.5mm-pitch BGA(BY81)
					40 55	Industrial Only } Speed in nanoseconds
					L	Low Power
					70P264	256K (16K x 16) 1.8V Dual-Port SRAM
					70P254	128K (8K x 16) 1.8V Dual-Port SRAM
					70P244	64K (4K x 16) 1.8V Dual-Port SRAM

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## Datasheet Document History

09/26/08:	Initial Datasheet
02/20/09:	Removed Preliminary status from entire datasheet Page 14 Removed "IDT" from orderable part number

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