

Dual N-Channel 2.5-V (G-S) MOSFET, ESD Protected

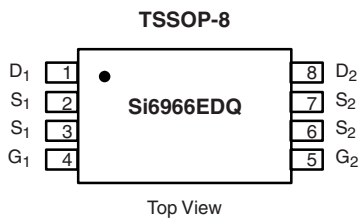
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.030 at $V_{GS} = 4.5$ V	± 5.2
	0.040 at $V_{GS} = 2.5$ V	± 4.5

FEATURES

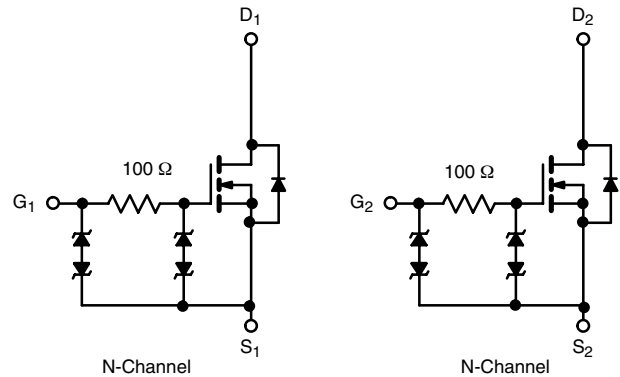
- Halogen-free
- ESD Protected: 4000 V



RoHS
COMPLIANT



Ordering Information: Si6966EDG-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150$ °C) ^{a, b}	I_D	$T_A = 25$ °C	± 5.2
		$T_A = 70$ °C	± 4.0
Pulsed Drain Current	I_{DM}	± 30	A
Continuous Source Current (Diode Conduction) ^{a, b}	I_S	1.25	
Maximum Power Dissipation ^{a, b}	P_D	$T_A = 25$ °C	1.25
		$T_A = 70$ °C	0.72
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	115	110	$t \leq 10$ s	°C/W
				Steady State	

Notes:

a. Surface Mounted on FR4 board.

b. $t \leq 10$ s.

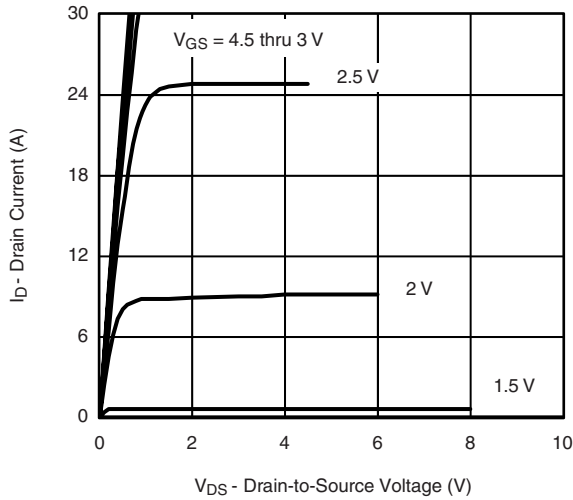
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 4.5\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = +20\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 4.5\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}$, $I_D = 5.2\text{ A}$		0.021	0.030	Ω
		$V_{GS} = 2.5\text{ V}$, $I_D = 4.5\text{ A}$		0.028	0.040	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 5.2\text{ A}$		20		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25\text{ A}$, $V_{GS} = 0\text{ V}$		0.65	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 5.2\text{ A}$		15	25	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			4.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}$, $R_L = 10\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_G = 6\text{ }\Omega$		100	200	ns
Rise Time	t_r			130	250	
Turn-Off Delay Time	$t_{d(off)}$			420	800	
Fall Time	t_f			220	450	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		210	500	

Notes:

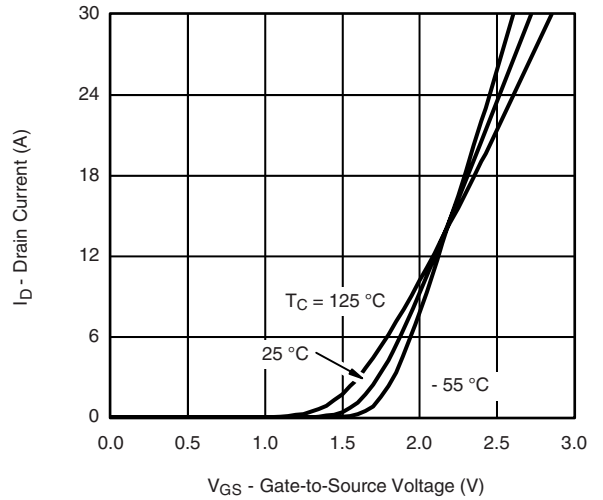
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

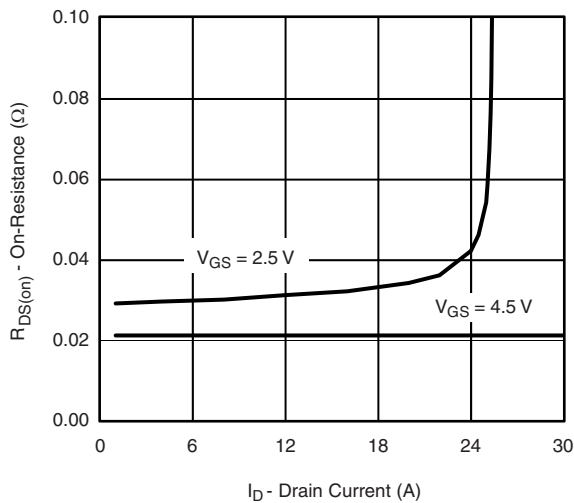
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



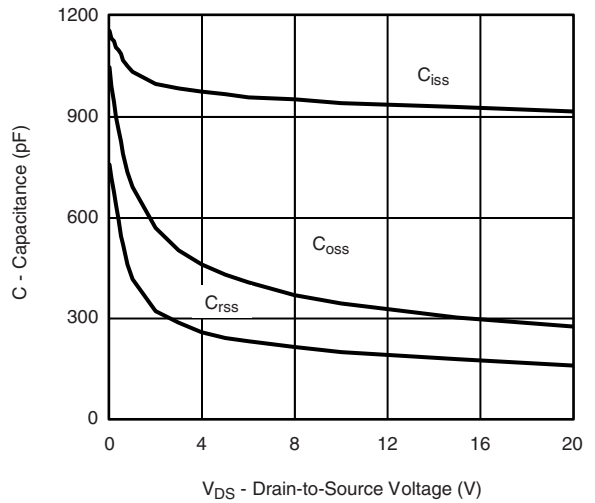
Output Characteristics



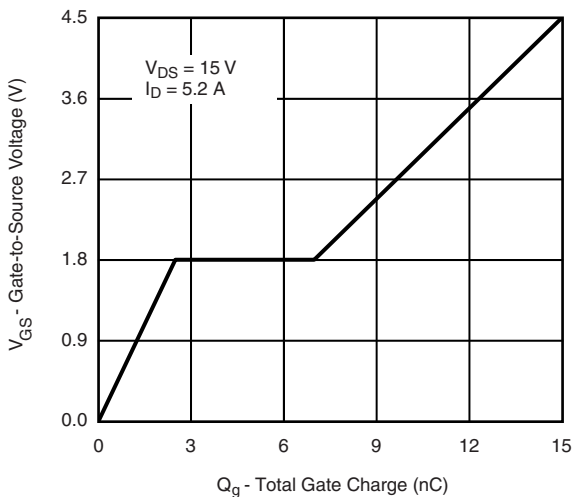
Transfer Characteristics



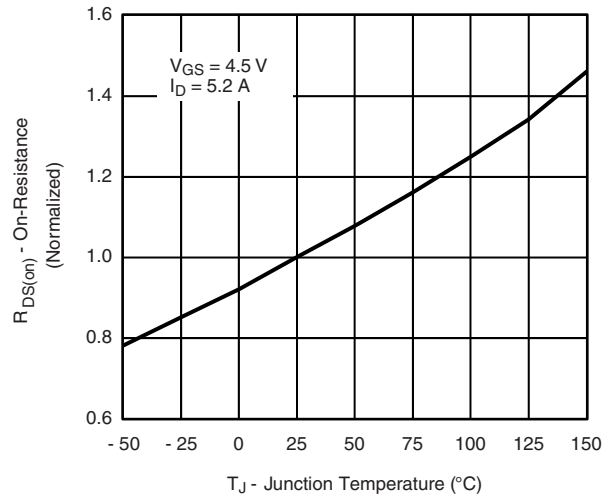
On-Resistance vs. Drain Current



Capacitance

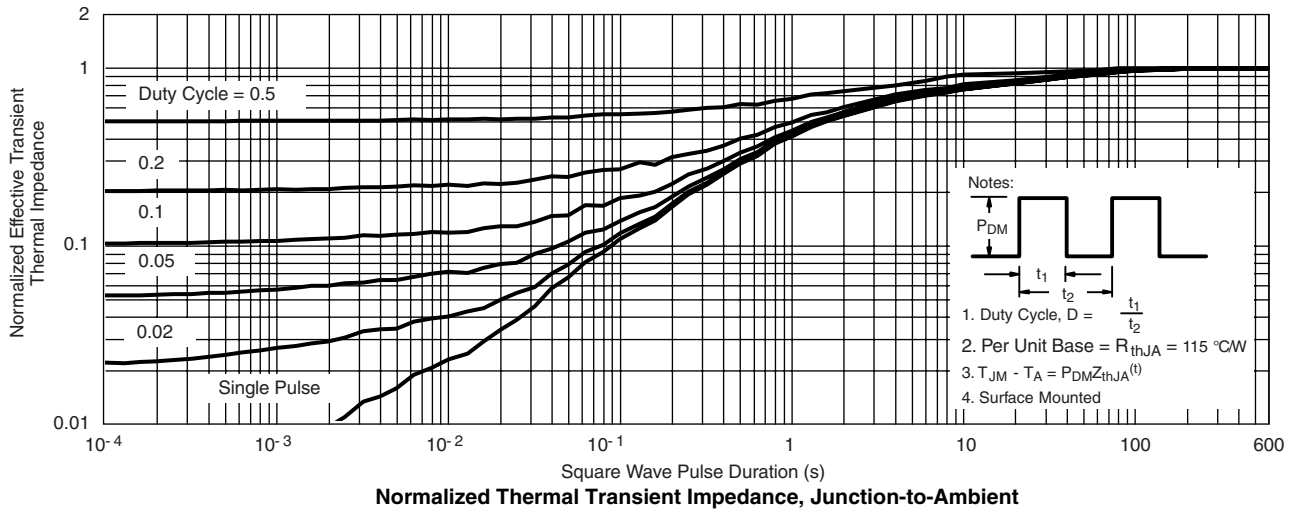
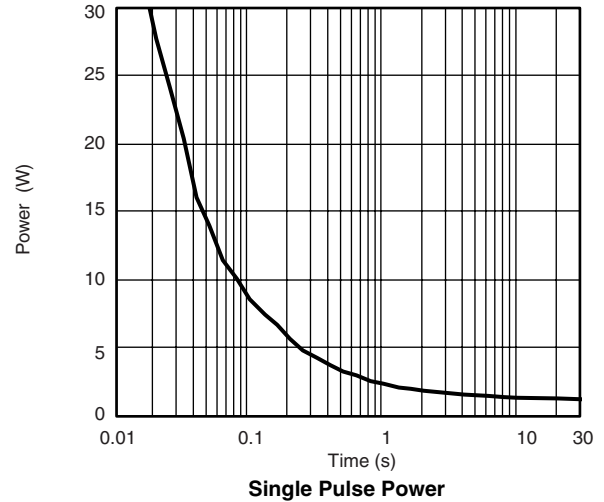
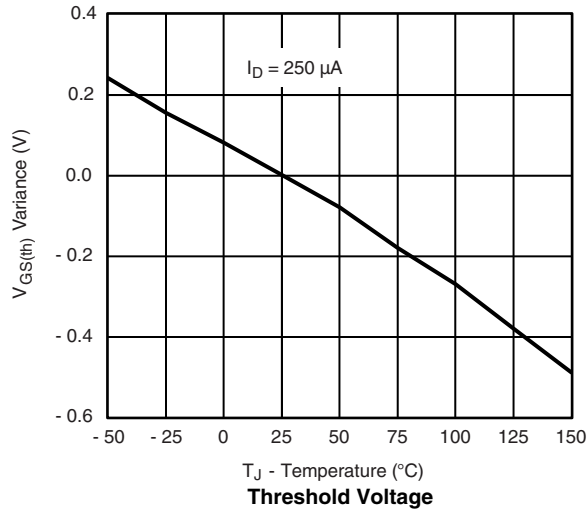
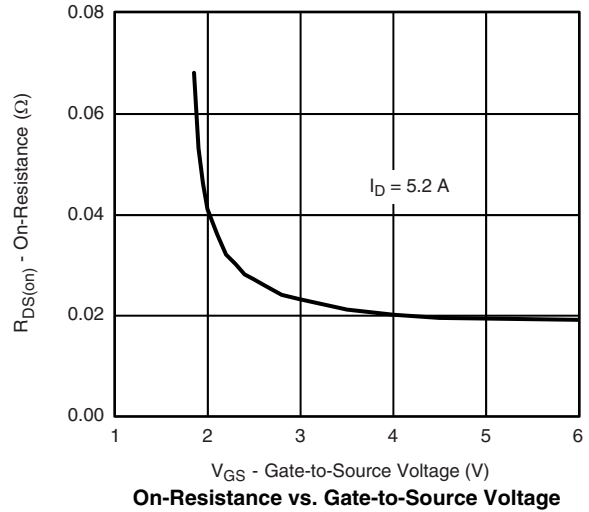
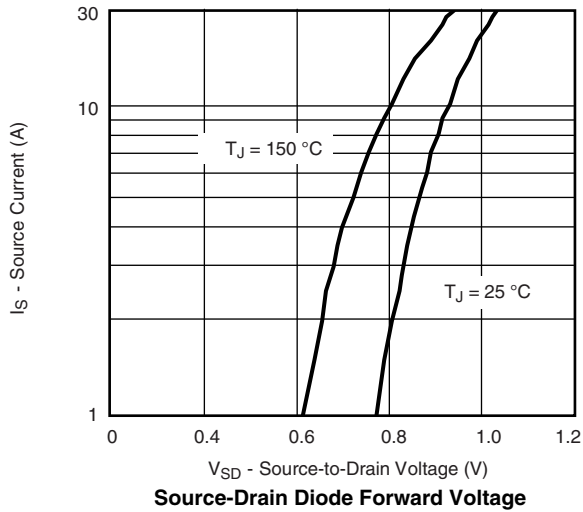


Gate Charge



On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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