CMOS Static RAM 16K (2K x 8-Bit)

6116SA
6116LA

Features

- **High-speed access and chip select times**
  - *Commercial: 15/20/25ns (max.)*
  - *Industrial: 20/25ns (max.)*
  - *Military: 20/25/35/45/55/70/90/120/150ns (max.)*
- **Low-power consumption**
- **Battery backup operation**
  - *2V data retention voltage (LA version only)*
- **Produced with advanced CMOS high-performance technology**
- **CMOS process virtually eliminates alpha particle soft-error rates**
- **Input and output directly TTL-compatible**
- **Static operation: no clocks or refresh required**
- **Available in ceramic 24-pin DIP, ceramic and plastic 24-pin Thin Dip and 24-pin SOIC**
- **Military product compliant to MIL-STD-833, Class B**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

Description

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using high-performance, high-reliability CMOS technology.

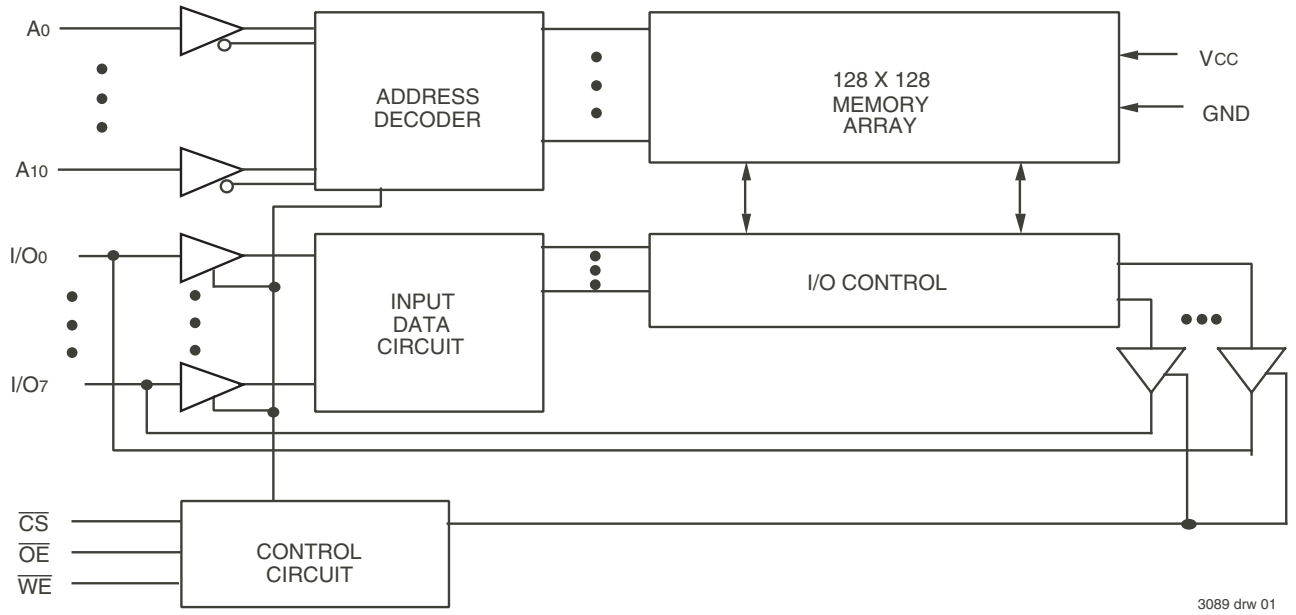
Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as $\overline{CS}$ remains HIGH. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

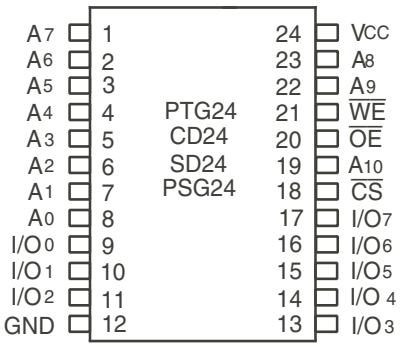
The IDT6116SA/LA is packaged in 24-pin 300mil plastic DIP, 24-pin 600mil and 300mil ceramic DIP, or 24-lead gull-wing SOIC providing high board-level packing densities.

Military grade product is manufactured in compliance to MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Functional Block Diagram



Pin Configurations(1)



3089 drw 02

DIP/SOIC
Top View

NOTE:
1. This text does not indicate orientation of actual part-marking.

Pin Description

Name	Description
A_0 - A_{10}	Address Inputs
I/O_0 - I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

3089 tbl 01

Truth Table(1)

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High-Z
Read	L	L	H	$DATA_{OUT}$
Read	L	H	H	High-Z
Write	L	X	L	$DATA_{IN}$

3089 tbl 02

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't Care.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

3089 tbl 03

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

Absolute Maximum Ratings(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

3089 tbl 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} +0.5V.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3089 tbl 05

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5(2)	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC} +0.5	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

3089 tbl 06

NOTES:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.
2. V_{IN} must not exceed V_{CC} +0.5V.

DC Electrical Characteristics
(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		IDT6116SA Min.	IDT6116SA Max.	IDT6116LA Min.	IDT6116LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L & IND	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L & IND	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

3089 tbl 07

DC Electrical Characteristics(1)
(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6116SA15 Com'l Only	6116SA20 6116LA20 Com'l & Ind	6116SA20 6116LA20 Mil	6116SA25 6116LA25 Com'l & Ind	6116SA25 6116LA25 Mil	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}$ ≤ V_{IL}, Outputs Open V_{CC} = Max., f = 0	SA	105	105	130	100	90	mA
		LA	—	95	120	95	85	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ ≤ V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	SA	150	130	150	120	135	mA
		LA	—	120	140	110	125	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	SA	40	40	50	40	45	mA
		LA	—	35	45	35	40	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}, f = 0	SA	2	2	10	2	10	mA
		LA	—	0.1	0.9	0.1	0.9	

3089 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, only address inputs are cycling at f_{MAX}, f = 0 means address inputs are not changing.

DC Electrical Characteristics(1) (continued)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6116SA35 6116LA35 Mil Only	6116SA45 6116LA45 Mil Only	6116SA55 6116LA55 Mil Only	6116SA70 6116LA70 Mil Only	6116SA90 6116LA90 Mil Only	6116SA120 6116LA120 Mil Only	6116SA150 6116LA150 Mil Only	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS} \le V_{IL}$, Outputs Open V_{CC} = Max., f = 0	SA	90	90	90	90	90	90	90	mA
		LA	85	85	85	85	85	85	85	
I_{CC2}	Dynamic Operating Current, $\overline{CS} \le V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	SA	115	100	100	100	100	100	90	mA
		LA	105	95	90	90	85	85	85	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	SA	35	25	25	25	25	25	25	mA
		LA	30	20	20	20	25	15	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \le V_{LC}$ or $V_{IN} \ge V_{HC}$, f = 0	SA	10	10	10	10	10	10	10	mA
		LA	0.9	0.9	0.9	0.9	0.9	0.9	0.9	

3089 tbl 09

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, only address inputs are toggling at f_{MAX}, f = 0 means address inputs are not changing.

Data Retention Characteristics Over All Temperature Ranges

(LA Version Only) (V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @ 2.0V	Typ.(1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	0.5	1.5	200	300	µA
			COM'L.	—	0.5	1.5	20	30	
t_{CDR}(3)	Chip Deselect to Data Retention Time	$\overline{CS} \ge V_{HC}$ $V_{IN} \ge V_{HC}$ or $\le V_{LC}$		—	0	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$	Input Leakage Current			—	—	—	2	2	µA

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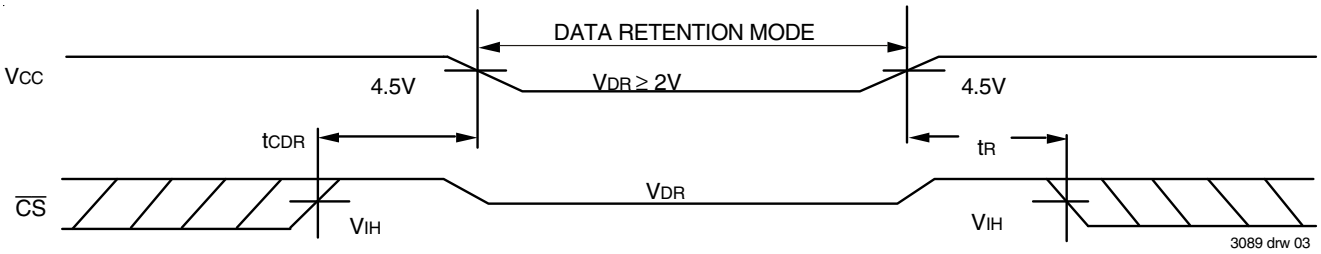
NOTES:
1. T_A = + 25°C
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

Low VCC Data Retention Waveform



AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

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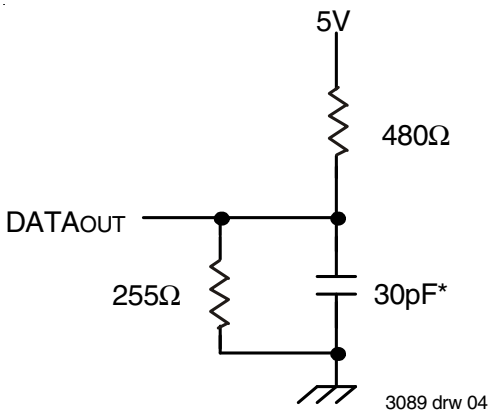

Figure 1. AC Test Load

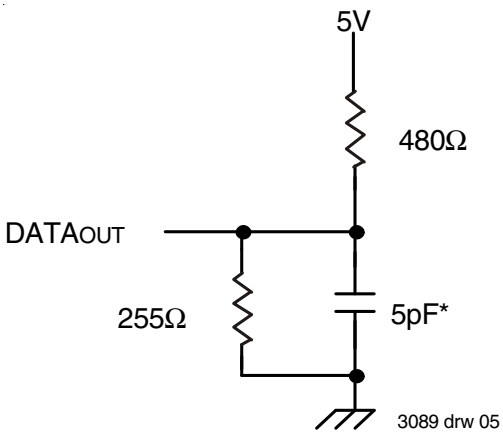

Figure 2. AC Test Load
(for tOLZ, tCLZ, tOHZ, tWHZ, tCHZ & tOW)

*Including scope and jig.

AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA15[1]		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35[2] 6116LA35[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	19	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
t_{CLZ}[3]	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	10	—	13	—	20	ns
t_{OLZ}[3]	Output Enable to Output in Low-Z	0	—	0	—	5	—	5	—	ns
t_{CHZ}[3]	Chip Deselect to Output in High-Z	—	10	—	11	—	12	—	15	ns
t_{OHZ}[3]	Output Disable to Output in High-Z	—	8	—	8	—	10	—	13	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}[3]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[3]	Chip Deselect to Power Down Time	—	15	—	20	—	25	—	35	ns

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AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges) (continued)

Symbol	Parameter	6116SA45[2] 6116LA45[2]		6116SA55[2] 6116LA55[2]		6116SA70[2] 6116LA70[2]		6116SA90[2] 6116LA90[2]		6116SA120[2] 6116LA120[2]		6116SA150[2] 6116LA150[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
t_{RC}	Read Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	—	90	—	120	—	150	ns
t_{ACS}	Chip Select Access Time	—	45	—	50	—	65	—	90	—	120	—	150	ns
t_{CLZ}[3]	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	25	—	40	—	50	—	60	—	80	—	100	ns
t_{OLZ}[3]	Output Enable to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[3]	Chip Deselect to Output in High-Z	—	20	—	30	—	35	—	40	—	40	—	40	ns
t_{OHZ}[3]	Output Disable to Output in High-Z	—	15	—	30	—	35	—	40	—	40	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns

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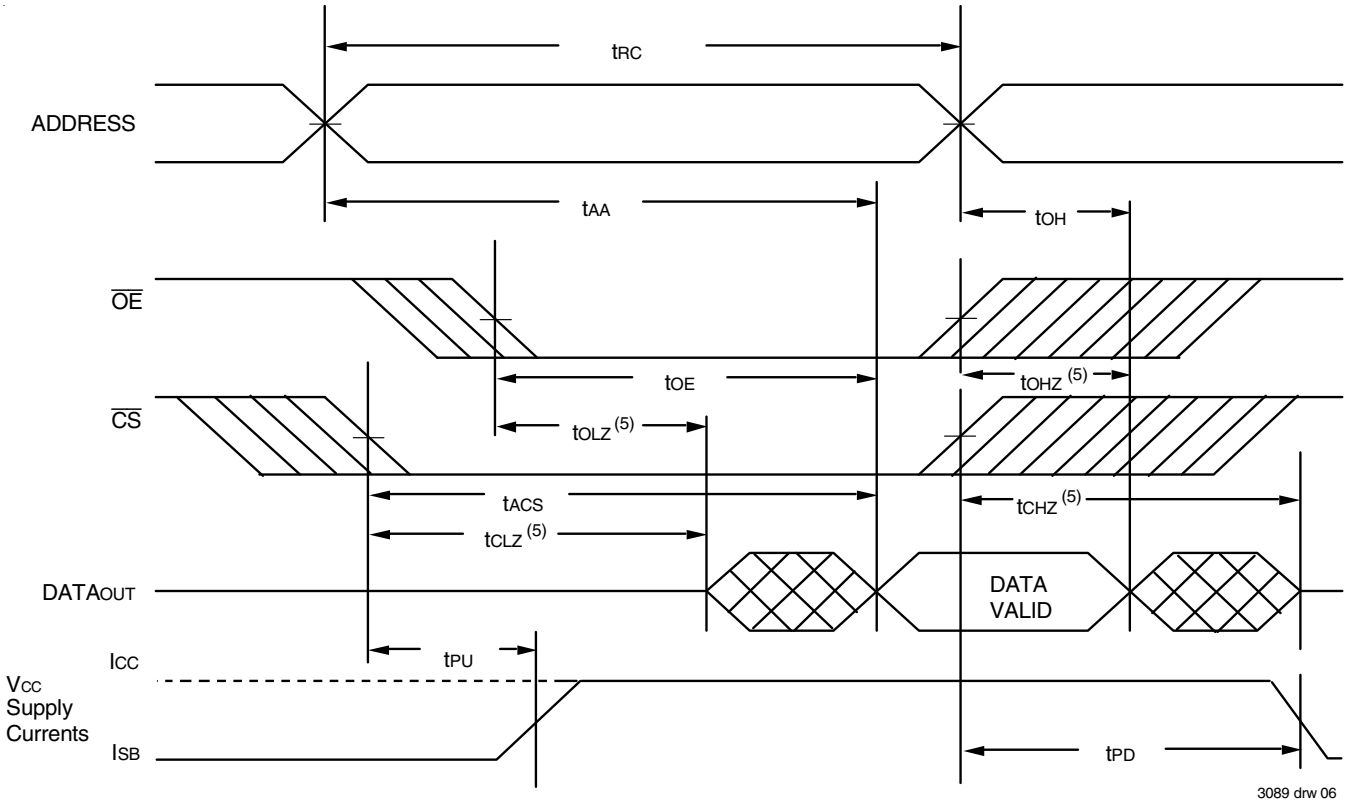
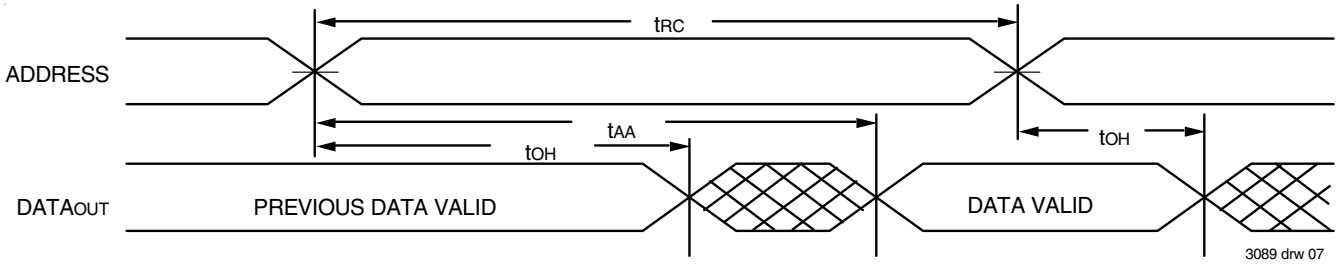
NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

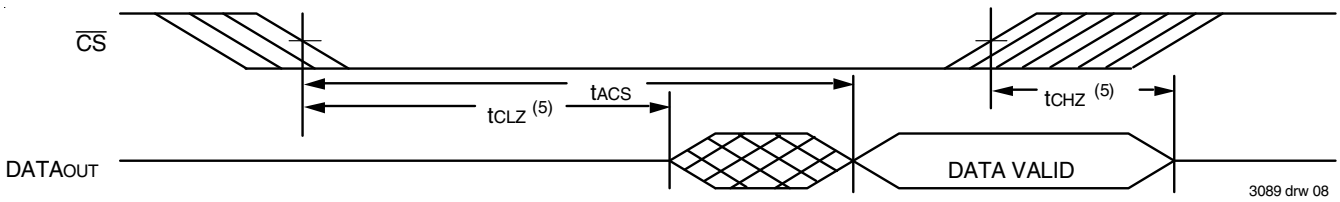
Timing Waveform of Read Cycle No. 1(1,3)



Timing Waveform of Read Cycle No. 2(1,2,4)



Timing Waveform of Read Cycle No. 3(1,3,4)



NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±500mV from steady state.

AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA15[1]		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35[2] 6116LA35[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	ns
t_{CW}	Chip Select to End-of-Write	13	—	15	—	17	—	25	—	ns
t_{AW}	Address Valid to End-of-Write	14	—	15	—	17	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[3]	Write to Output in High-Z	—	7	—	8	—	16	—	20	ns
t_{DW}	Data to Write Time Overlap	12	—	12	—	13	—	15	—	ns
t_{DH}[4]	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[3,4]	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

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AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)(con't)

Symbol	Parameter	6116SA45[2] 6116LA45[2]		6116SA55[2] 6116LA55[2]		6116SA70[2] 6116LA70[2]		6116SA90[2] 6116LA90[2]		6116SA120[2] 6116LA120[2]		6116SA150[2] 6116LA150[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
t_{WC}	Write Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
t_{CW}	Chip Select to End-of-Write	30	—	40	—	40	—	55	—	70	—	90	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	45	—	65	—	80	—	105	—	120	—	ns
t_{AS}	Address Set-up Time	0	—	5	—	15	—	15	—	20	—	20	—	ns
t_{WP}	Write Pulse Width	25	—	40	—	40	—	55	—	70	—	90	—	ns
t_{WR}	Write Recovery Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
t_{WHZ}[3]	Write to Output in High-Z	—	25	—	30	—	35	—	40	—	40	—	40	ns
t_{DW}	Data to Write Time Overlap	20	—	25	—	30	—	30	—	35	—	40	—	ns
t_{DH}[4]	Data Hold from Write Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
t_{OW}[3,4]	Output Active from End-of-Write	0	—	0	—	0	—	0	—	0	—	0	—	ns

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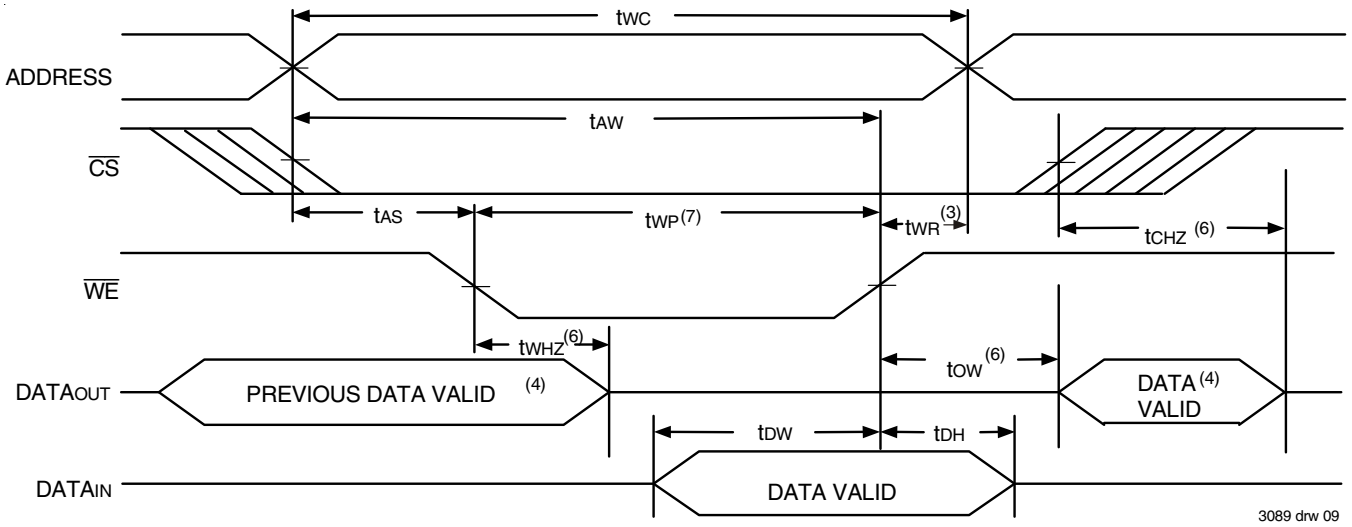
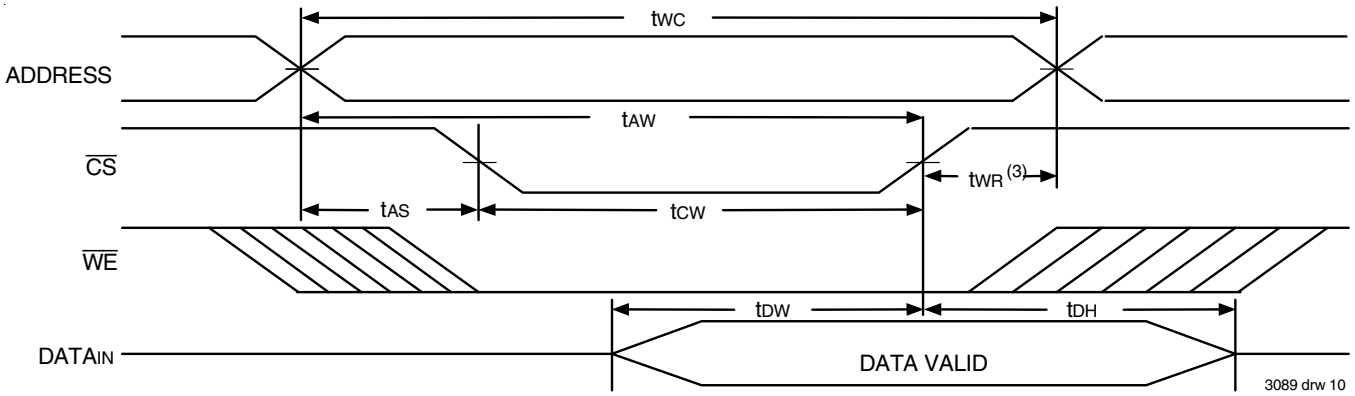
NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operation conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,2,5,7)

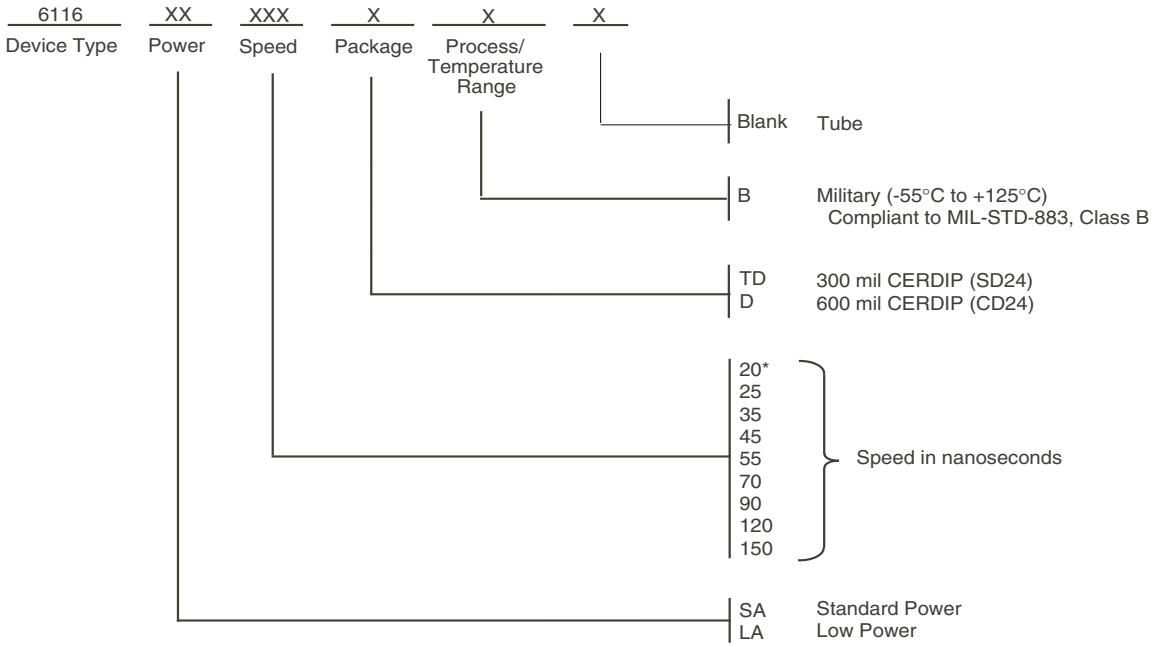


Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1,2,3,5,7)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±500mV from steady state.
7. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP}. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW}.

Ordering Information — Military



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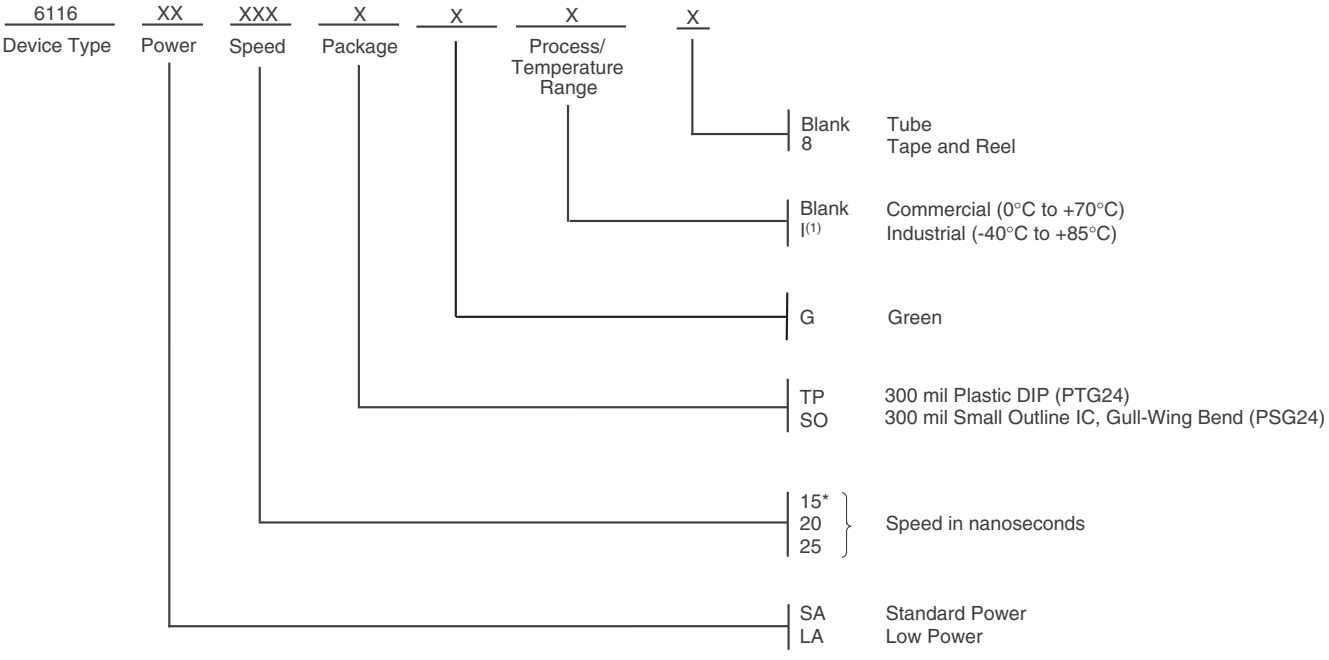
Ordering Information — Commercial & Industrial



*Available in commercial temperature range and standard power only.

NOTE:

1. Contact your local sales office for industrial temp range for other speeds, packages and powers.

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Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
20	6116LA20SOG	PSG24	SOIC	C
	6116LA20SOG8	PSG24	SOIC	C
	6116LA20SOGI	PSG24	SOIC	I
	6116LA20SOGI8	PSG24	SOIC	I
	6116LA20TDB	SD24	CDIP	M
	6116LA20TPG	PTG24	PDIP	C
	6116LA20TPGI	PTG24	PDIP	I
25	6116LA25DB	CD24	CDIP	M
	6116LA25SOG	PSG24	SOIC	C
	6116LA25SOG8	PSG24	SOIC	C
	6116LA25SOGI	PSG24	SOIC	I
	6116LA25SOGI8	PSG24	SOIC	I
	6116LA25TDB	SD24	CDIP	M
	6116LA25TPG	PTG24	PDIP	C
35	6116LA35DB	CD24	CDIP	M
	6116LA35TDB	SD24	CDIP	M
45	6116LA45DB	CD24	CDIP	M
	6116LA45TDB	SD24	CDIP	M
55	6116LA55DB	CD24	CDIP	M
	6116LA55TDB	SD24	CDIP	M
70	6116LA70DB	CD24	CDIP	M
	6116LA70TDB	SD24	CDIP	M
90	6116LA90DB	CD24	CDIP	M
	6116LA90TDB	SD24	CDIP	M
120	6116LA120DB	CD24	CDIP	M
	6116LA120TDB	SD24	CDIP	M
150	6116LA150DB	CD24	CDIP	M
	6116LA150TDB	SD24	CDIP	M

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
15	6116SA15SOG	PSG24	SOIC	C
	6116SA15SOG8	PSG24	SOIC	C
	6116SA15TPG	PTG24	PDIP	C
20	6116SA20DB	CD24	CDIP	M
	6116SA20SOG	PSG24	SOIC	C
	6116SA20SOG8	PSG24	SOIC	C
	6116SA20TDB	SD24	CDIP	M
	6116SA20TPG	PTG24	PDIP	C
	6116SA20TPGI	PTG24	PDIP	I
25	6116SA25SOG	PSG24	SOIC	C
	6116SA25SOG8	PSG24	SOIC	C
	6116SA25SOGI	PSG24	SOIC	I
	6116SA25SOGI8	PSG24	SOIC	I
	6116SA25TDB	SD24	CDIP	M
	6116SA25TPG	PTG24	PDIP	C
	6116SA25TPGI	PTG24	PDIP	I
35	6116SA35TDB	SD24	CDIP	M
45	6116SA45DB	CD24	CDIP	M
	6116SA45TDB	SD24	CDIP	M
55	6116SA55DB	CD24	CDIP	M
	6116SA55TDB	SD24	CDIP	M
70	6116SA70DB	CD24	CDIP	M
	6116SA70TDB	SD24	CDIP	M
90	6116SA90DB	CD24	CDIP	M
	6116SA90TDB	SD24	CDIP	M
120	6116SA120DB	CD24	CDIP	M
	6116SA120TDB	SD24	CDIP	M
150	6116SA150DB	CD24	CDIP	M
	6116SA150TDB	SD24	CDIP	M

Datasheet Document History

01/07/00		Updated to new format
	Pg. 1, 3, 4, 10	Added Industrial Temperature range offerings
	Pg. 9, 10	Separated ordering information into military, commercial, and industrial temperature range offerings
	Pg. 11	Added Datasheet Document History
08/09/00		Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"
12/30/03	Pg. 3,10	Corrected Industrial temp from -45C to -40C.
03/31/05	Pg. 10	Added "Restricted hazardous substance device" to ordering information.
11/15/06	Pg. 3	Changed power limits for commercial and industrial on speed grades 25ns and 35ns.
	Pg.4	Changed power limits for commercial and industrial on speed grade 45ns. Refer to PCN SR-0602-02.
04/26/11	Pg.1,2,3,4,6,10	Updated "Restricted hazardous substance device" to "Green". Obsoleted 24-pin SOJ, 24-pin 600 mil and 35ns, 45ns for Industrial & Commercial.
05/01/13	Pg. 1	Description paragraph 4, package information. Changed text to read "The IDT6116SA/LA is packaged in 24-pin 300mil plastic DIP, 24-pin 600mil and 300mil ceramic DIP, or 24-lead gull-wing SOIC providing high board-level packing densities". Removed IDT in reference to fabrication.
	Pg. 3	Updated DC Elec Chars (V_{CC} = 5.0V ± 10%) table by adding industrial to the Test Conditions. Updated DC Elec Chars (V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} + V_{CC} - 0.2V) table by removing the LA power for the 15ns speed.
	Pg. 10	Removed footnote "*Available in 300mil packaging only" from the Military ordering information.
07/17/20	Pg. 1 - 13	Rebranded as Renesas datasheet
	Pg. 2 & 10	Updated package codes.
	Pg. 10	Updated Ordering Information.
	Pg. 11	Added Orderable Part Information tables.

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