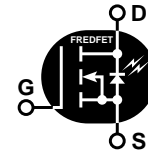


POWER MOS V®
FREDFET


Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.

- Fast Recovery Body Diode
- Lower Leakage
- Faster Switching
- 100% Avalanche Tested
- Surface Mount D³PAK Package


MAXIMUM RATINGS

 All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT20M45SVFR(G)	UNIT
V_{DSS}	Drain-Source Voltage	200	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	56	Amps
I_{DM}	Pulsed Drain Current ^①	224	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	300	Watts
	Linear Derating Factor	2.4	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	56	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	1300	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	200			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	56			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D[Cont.]}$)			0.045	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1.0mA$)	2		4	Volts


CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

USA

405 S.W. Columbia Street

EUROPE

Avenue J.F. Kennedy Bât B4 Parc Cadéra Nord

APT Website - <http://www.advancedpower.com>

Bend, Oregon 97702-1035

F-33700 Merignac - France

Phone: (541) 382-8028

Phone: (33) 5 57 92 15 15

FAX: (541) 388-0364

FAX: (33) 5 56 47 97 61

DYNAMIC CHARACTERISTICS

APT20M45SVFR(G)

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1 \text{ MHz}$		4050	4860	pF
C_{oss}	Output Capacitance			980	1375	
C_{rss}	Reverse Transfer Capacitance			300	450	
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_D [\text{Cont.}] @ 25^\circ\text{C}$		130	195	nC
Q_{gs}	Gate-Source Charge			30	45	
Q_{gd}	Gate-Drain ("Miller") Charge			55	80	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_D [\text{Cont.}] @ 25^\circ\text{C}$ $R_G = 1.6\Omega$		12	24	ns
t_r	Rise Time			14	28	
$t_{d(off)}$	Turn-off Delay Time			43	70	
t_f	Fall Time			7	14	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			56	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			224	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V$, $I_S = -I_D [\text{Cont.}]$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ⑤			5	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -I_D [\text{Cont.}]$, $di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		200	ns
		$T_j = 125^\circ\text{C}$		300	
Q_{rr}	Reverse Recovery Charge ($I_S = -I_D [\text{Cont.}]$, $di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$	0.7		μC
		$T_j = 125^\circ\text{C}$	2.4		
I_{RRM}	Peak Recovery Current ($I_S = -I_D [\text{Cont.}]$, $di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$	10		Amps
		$T_j = 125^\circ\text{C}$	18		

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.42	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature.

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ\text{C}$, $L = 0.83\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 56A$

⑤ $I_S \leq -I_D [\text{Cont.}]$, $di/dt = 100A/\mu s$, $V_{DD} \leq V_{DSS}$, $T_j \leq 150^\circ\text{C}$, $R_G = 2.0\Omega$, $V_R = 200V$.

APT Reserves the right to change, without notice, the specifications and information contained herein.

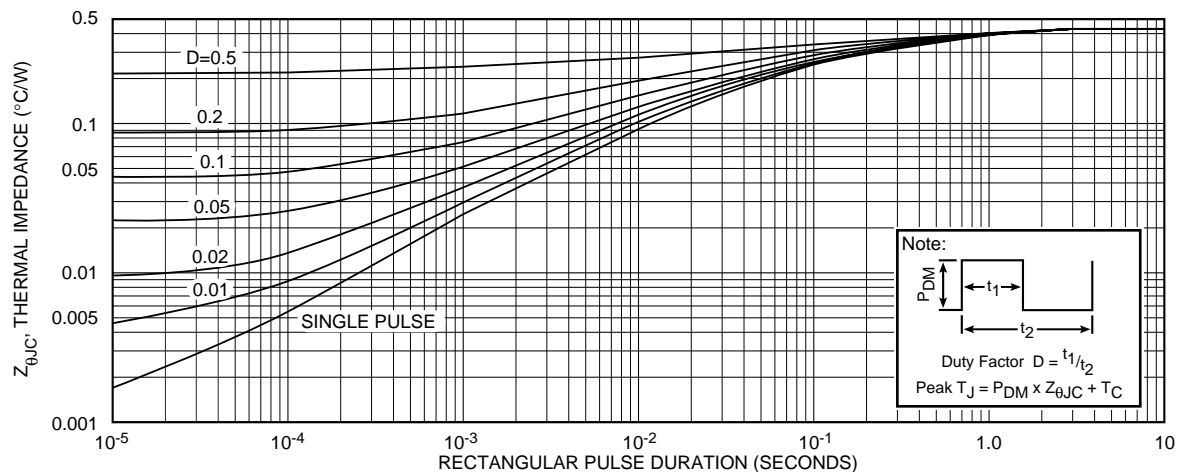


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

APT20M45SVFR(G)

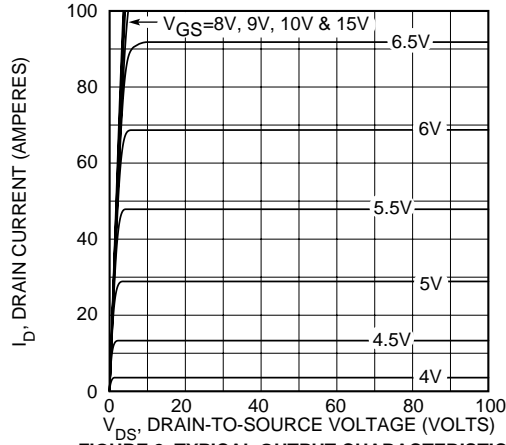


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

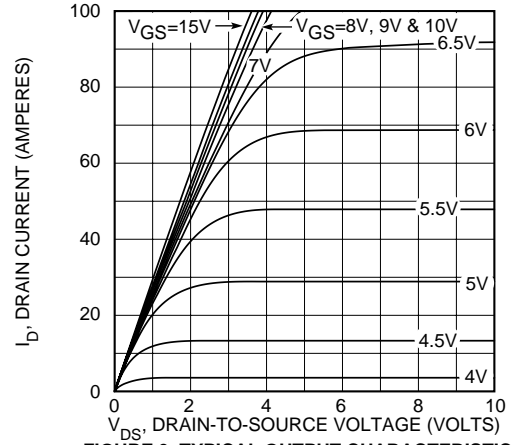


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

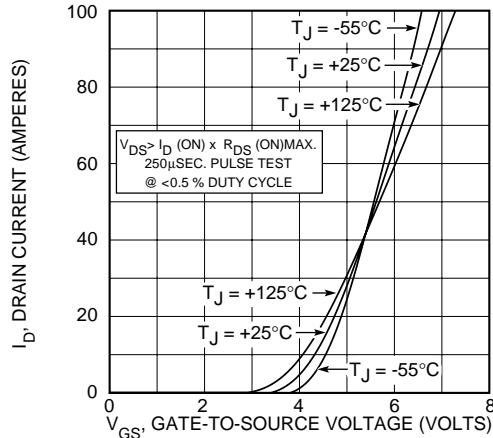


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

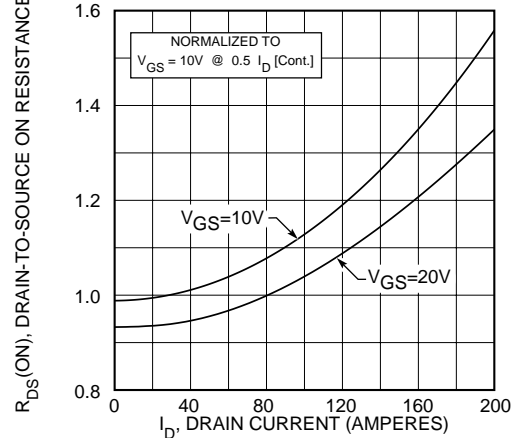


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

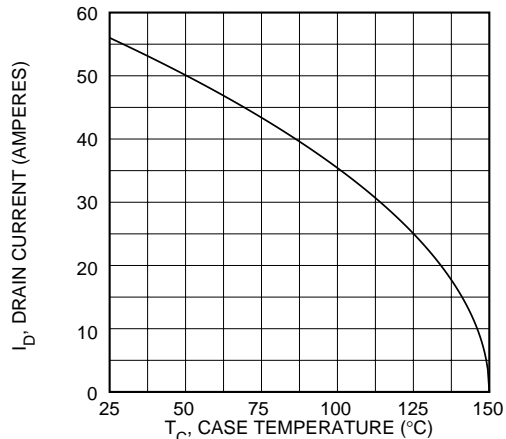


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

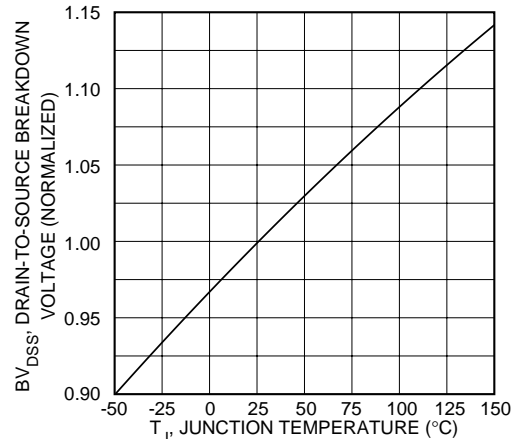


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

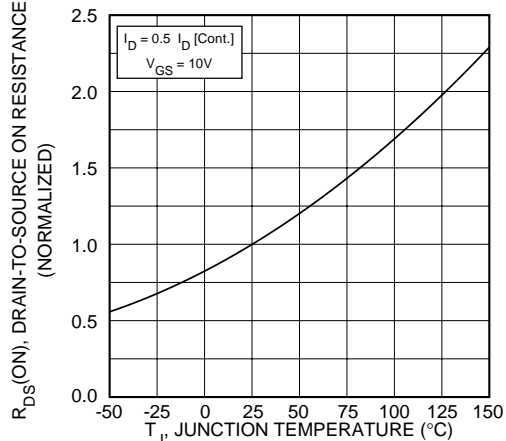


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

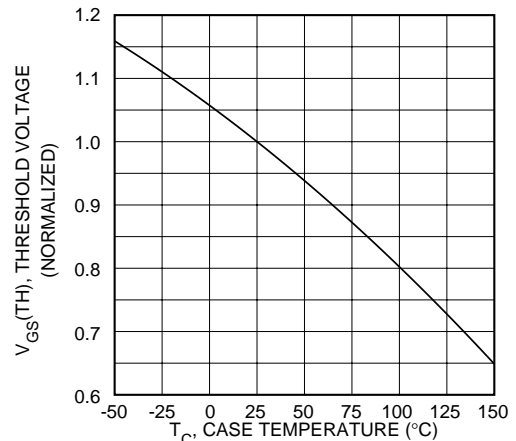


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

APT20M45SVFR(G)

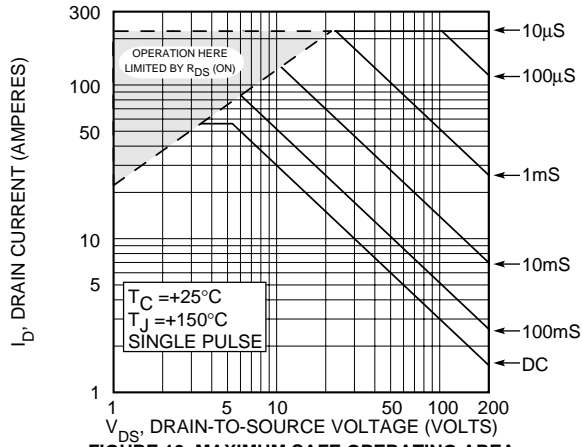


FIGURE 10, MAXIMUM SAFE OPERATING AREA

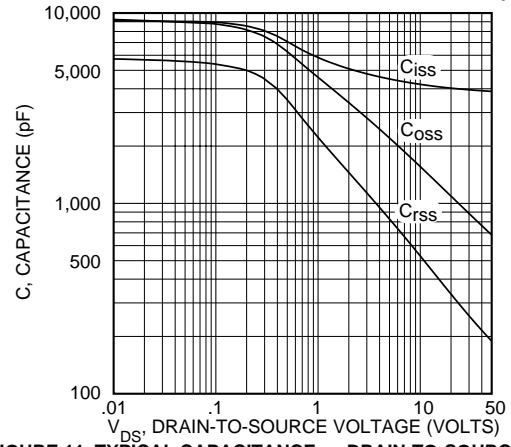


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

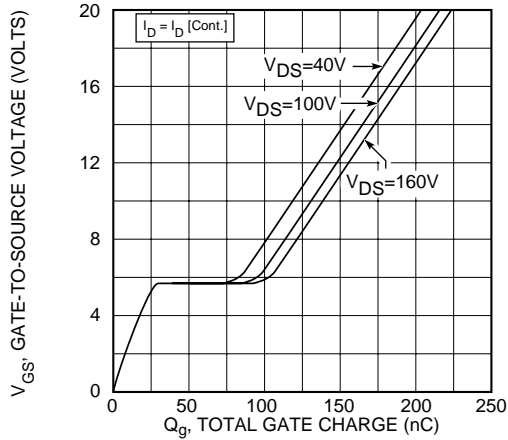


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

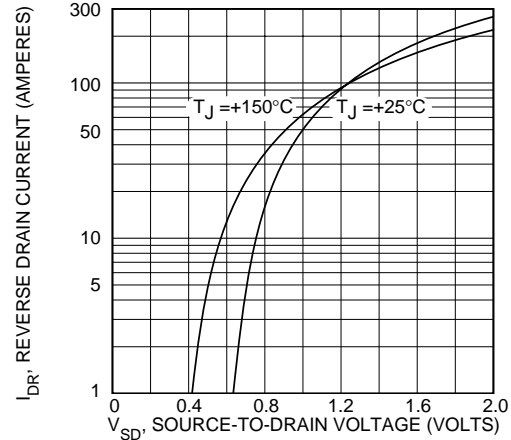


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

D³PAK Package Outline

e3 100% Sn Plated

