MP2238

High-Efficiency, 8A, 18V, Synchronous Step-Down Converter

DESCRIPTION

The MP2238 is a high frequency, synchronous, rectified, step-down switch-mode converter. It offers a fully integrated solution to achieve an 8A continuous output current with excellent load and line regulation over a wide input supply range.

Constant-on-time (COT) control operation provides fast transient response. Full protection features include hiccup over-current protection and thermal shutdown.

The MP2238 requires a minimal number of readily available, standard, external components with a space-saving 12-pin QFN 2mmx3mm package.

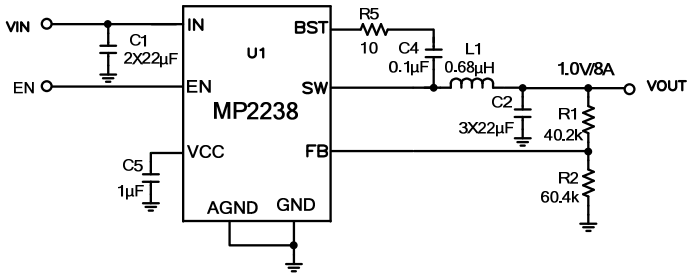
FEATURES

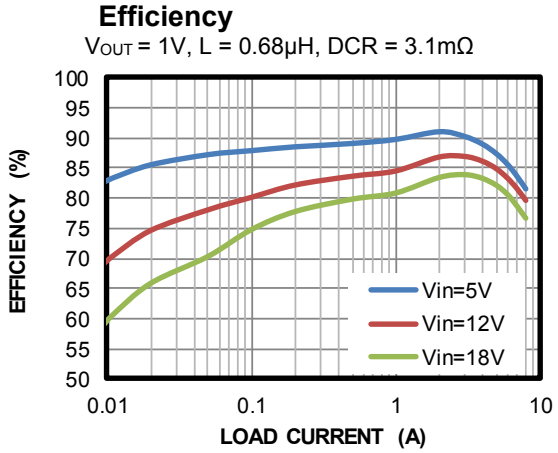
- Wide 4.2V to 18V Operating Input Range
- 8A Continuous Output Current
- 22mΩ/10mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Default 600mV Reference Voltage
- Adjustable Output Voltage
- 600kHz Switching Frequency
- Ton Extension
- Hiccup OCP Protection
- Thermal Shutdown Protection
- Available in a 12-Pin QFN 2mmx3mm Package

APPLICATIONS

- Flat-Panel Television and Monitors
- Digital TV Power Supply
- Digital Set-Top Boxes
- Distributed Power Systems
- General Consumer

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2238GD	QFN-12 (2mmx3mm)	*See Below*

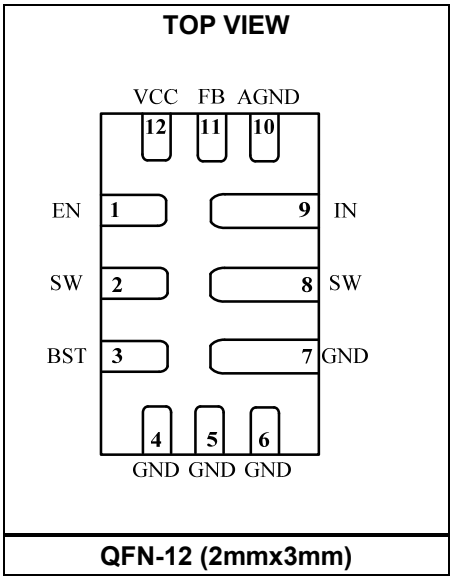
* For Tape & Reel, add suffix –Z (e.g. MP2238GD–Z).

TOP MARKING

BGB
YWW
LLL

BGB: Product code of MP2238GD
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-12 (2mmx3mm)

PIN FUNCTIONS

PIN #	Name	Description
1	EN	**Enable pin.** Pull EN high to enable the MP2238. EN has a 2MΩ pull-down resistor to GND.
2,8	SW	**Switch output.** Connect using a wide PCB trace.
3	BST	**Bootstrap.** Requires a 0.1µF capacitor between SW and BST to form a floating supply across the high-side switch driver.
4,5,6,7	GND	**System power ground.** Reference ground of the regulated output voltage. Requires special consideration during PCB layout. Connect to ground plane with copper traces and vias.
9	IN	**Supply voltage.** The MP2238 operates from a 4.2V to 18V input rail. Requires a ceramic capacitor to decouple the input rail. Connect using a wide PCB trace.
10	AGND	**Analog ground.** Connect AGND to GND.
11	FB	**Feedback.** Connect to the tap of an external resistor divider from output to GND to set the output voltage.
12	VCC	**Internal bias supply.** Decouple with a 1µF capacitor. The VCC capacitor should be placed as close as possible to VCC and GND.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 20V
V_{SW}..... -0.3V (-6.5V for <10ns) to V_{IN} + 0.7V (25V for <25ns)
V_{BST}..... V_{SW} + 4V
V_{EN}..... 20V
All other pins..... -0.3V to 4V
Continuous power dissipation (T_A = +25°C) (2)(5)
QFN-12 (2mmx3mm)..... 3.6W
Junction temperature.....150°C
Lead temperature..... 260°C
Storage temperature..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN})..... 4.2V to 18V
Output voltage (V_{OUT})..... 0.6V to 12V or V_{IN}*D_{MAX} (4)
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance

QFN-12 (2mmx3mm)	***θ_{JA}***	***θ_{JC}***
EV2238-D-00A (5)	34	9 °C/W
JESD51-7 (6)	65	13 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) For more information on D_{MAX}, please see the Low-Dropout Operation section on page 13.
5) Measured on EV2238-D-00A, 4-layer PCB.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (7), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V, T_J = 25°C			1	μA
Supply current (quiescent)	I_q	V_{FB} = 0.63V, PFM mode		150	210	μA
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 3.3V		22		mΩ
LS switch on resistance	LS_{RDS-ON}			10		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V, T_J = 25°C			1	μA
Low-side valley current limit	I_{LIMIT_L}		8	9.5		A
Low-side ZCD threshold	I_{ZCD}			50		mA
Switching frequency	f_{SW1}	V_{IN} = 12V, V_{OUT} = 3.3V	480	600	720	kHz
Minimum off time (8)	T_{OFF_MIN}			170		ns
Minimum on time (8)	t_{ON_MIN}			70		ns
Reference voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	mV
FB pin current	I_{FB}	V_{FB} = 0.63V		10	50	nA
EN rising threshold	V_{EN_RISING}		1.12	1.2	1.28	V
EN hysteresis	V_{EN_HYS}			200		mV
EN to GND pull-down resistor	R_{EN}	V_{EN} = 2V		2		MΩ
VIN under-voltage lockout threshold rising	$INUV_{Vth}$		3.55	3.85	4.15	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			400		mV
VCC regulator	V_{CC}	I_{CC} = 5mA		3.5		V
UVP1 threshold (8)	UV_{TH1}	Hiccup entry		80%		V_{REF}
Soft-start time	T_{SS}	T_J = 25°C, from 10% to 90%	0.5	1	1.5	ms
Thermal shutdown (8)	T_{TSD}			150		°C
Thermal hysteresis (8)	T_{TSD_HYS}			20		°C

Notes:

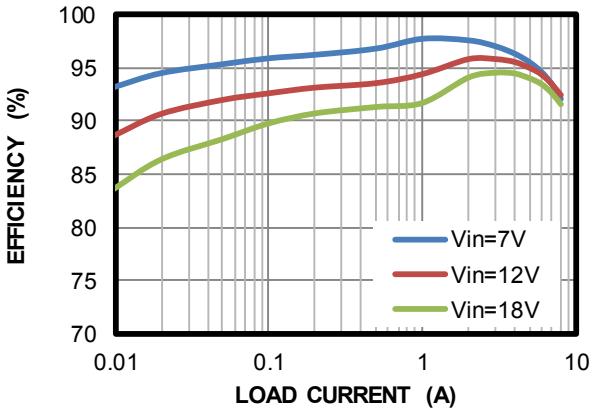
7) Not tested in production. Guaranteed by over-temperature correlation.

8) Guaranteed by design and engineering sample characterization.

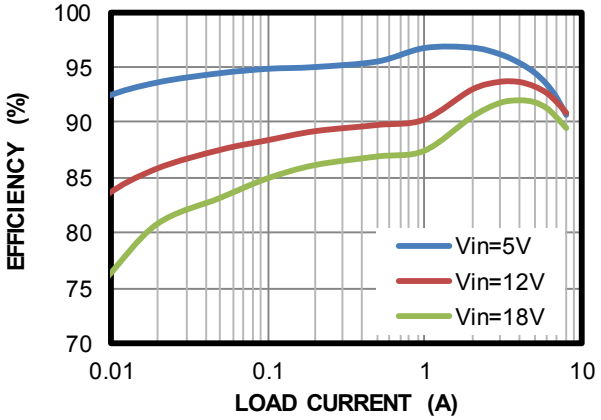
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1V, L = 0.68µH, T_A = 25°C, unless otherwise noted.

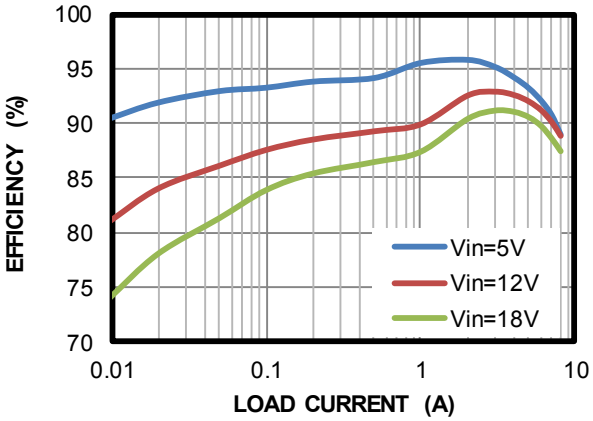
Efficiency
V_{OUT} = 5V, L = 2.2µH, DCR = 11.4mΩ



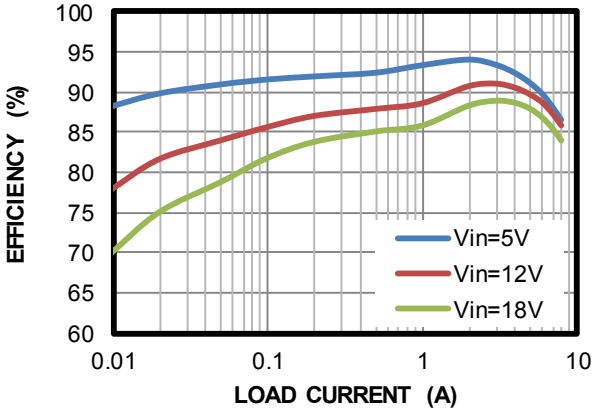
Efficiency
V_{OUT} = 3.3V, L = 1.5µH, DCR = 4.3mΩ



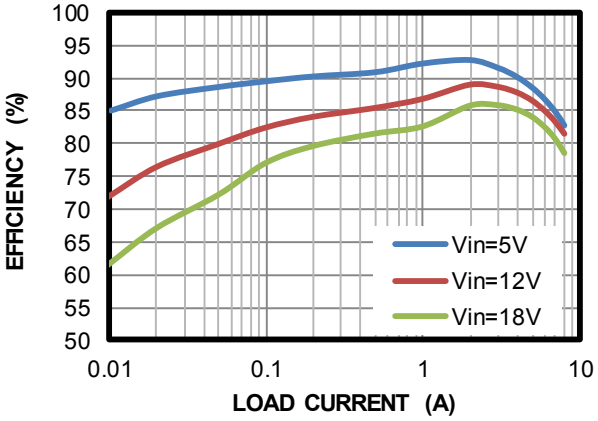
Efficiency
V_{OUT} = 2.5V, L = 1.5µH, DCR = 4.3mΩ



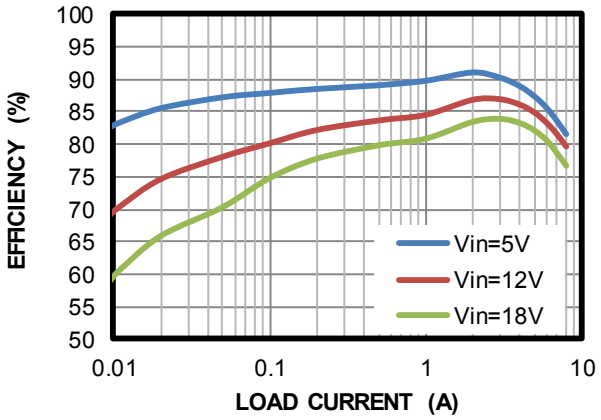
Efficiency
V_{OUT} = 1.8V, L = 1µH, DCR = 4.6mΩ



Efficiency
V_{OUT} = 1.2V, L = 1µH, DCR = 4.6mΩ



Efficiency
V_{OUT} = 1V, L = 0.68µH, DCR = 3.1mΩ

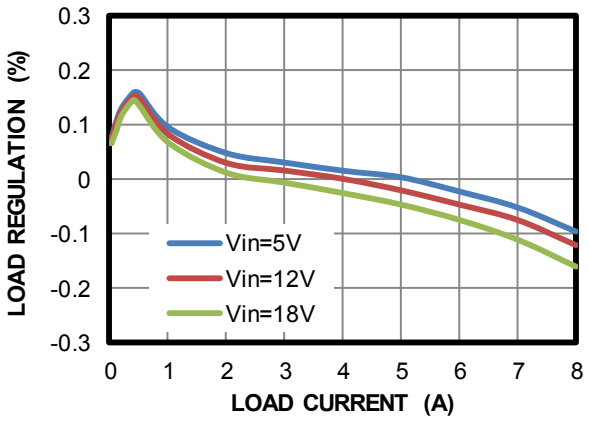


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN} = 12V, V_{OUT} = 1V, L = 0.68µH, T_A = 25°C, unless otherwise noted.

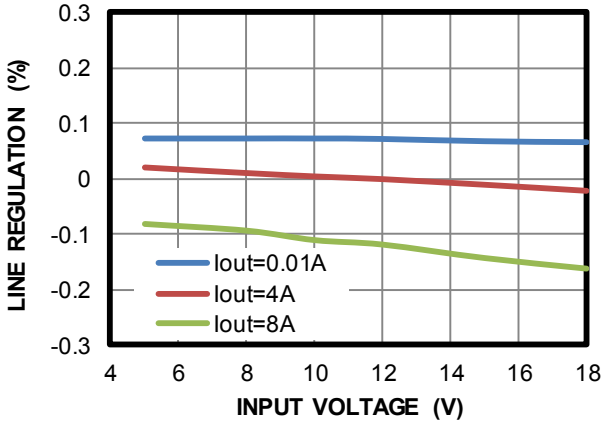
Load Regulation

I_{OUT} = 0.01A to 8A



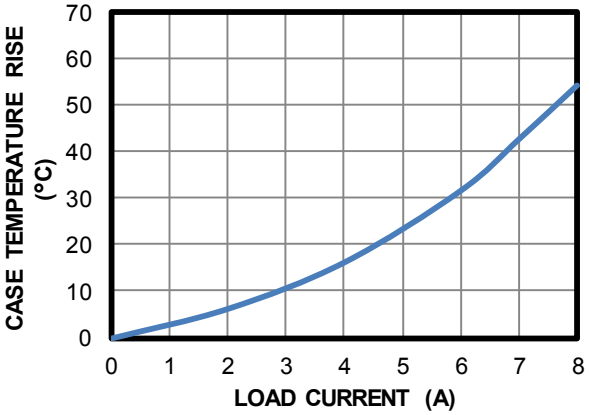
Line Regulation

V_{IN} = 5V to 18V



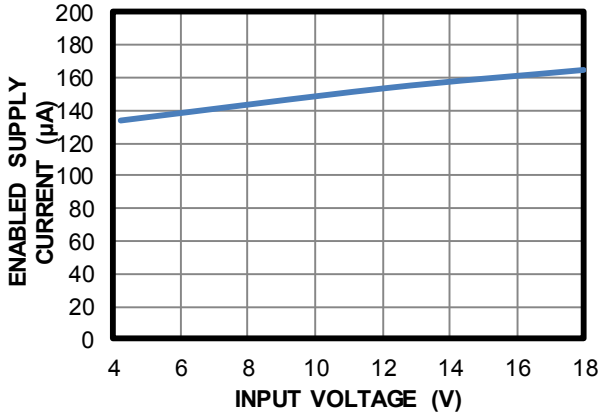
Case Temperature Rise vs. Load Current

V_{IN} = 12V, V_{OUT} = 1V



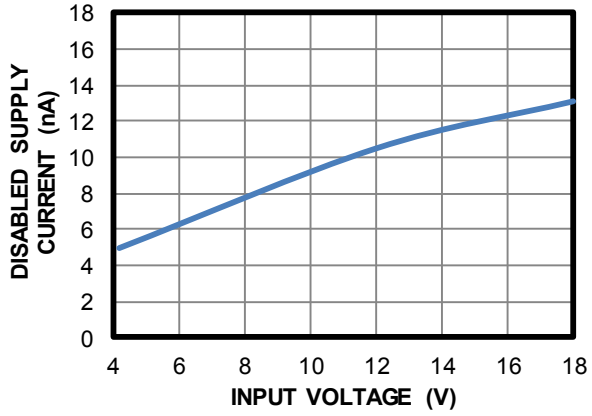
Enabled Supply Current vs. Input Voltage

V_{EN} = 2V, V_{FB} = 0.63V

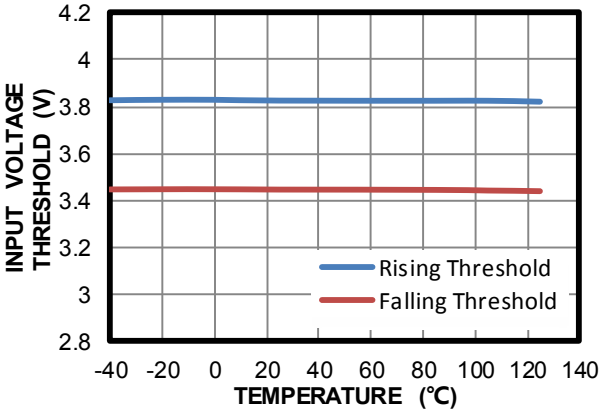


Disabled Supply Current vs. Input Voltage

V_{EN} = 0V



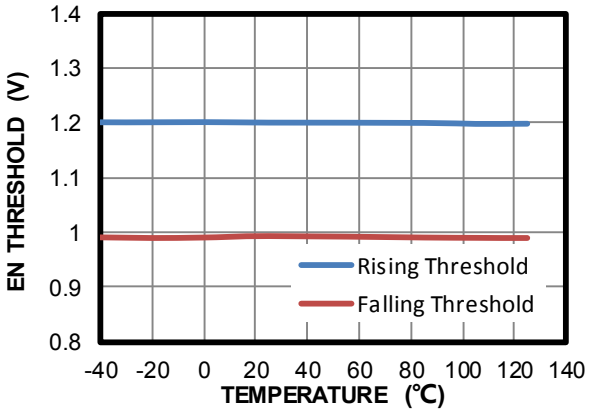
Input Voltage Threshold vs. Temperature



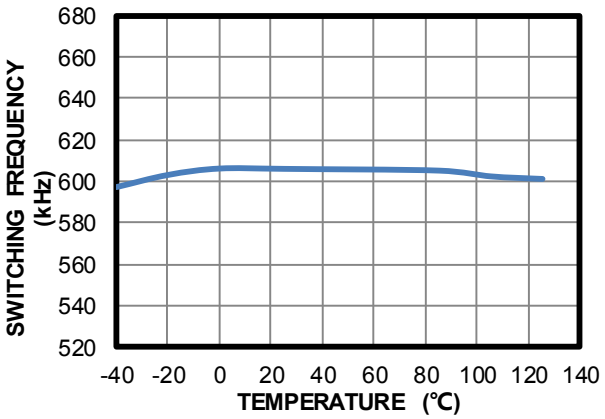
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1V, L = 0.68µH, T_A = 25°C, unless otherwise noted.

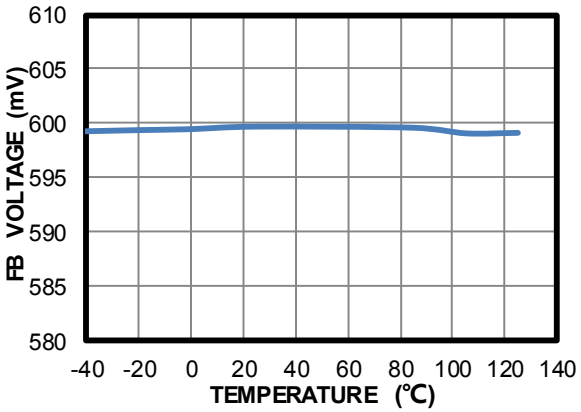
EN Threshold vs. Temperature



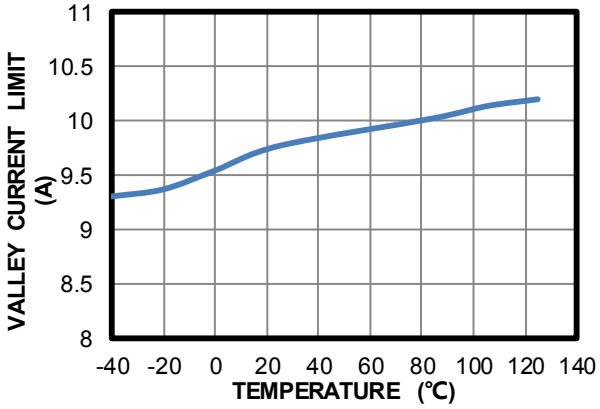
Switching Frequency vs. Temperature



FB Voltage vs. Temperature



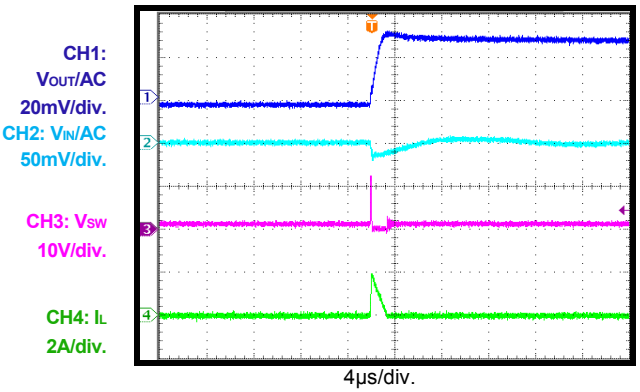
Valley Current Limit vs. Temperature



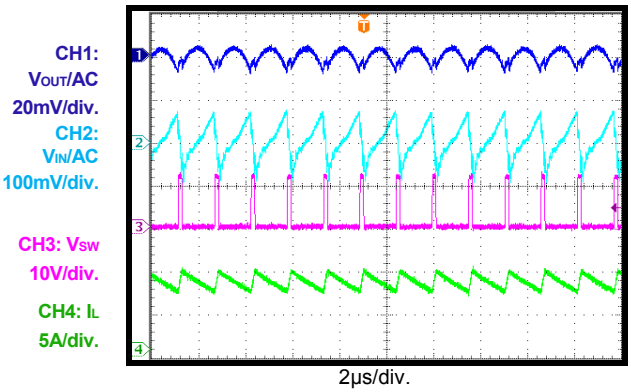
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1V, L = 0.68µH, T_A = 25°C, unless otherwise noted.

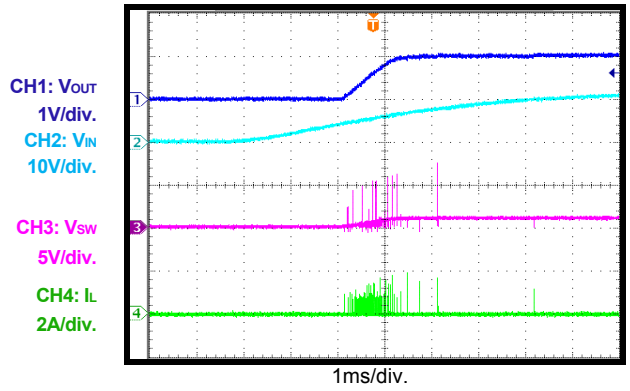
Input / Output Ripple
I_{OUT} = 0A



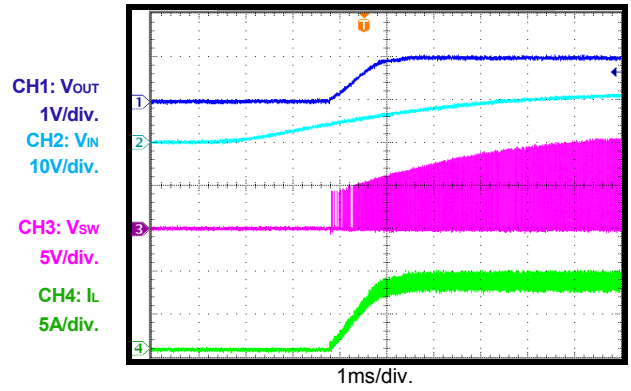
Input / Output Ripple
I_{OUT} = 8A



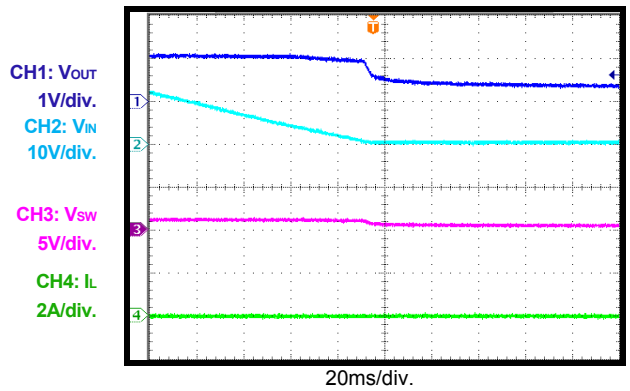
Start-Up through Input Voltage
I_{OUT} = 0A



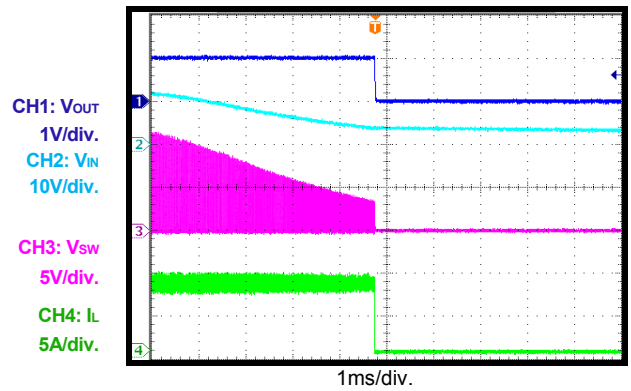
Start-Up through Input Voltage
I_{OUT} = 8A



Shutdown through Input Voltage
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 8A

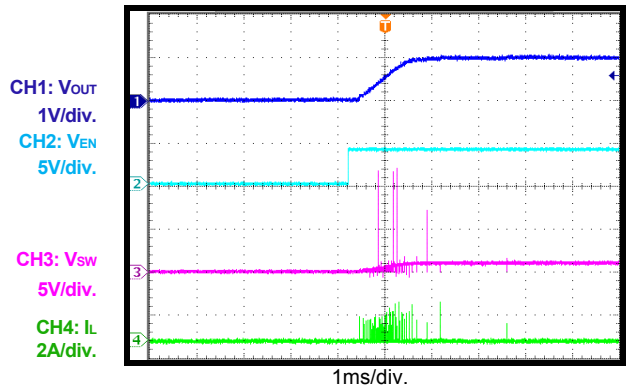


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1V, L = 0.68µH, T_A = 25°C, unless otherwise noted.

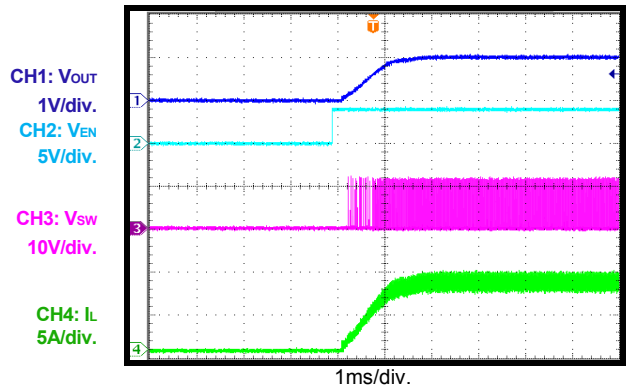
Start-Up through Enable

I_{OUT} = 0A



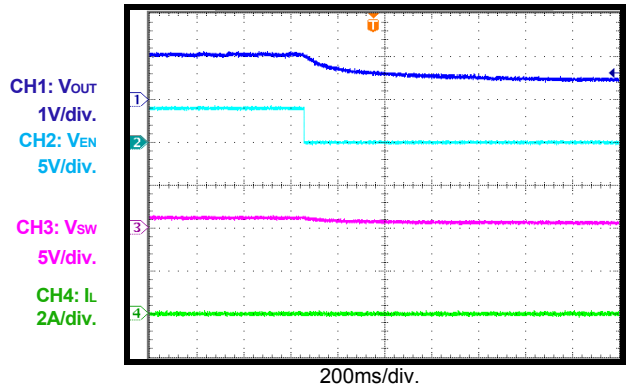
Start-Up through Enable

I_{OUT} = 8A



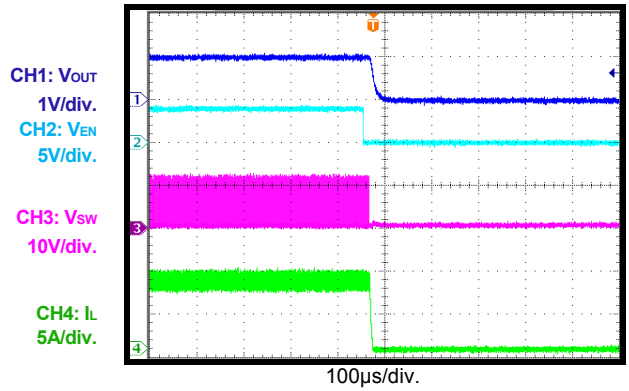
Shutdown through Enable

I_{OUT} = 0A

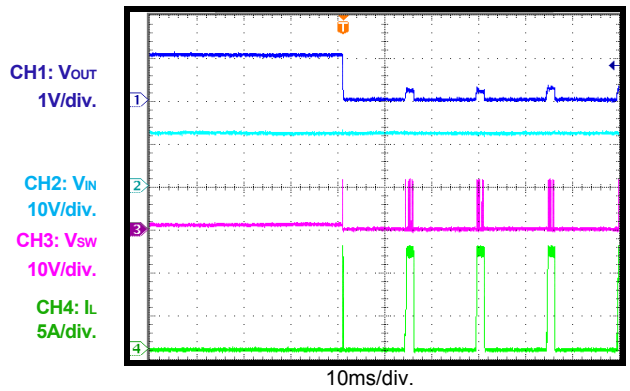


Shutdown through Enable

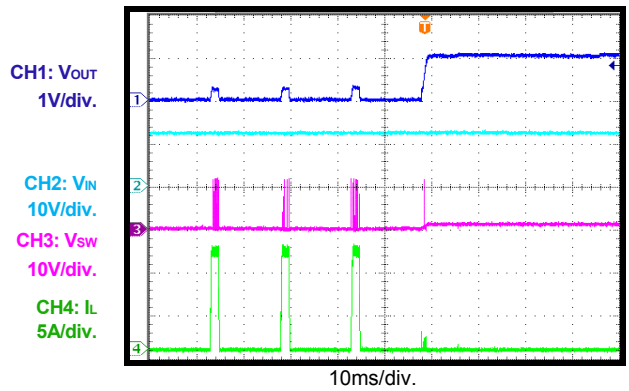
I_{OUT} = 8A



Short-Circuit Entry



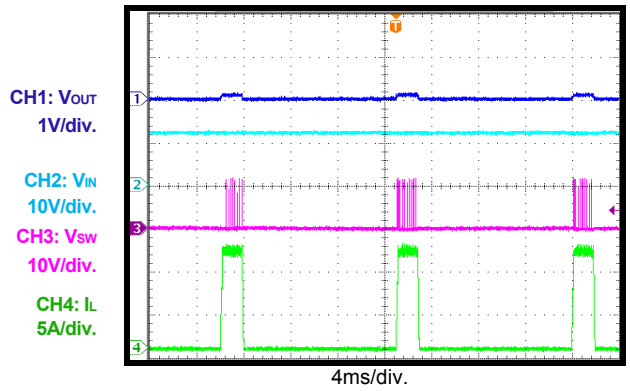
Short-Circuit Recovery



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

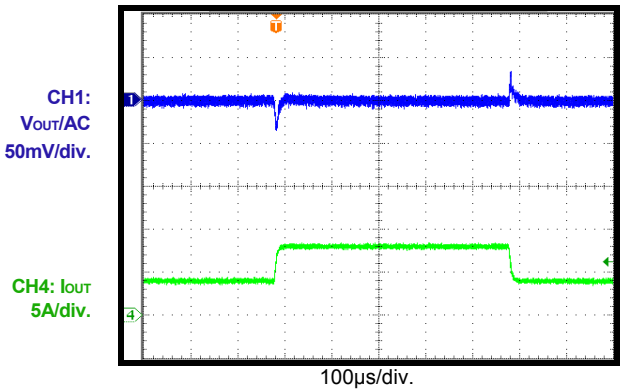
Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1V, L = 0.68µH, T_A = 25°C, unless otherwise noted.

Short-Circuit Steady



Transient Response

I_{OUT} = 4A to 8A



FUNCTIONAL BLOCK DIAGRAM

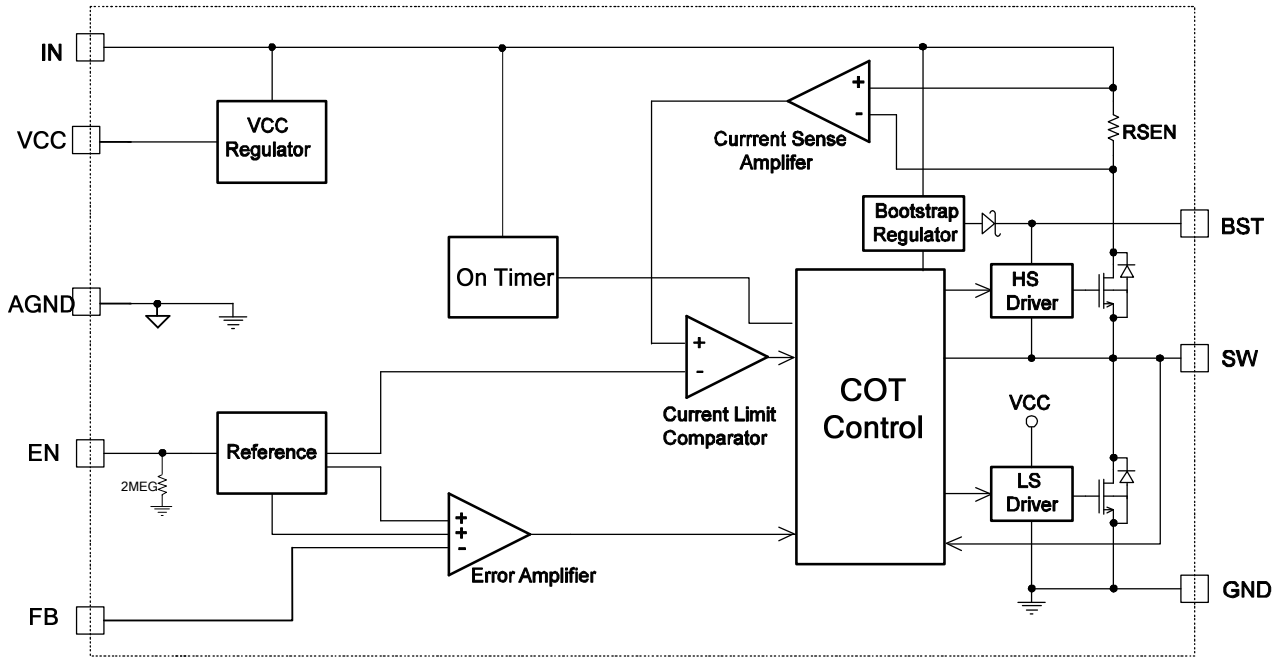


Figure 1: Functional Block Diagram

OPERATION

PWM Operation

The MP2238 is a fully integrated, synchronous, rectified, step-down switch converter. The device uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. Figure 2 shows the simplified ramp compensation block in the MP2238. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage (V_{RAMP}) is lower than the error amplifier output voltage (V_{EAO}), which indicates insufficient output voltage. The on period is determined by both the output voltage and input voltage, to ensure the switching frequency is fairly constant over a wide input voltage range.

After the on period elapses, the HS-FET enters the off state. By cycling the HS-FET between the on and off states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss.

Shoot-through occurs when both the HS-FET and LS-FET are turned on at the same time, causing a dead short between the input and GND. Shoot-through dramatically reduces efficiency, and the MP2238 avoids this by internally generating a dead time (DT) between when the HS-FET turns off and the LS-FET turns on, or vice versa. The device enters heavy-load operation or light-load operation depending on the amplitude of the output current.

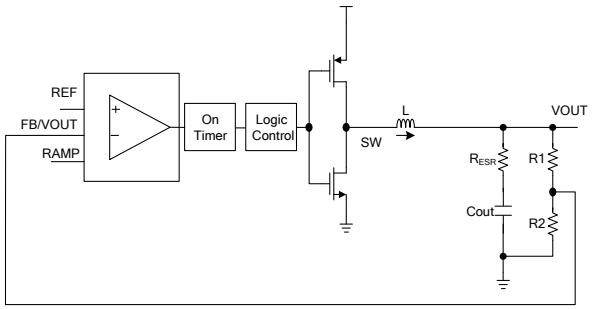


Figure 2: Simplified Compensation Block

Light-Load Operation

When the MP2238 works in PFM and during light-load operation, the switching frequency automatically reduces to maintain high efficiency, and the inductor current drops near zero (see Figure 3). When the inductor current reaches zero, the LS-FET driver goes into tri-state (high Z). The output capacitors discharge slowly to GND through the LS-FET, R1, and R2. This operation greatly improves device efficiency when the output current is low.

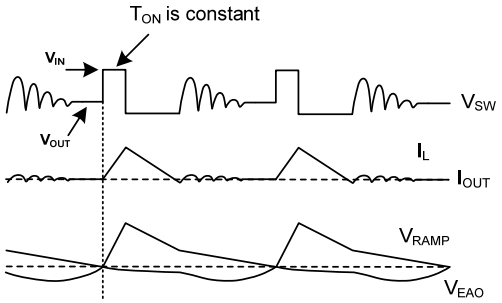


Figure 3: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does during heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the current modulator regulates shorter time periods, and the HS-FET turns on more frequently. The switching frequency then increases in turn. The output current reaches the critical level when the current modulator time is zero, and can be determined using Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device reverts to PWM mode once the output current exceeds the critical level. Then the switching frequency stays fairly constant over the output current range.

Error Amplifier

The error amplifier compares the FB voltage against the internal 0.6V reference (REF) and outputs the PWM modulation signal. The optimized internal ramp compensation minimizes the external component count and simplifies the control loop design.

Enable

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive it low to turn it off. An internal 2MΩ resistor is connected from EN to ground. EN can function with a 20V input voltage, which allows EN to be connected directly to V_{IN} for automatic start-up.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2238 UVLO comparator monitors the input voltage. The part is active when the input voltage exceeds the UVLO rising threshold.

Soft Start and Pre-Bias Start-Up

Soft start prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to internal VCC. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, REF takes over.

The soft-start time is internally set to 1ms (V_{OUT} from 10% to 90%). If the output of the MP2238 is pre-biased to a certain voltage during start-up, the IC will disable the switching of both the high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at FB.

Low Dropout Operation

To improve dropout, the MP2238 is designed to extend the on time when the duty cycle is over 85% of its typical value. The HS-FET on time then extends and the frequency drops. The typical minimum frequency is 260kHz. When the frequency drops to 260kHz, it cannot reduce anymore and the HS-FET off time starts to decrease. The duty cycle reaches D_{MAX} when the off time is down to its minimum value. If the input voltage continues to drop, the MP2238 works at max duty cycle and the output voltage drops.

The typical max duty cycle (D_{MAX}) is determined with Equation (2):

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{SW\_MIN} \quad (2)$$

Where T_{OFF_MIN} = 170ns and f_{SW_MIN} = 260kHz.

Over-Current Protection and Hiccup

The MP2238 has cycle-by-cycle over-current limiting control. The current-limit circuit employs a low-side valley current-sensing algorithm. The part uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element for the valley current limit. During the LS-FET turn-on, the inductor current is monitored by the voltage between GND and SW. GND is used as the positive current-sensing node, and should be connected to the source terminal of the bottom MOSFET. The PWM is not allowed to initiate a new cycle before the inductor current falls to the valley threshold.

After the MP2238 reaches the cycle-by-cycle over-current limit, the output voltage drops until VOUT is below the under-voltage (UV) threshold. There are two UV thresholds: 80% UV1 and 60% UV2. Once UV1 and OC are both triggered, the MP2238 waits 30 cycles. If OC exits after 31 cycles, the chip enters hiccup mode to restart the part periodically. If UV2 and OC are triggered, the MP2238 enters hiccup mode after 3 cycles. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and to protect the regulator. The MP2238 exits hiccup mode once it is no longer in an over-current condition.

Thermal Shutdown

Thermal shutdown prevents the MP2238 from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 150°C, it shuts down the whole chip. When the temperature is less than its lower threshold, typically 130°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 1.2V, with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1, and C2 (see Figure 4). If (V_{IN} - V_{SW}) exceeds 3.3V, U1 will regulate M1 to maintain a 3.3V BST voltage across C4.

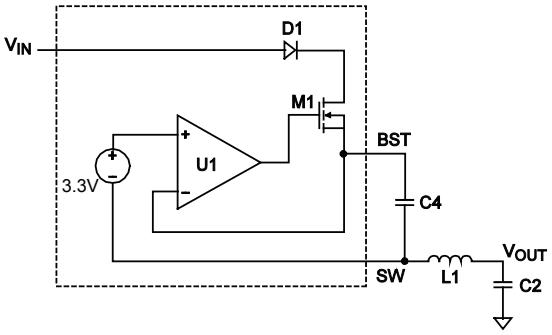


Figure 4: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked to avoid any fault triggering, and then the internal supply rail is pulled down.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider can set the output voltage through FB. Choose R1 and R2 using Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1} \quad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	40.2	60.4
1.2	40.2	40.2
1.8	100	49.9
2.5	100	31.6
3.3	100	22.1
5	100	13.7

Selecting the Inductor

Use a 0.47μH to 10μH inductor with a DC current rating at least 25% percent higher than the maximum load current for most applications. For highest efficiency, use an inductor with a DC resistance of less than 15mΩ. For most designs, the inductance value can be derived using Equation (4):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (4)$$

Where ΔI_L is the inductor ripple current.

The inductor ripple current should be approximately 30% of the maximum load current. The maximum inductor peak current is calculated with Equation (5):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (5)$$

Use a larger inductor for improved efficiency under light-load conditions (below 100mA).

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended for best results because of their low ESR and small temperature coefficients. For most applications, use two 22μF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, determined using Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 1μF) placed as close to the IC as possible. When using ceramic capacitors, ensure they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The traditional COT control scheme is intrinsically unstable if the output capacitor's ESR is not large enough as an effective current-sense resistor. The MP2238 has built-in internal ramp compensation to ensure the system is stable without the output capacitor's ESR. The pure ceramic capacitor solution can significantly reduce the output ripple, total BOM cost, and the board area.

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated using Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (9)$$

Where L_1 is the inductor value and R_{ESR} is the ESR value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2238 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator if V_{IN} is below 5V, V_{OUT} is 3.3V, and the duty cycle is high, which can be determined using Equation (12):

$$D = \frac{V_{OUT}}{V_{IN}} > 65\% \quad (12)$$

In these cases, add an external BST diode from VCC to BST see Figure 5).

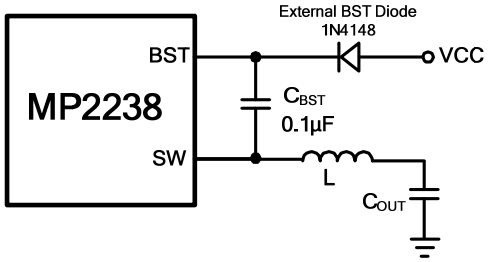


Figure 5: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is 1N4148, and the recommended BST capacitor value is 0.1µF.

PCB Layout Guidelines [9]

PCB layout is very important for stable operation. A 4-layer board is recommended for better thermal performance. Figure 6 and Figure 7 show the top and bottom layers (Inner 1 and Inner 2 are GND). For best results, refer to Figure 6 and Figure 7, and follow the guidelines below:

1. Connect the input ground to GND using the shortest and widest trace possible.
2. Connect the input capacitor to IN using the shortest and widest trace possible.
3. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4. Route SW away from sensitive analog areas, such as VOUT.
5. Connect AGND to PGND using the shortest and widest trace possible.

Notes:

9) The recommended layout is based on the Figure 8 in Typical Application Circuit section.

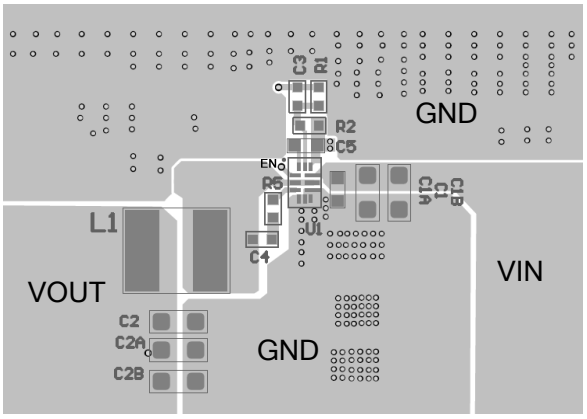


Figure 6: Recommended PCB Layout, Top Layer

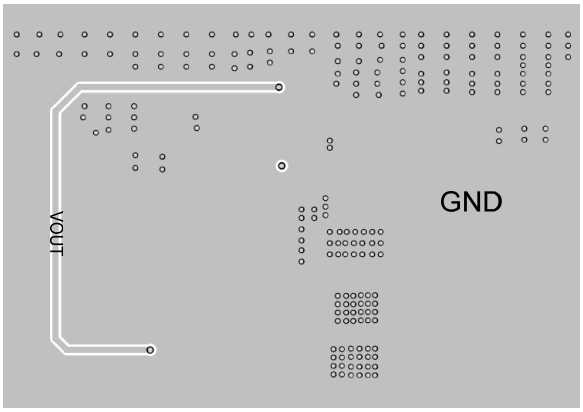


Figure 7: Recommended PCB Layout, Bottom Layer

Design Example

Table 2 is a design example following the application guidelines for the following specifications:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	1V
I_{OUT}	8A

Figure 8 shows a detailed application schematic. See the Typical Performance Characteristics section on pages 5 to 10 for the typical performance and circuit waveforms. For more device applications, see the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS

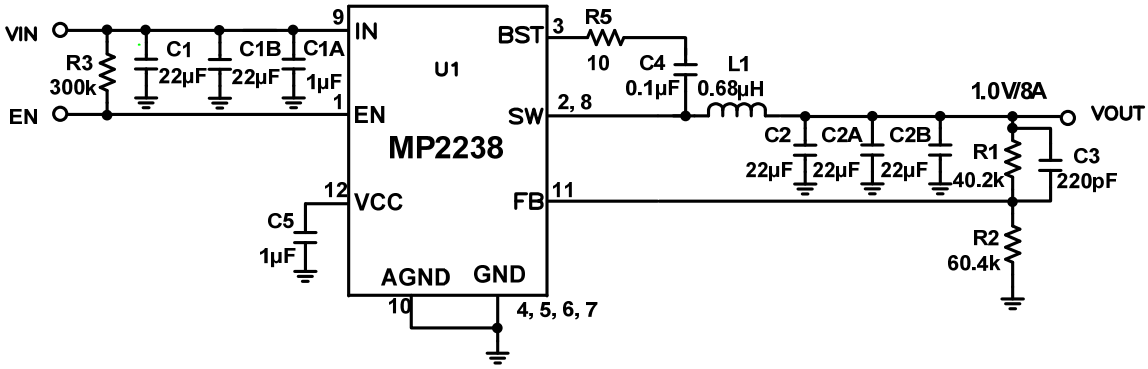


Figure 8: V_{IN} = 12V, Output = 1.0V/8A

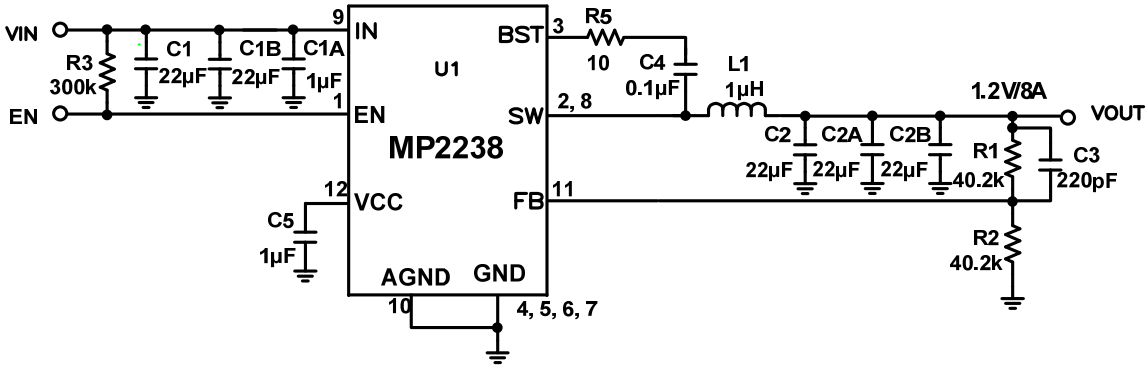


Figure 9: V_{IN} = 12V, Output = 1.2V/8A

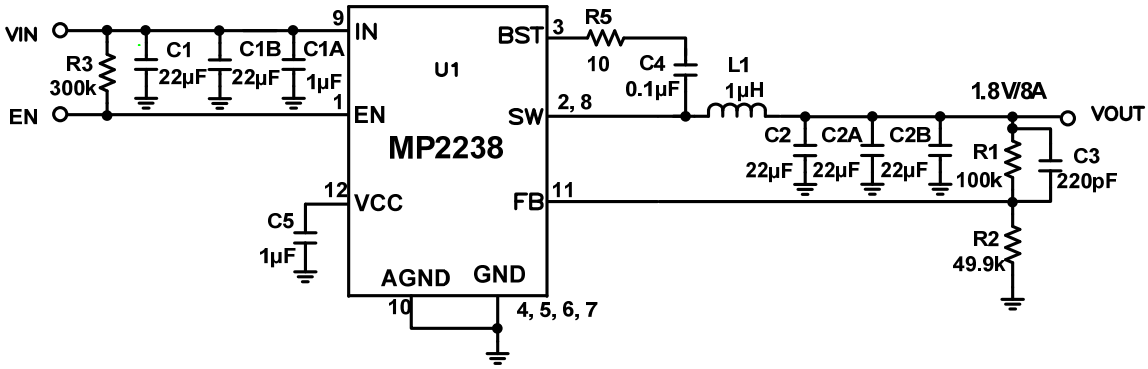


Figure 10: V_{IN} = 12V, Output = 1.8V/8A

TYPICAL APPLICATION CIRCUITS *(continued)*

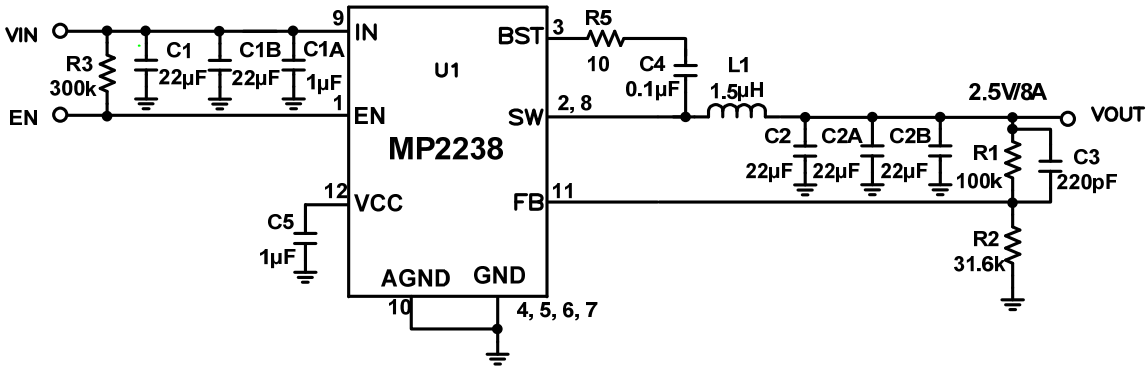


Figure 11: V_{IN} = 12V, Output = 2.5V/8A

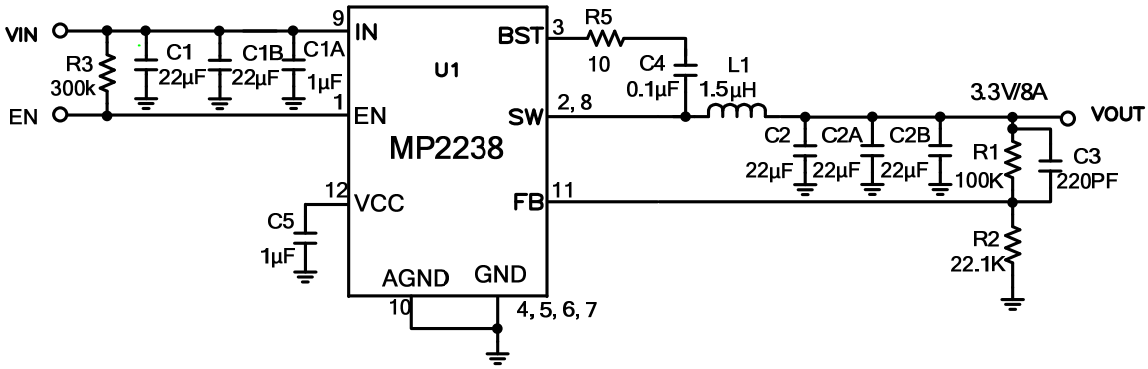


Figure 12: V_{IN} = 12V, Output = 3.3V/8A

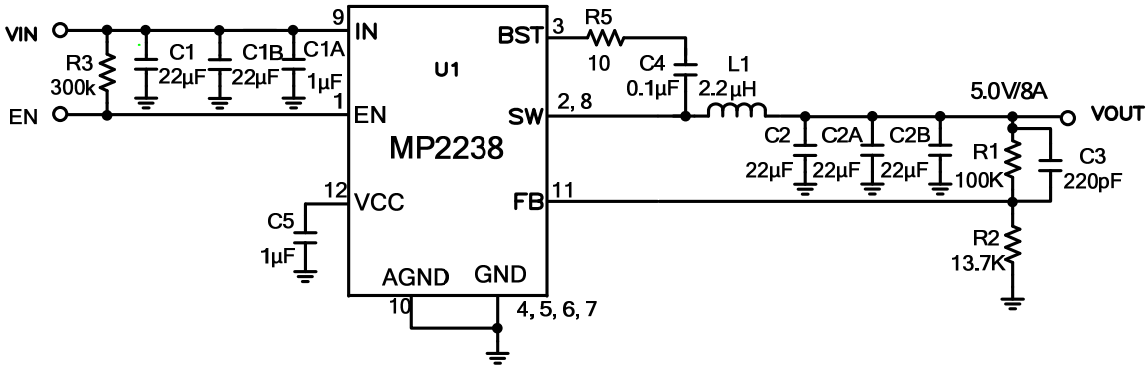
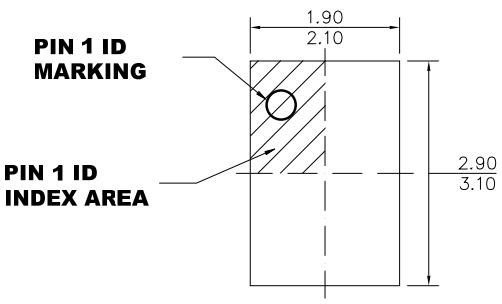


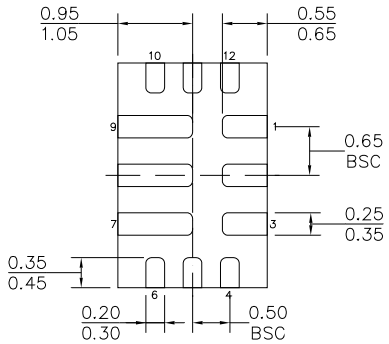
Figure 13: V_{IN} = 12V, Output = 5V/8A

PACKAGE INFORMATION

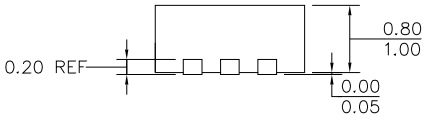
QFN-12 (2mmx3mm)



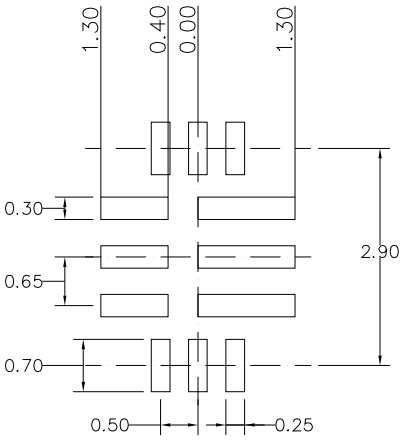
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.