BURR-BROWN®

4127

LOGARITHMIC AMPLIFIER

FEATURES

- **ACCEPTS INPUT VOLTAGES OR CURRENTS OF EITHER POLARITY**
- **WIDE INPUT DYNAMIC RANGE**
  6 Decades of Current
  4 Decades of Voltage
- **VERSATILE**
  Log, Antilog, and Log Ratio Capability

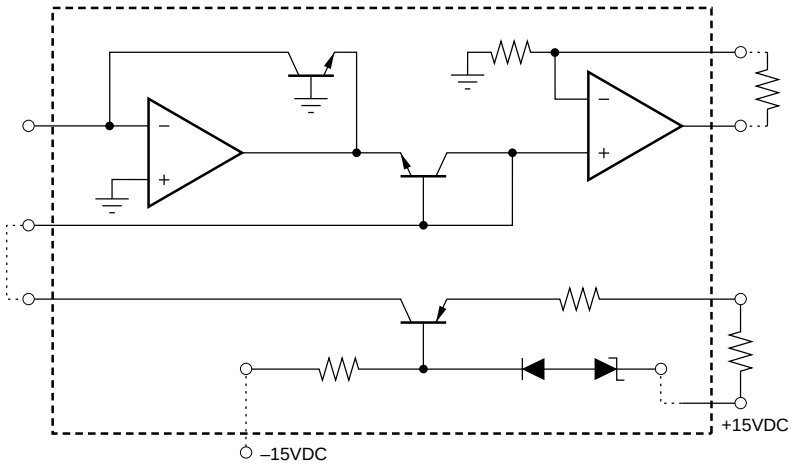
DESCRIPTION

Packaged in a ceramic double wide DIP, the 4127 is the first hybrid logarithmic amplifier that accepts signals of either polarity from current or voltage sources. A special purpose monolithic chip, developed specifically for logarithmic conversions, functions accurately for up to six decades of input current and four decades of input voltage. In addition, a current inverter and a precise internal reference allow pin programming of the 4127 as a logarithmic, log ratio, or antilog amplifier.

To further increase its versatility and reduce your system cost, the 4127 has an uncommitted operational amplifier in its package that can be used as a buffer, inverter, filter, or gain element.

The 4127 is available with initial accuracies (log conformity) of 0.5% and 1.0%, and operates over an ambient temperature range of –10°C to +70°C.

With its versatility and high performance, the 4127 has many applications in signal compression, transducer linearization, and phototube buffering. Manufacturers of medical equipment, analytical instruments, and process control instrumentation will find the 4127 a low cost solution to many signal processing problems.



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SPECIFICATIONS

ELECTRICAL

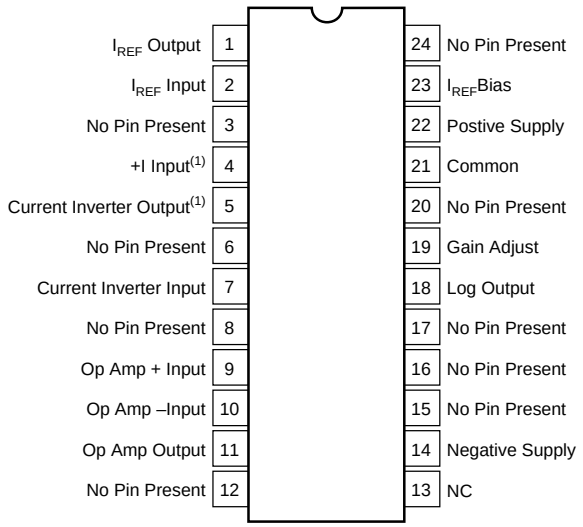
Typical Specifications at +25°C with rated supplies, unless otherwise noted.

MODEL	4127KG	4127JG
ACCURACY[1], % of FSR		
Current Source Input: 1nA to 1mA	0.5% max	1% max
Voltage Input: 1mV to 10V	0.5% max	1% max
INPUT		
Current Source Input, Pin 4	+1nA to +1mA	
Current Source Input, Pin 7	–1nA to –1mA	
Reference Current Input, Pin 2	+1µA to +1mA	
Absolute Maximum Inputs	±10mA or ±Supply Volts	
OUTPUT		
Voltage	±10V	
Current	±5mA	
Impedance	10Ω	
FREQUENCY RESPONSE		
–3dB Small Signal at Current Input		
of 100µA	90kHz	
of 10µA	50kHz	
of 1µA	5kHz	
of 100nA	250Hz	
of 10nA	80Hz	
Step Response to within ±1% of		
Final Value (I_R = 1µA, A = 5)	10ms	
STABILITY		
Scale Factor Drift (ΔA/°C)	±0.0005A/°C	
Reference Current Drift (ΔI_R/°C)	±0.001 I_R/°C for $I_R \geq$ 1µA	
	±0.003 I_R/°C for 400nA < I_R < 1µA	
Input Offset Current Drift (ΔI_S/°C)	10pA at +25°C, Doubles Every 10°C	
Input Offset Voltage Drift	±10µV/°C	
Accuracy vs Supply Variation		
Reference Current	±0.001I_R/V	
Input Offset Voltage	±300µV/V	
Input Noise - Current Input	1pA, rms, 10Hz to 10kHz	
Input Noise - Voltage Input	10µA, rms, 10Hz to 10kHz	
UNCOMMITTED OP AMP CHARACTERISTICS		
Input Offset Voltage	5mV	
Input Bias Current	40nA	
Input Impedance	1MΩ	
Large Signal Voltage Gain	85dB	
Output Current	5mA	
TEMPERATURE RANGE		
Specification	0°C to +60°C	
Operating	–10°C to +70°C	
Storage	–55°C to +125°C	
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltages	±15VDC	
Supply Voltage Range	±14VDC to ±16VDC	
Supply Current Drain		
at Quiescent, max	±20mA	
at Full Load, max	±26mA	

NOTE: (1) Log conformity at 25°C.

PIN CONFIGURATION

Top View



NOTE: (1) Pins 4 and 5 are internally connected.

PACKAGE INFORMATION

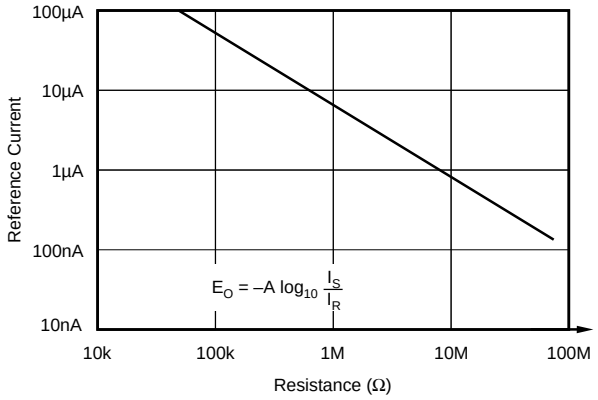
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
4127KG	24-Pin	075
4127JG	24-Pin	075

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

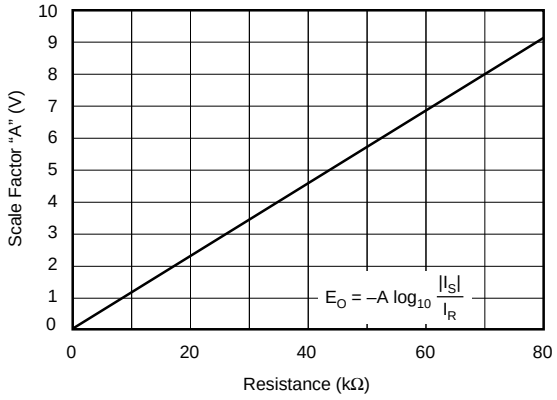
TYPICAL PERFORMANCE CURVES

At +25°C with rated supplies, unless otherwise noted.

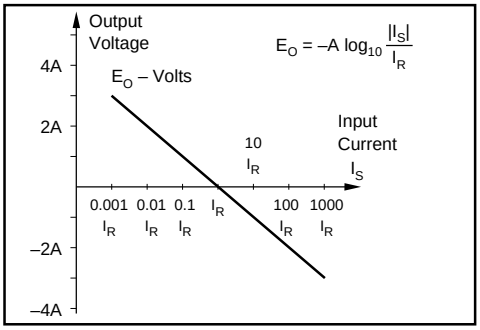
RELATIONSHIP OF REFERENCE CURRENT, I_R AND EXTERNAL RESISTOR, R_1



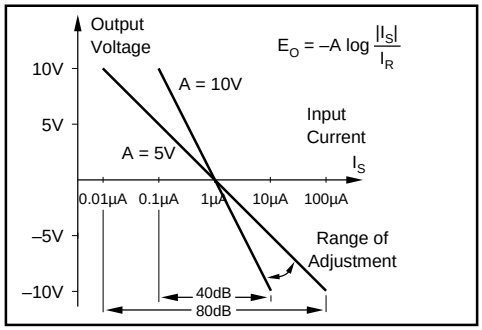
RELATIONSHIP OF SCALE FACTOR "A" TO GAIN SETTING RESISTOR, R_2



LOG RELATIONSHIP OF $\frac{|I_S|}{I_R}$ AND OUTPUT VOLTAGE IN TERMS OF "A"



RELATIONSHIP OF $\frac{|I_S|}{I_R}$ AND OUTPUT VOLTAGE For I_R = 1µA and A = 5V and 10V



DISCUSSION OF SPECIFICATIONS

ACCURACY

The deviation from the ideal output voltage defined as a percent of the full scale output voltage.

INPUT/OUTPUT RANGE

The log relationships of $-A \log \frac{I_S}{I_R}$ and $-A \log \frac{E_S}{I_R R}$ are subject to the constraints specified. The 4127 can be operated with inputs lower than those given, but the accuracy will be degraded.

FREQUENCY RESPONSE

The small-signal frequency response varies considerably with signal level and scaling, so the frequency response is specified under several different operating conditions.

STABILITY

The use of a monolithic transistor quad and low-drift amps minimizes drift, but some drift remains in the scale-factor, reference current, and input offset. Input offset consists of a bias current plus the op amp input voltage offset divided by the signal source resistance. Also, there is some slight drift in conformity to the log function and in output amplifier offset, but this is generally negligible.

THEORY OF OPERATION

The 4127 is a complete logarithmic amplifier that can be pin-programmed to accept input currents or voltages of either polarity. By making use of the internal current inverter, reference current generator, log ratio element, and uncommitted op amp, you can generate a variety of logarith-

mic functions, including the log ratio of two signals, the logarithm of an input signal, or the antilog of an input signal. The unique FET-input current-inverting element removes the polarity limitations present in most conventional log amplifiers.

Utilizing the inherent exponential characteristics of transistor functions, the 4127 calculates accurate log functions for input currents from 1nA to 1mA, or input voltages from 1mV to 10V. Carefully matched monolithic quad transistors and temperature sensitive gain elements are used to produce a log amplifier with excellent temperature characteristics.

A functional diagram of the 4127 circuit is shown in Figure 1. In addition to the basic log amplifier, the 4127 contains a separate internal current source, a current inverter, and an uncommitted operational amplifier. The current inverter accurately converts negative input current to a positive current of equal magnitude.

The 4127 is capable of accurately logging input current over a 120dB range, but to use this full range, good shielding practice must be followed. A current source input is, by definition, a high impedance source and is therefore subject to electrostatic pickup.

The input op amps, A_1 and A_3, have FET input stages for low noise and very-low input bias current. The op amp, A_1, will make the collector current of Q_1 equal to the signal input current I_S, and the collector current of Q_2 will be the reference input current I_R.

From the semiconductor junction characteristics, the base-to-emitter voltage will be:

$$V_{BE} \approx \frac{mKT}{q} \ell n \frac{I_C}{I_L},$$

where: I_C = Collector current
I_L = Reverse saturation current
q, m, K = Constants
T = Absolute temperature

$$\text{So } E_1 = -\frac{mKT_1}{q} \ell n \frac{I_S}{I_{L1}} \text{ and } E_2 - E_1 = \frac{mKT_2}{q} \ell n \frac{I_R}{I_{L2}}$$

If the transistors Q_1 and Q_2 are at the same temperature and have matched characteristics, then:

$$E_2 = \frac{mKT}{q} \left[\ell n \frac{I_R}{I_L} - \ell n \frac{I_S}{I_L} \right]$$

$$E_2 = \frac{-mKT}{q} \ell n \frac{I_S}{I_R}$$

The output op amp, A_2, provides a voltage gain of approximately $(R_T + R_2)/R_T$, and the value of (mKT)/q is about 26mV at room temperature. Since resistor R_T varies with temperature to compensate for gain drift, the output voltage, E_O, expressed as a log will be:

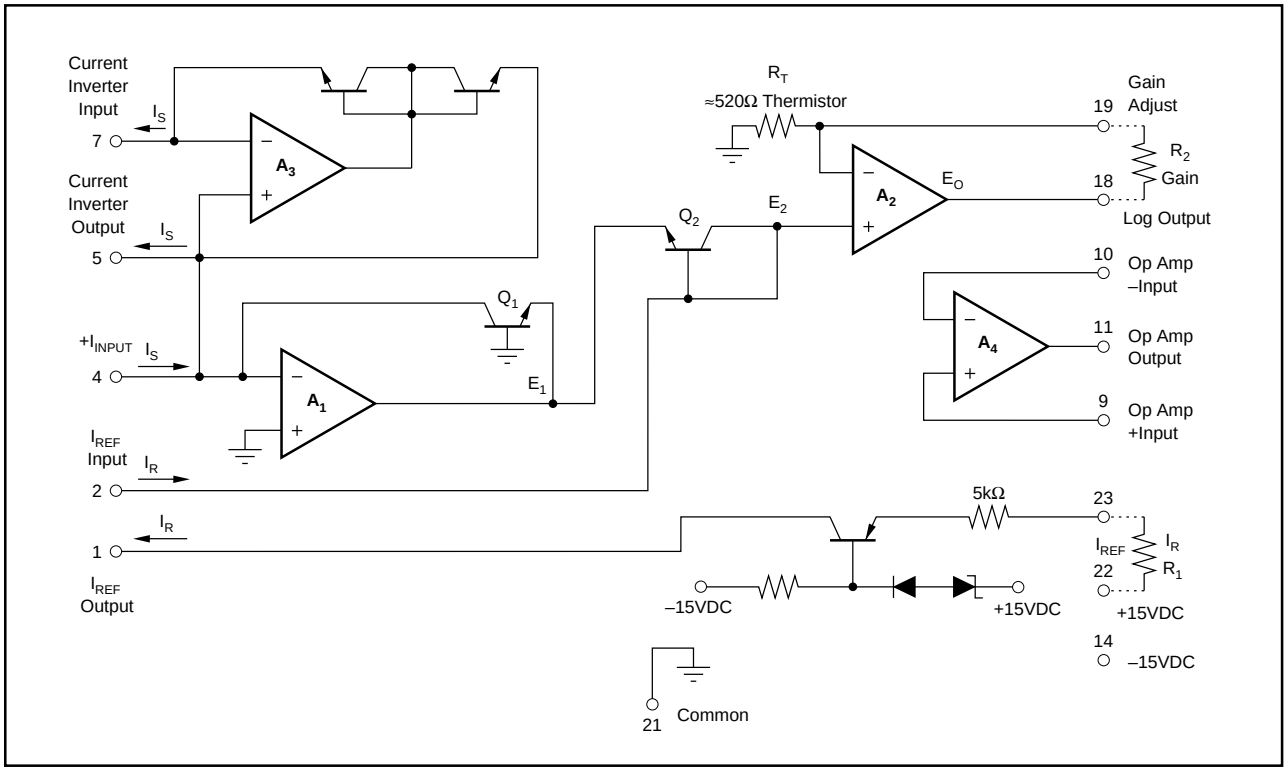


FIGURE 1. Functional Diagram.

$$E_O = -A \log_{10} \frac{I_S}{I_R},$$

$$\text{where } A \approx \frac{R_T + R_2}{R_T}(26\text{mV})\frac{1}{0.434},\ R_T \approx 520\Omega$$

The external resistor R_1 sets the reference current I_R and resistor R_2 sets the scale-factor "A". R_1 and R_2 must be trimmed to the desired values, but the approximate relationships are shown in Typical Performance Curves.

The relationship between the input current, I_S, and the output voltage, E_O, in terms of the externally adjusted parameters, I_R and "A", is illustrated in Typical Performance Curves. This relationship is, of course, restricted to values of I_S between 1nA and 1mA and output voltages of less than ±10V.

CHOOSING THE OPTIMUM SCALE FACTOR AND REFERENCE CURRENT

To minimize the effects of output offset and noise, it is usually best to use the full ±10V output range. Once an output range of ±10V has been chosen, then "A" and I_R can be determined from the Min/Max of the input current, I_S.

$$E_O = -A \log \frac{I_S}{I_R},\ \text{where } I_{MIN} < I_S < I_{MAX}$$

The output range of ±10V for an input range of I_{MIN} to I_{MAX} means that:

$$+10 = -A \log \frac{I_{MIN}}{I_R} \quad \text{and} \quad -10 = -A \log \frac{I_{MAX}}{I_R}$$

Adding these two equations together

$$\log \frac{I_{MAX} + I_{MIN}}{I_R^2} = 0, \text{ or } I_R = \sqrt{I_{MAX}\, I_{MIN}}$$

The value for A can be found from:

$$10 = A \log \frac{I_{MAX}}{\sqrt{I_{MAX}\, I_{MIN}}}$$

In terms of the input current range for I_S, the values for I_R and A that will provide a full ±10V output swing are:

$$I_R = \sqrt{I_{MAX}\, I_{MIN}} \text{ and } A = \frac{10}{\log \frac{I_{MAX}}{I_R}}$$

EXAMPLE

Assume that I_{MIN} is +10nA and I_{MAX} is +100µA.

This is an 80dB range.

$$I_R = \sqrt{I_{MAX}\, I_{MIN}} =$$

$$\sqrt{(10^{-4})\,(10^{-8})} = 10^{-6}, \text{ or } 1\mu A.$$

$$\frac{I_{MAX}}{I_R} = \frac{10^{-4}}{10^{-6}} = 100$$

$$\log \frac{I_{MAX}}{I_R} = 2; \text{ So, } A = 5$$

For an I_R of 1µA and A of 5,

$$E_O = -5\log \frac{I_S}{1\mu A}$$

CONNECTION DIAGRAMS

Transfer function is $E_O = -A \log \frac{I_1}{I_R}$ where I_1 is a positive input current and I_R is the resistor-programmed internal reference current (see Figure 2).

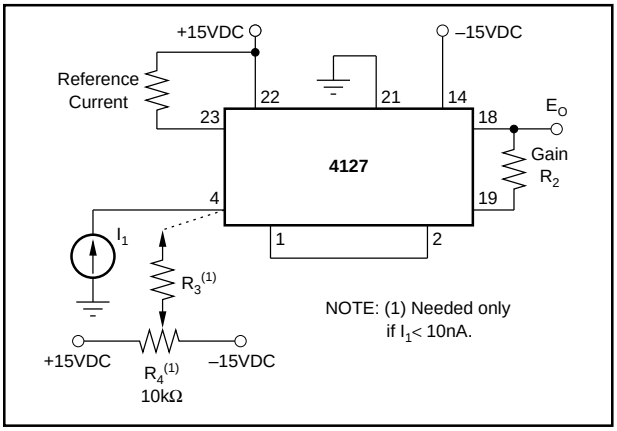


FIGURE 2. Transfer Function When I_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $|I_1| = I_R$, adjust R_1 such that $E_O = 0$.
3. Apply $|I_1| = I_{MAX}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $|I_{1MIN}| \geq 10$nA. Otherwise, apply $|I_1|$ = 1nA, make R_3 = 1kMΩ and adjust R_4 for the proper output voltage. For R_3, a single resistor is recommended. A voltage divider network is difficult to use due to amplifier offset voltage.

Transfer function is $E_O = -A \log \frac{|I_1|}{I_R}$ where I_1 is a negative input current and I_R is the resistor-programmed internal reference current (see Figure 3).

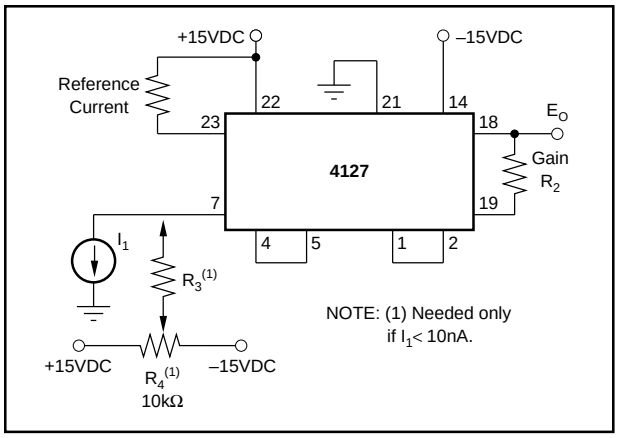


FIGURE 3. Transfer Function When I_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $|I_1| = I_R$ adjust R_1 such that $E_O = 0$.
3. Apply $|I_1| = I_{MAX}$, adjust R_2 for the proper output voltage
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $|I_{1MIN}| \geq 10nA$. Otherwise, apply $|I_1| = 1nA$, make $R_3 = 1kM\Omega$ and adjust R_4 for the proper output voltage. For R_3, a single resistor is recommended. A voltage divider network is difficult to use due to amplifier offset voltage.

Transfer function is $E_O = -A \log \frac{E_1}{R_4 I_R}$, where E_1 is a positive input voltage and I_R is the resistor-programmed internal reference current (see Figure 4).

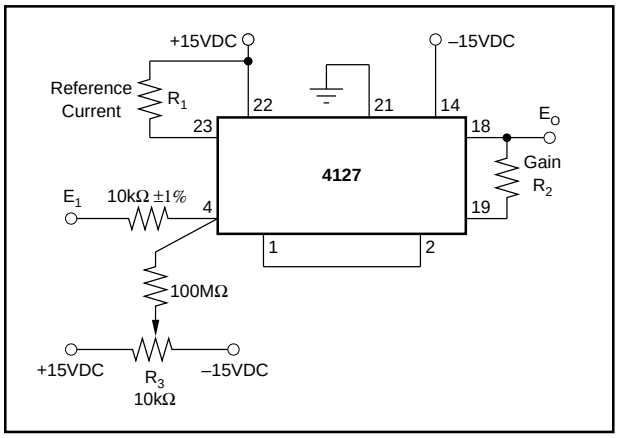


FIGURE 4. Transfer Function When E_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $E_1 = I_R$ (10kΩ), adjust R_1 such that $E_O = 0$.
3. Apply $E_1 = E_{MAX}$, adjust R_2 for the proper output voltage.
4. Apply $E_1 = E_{MIN}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_O = -A \log \frac{|E_1|}{R_4 I_R}$, where E_1 is a negative input voltage and I_R is the resistor-programmed internal reference current (see Figure 5).

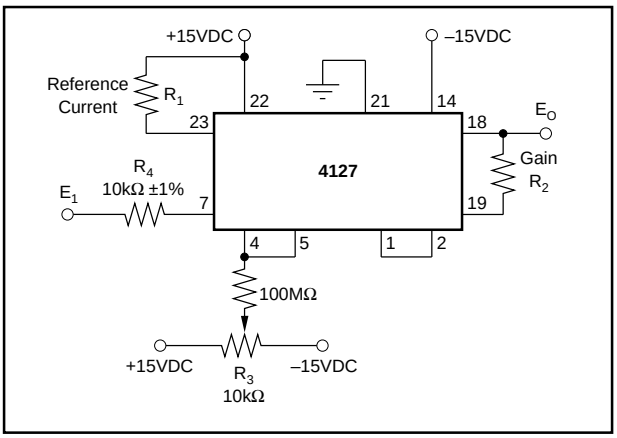


FIGURE 5. Transfer Function When E_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $|E_1| = I_R$ (10kΩ), adjust R_1 such that $E_O = 0$.
3. Apply $|E_1| = E_{MAX}$, adjust R_2 for the proper output voltage.
4. Apply $|E_1| = E_{MIN}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_O = -A \log \frac{|I_1|}{|I_2|}$ with I_1 and I_2 negative; $|I_1| \geq 1nA$, $|I_2| \geq 1\mu A$ (see Figure 6).

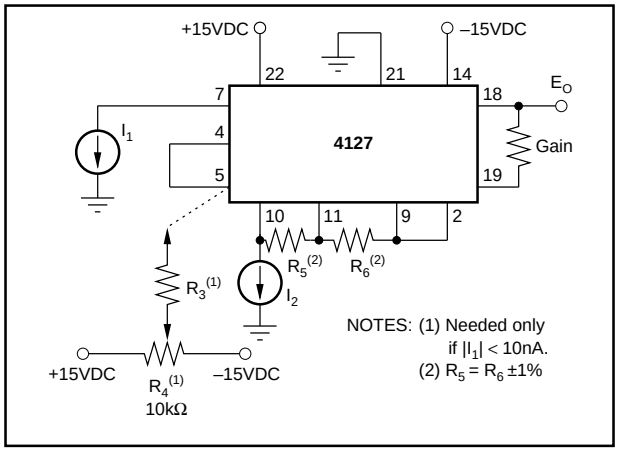


FIGURE 6. Transfer Function When I_1 and I_2 are Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $I_{1\ MIN} \geq 10nA$, otherwise connect the R_3 and R_4 network, with $R_4 = 10k\Omega$ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of ±5mV, it is not practical to use a T-network to replace R_3.

Transfer function is $E_O = -A \log \frac{|I_1|}{I_2}$ with I_1 negative, I_2 positive; $|I_1| \geq 1nA$, $I_2 \geq 1\mu A$ (see Figure 7).

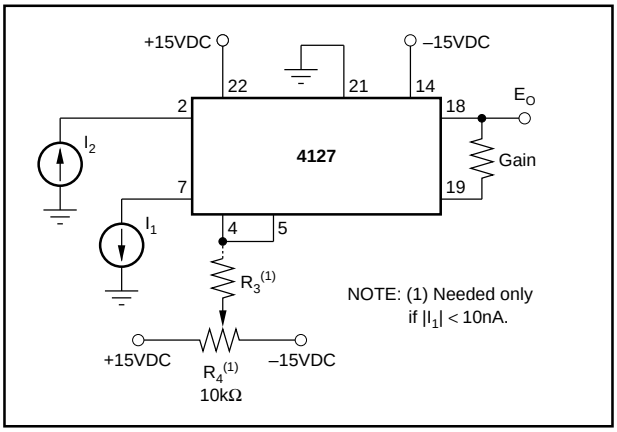


FIGURE 7. Transfer Function When I_1 is Negative, I_2 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $|I_1|_{MIN} \geq 10nA$, otherwise connect the R_3 and R_4 network, with $R_4 = 10k\Omega$ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of ±5mV, it is not practical to use a T-network to replace R_3.

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Transfer function is $E_O = -A \log \frac{I_1}{I_2}$ with I_1 and I_2 positive; $I_1 \geq 1nA$, $I_2 \geq 1\mu A$ (see Figure 8).

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $I_{1\ MIN} \geq 10nA$, otherwise connect the R_3 and R_4 network, with $R_4 = 10k\Omega$ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of ±5mV, it is not practical to use a T-network to replace R_3.

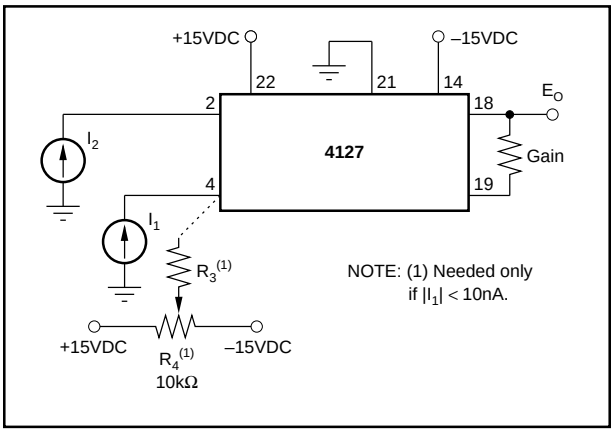

FIGURE 8. Transfer Function When I_1 and I_2 is Positive.

ANTILOG OPERATION

The 4127 can also perform the antilog function. The output is connected through a resistor, R_O, into the current input, pin 4. The input signal is connected through a gain resistor to pin 19 as shown in Figure 9.

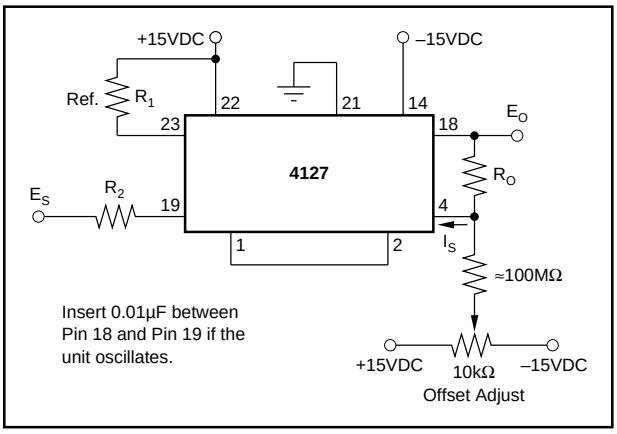

FIGURE 9. Antilog Operation.

These connections form an implicit loop for computing the antilog function. From the block diagram of Figure 1, the voltage at the inverting input of the output amplifier A_2 must equal E_2, so

$$E_2 \approx \frac{R_T}{R_T + R_2} E_S,\ R_T \approx 520\Omega$$

Since the output is connected through R_O to pin 4, the current I_S will equal E_O/R_O and E_2 will be

$$E_2 = -\frac{mKT}{q} \ell n \frac{E_O}{R_O I_R}$$

Combining expressions for E_2 gives the relationship:

$$\frac{R_T}{R_T + R_2} E_S = - \frac{mKT}{q} \ell n \frac{E_O}{R_O I_R}$$

$$- \frac{E_S}{A} = \log \frac{E_O}{R_O I_R}$$

where:

$$A \approx \frac{R_T + R_2}{R_T} (26mV) \frac{1}{0.434}$$

$$E_O = R_O I_R \text{ Antilog} - \frac{E_S}{A}$$

Setting R_O and I_R will set the scale factor. For example, an R_O of 1MΩ and I_R of 1μA will give a scale factor of unity and $E_O = \text{Antilog} - \frac{E_S}{A}$

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
4127JG	NRND	CDIP	JNA	24	15
4127KG	NRND	CDIP	JNA	24	15

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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