PIC16F152XX Family Programming Specification

Introduction

This programming specification describes a SPI-based programming method for the PIC16F152XX family of microcontrollers. Programming Algorithms describes the programming commands, programming algorithms, and electrical specifications used in that particular method. Appendix B contains individual part numbers, device identification, pinout and packaging information, and Configuration Words.

Important: To enter Low-Voltage Programming (LVP) mode, the MSb of the Most Significant nibble must be shifted in first. This differs from entering the key sequence on some other device families.

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1. Overview

1.1 Programming Data Flow

Nonvolatile Memory (NVM) programmed data can be supplied by either the high-voltage In-Circuit Serial Programming™ (ICSP™) interface or the low-voltage In-Circuit Serial Programming (ICSP) interface. Data can be programmed into the Program Flash Memory (PFM), dedicated “User ID” locations, and the Configuration Words.

1.2 Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in Table 1-1. For pin locations and packaging information, refer to this table.

Table 1-1. Pin Descriptions During Programming

Pin Name	During Programming		
	Function	Pin Type	Pin Description
ISCPCLK	ICSPCLK	I	Clock Input - Schmitt Trigger Input
ISCPDAT	ICSPDAT	I/O	Data Input/Output - Schmitt Trigger Input
$\overline{MCLR}/V_{PP}$	Program/Verify mode	I(1)	Program Mode Select
V_{DD}	V_{DD}	P	Power Supply
V_{SS}	V_{SS}	P	Ground

Legend: I = Input, O = Output, P = Power

Note:

1. The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to the $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

1.3 Hardware Requirements

1.3.1 High-Voltage ICSP Programming

In High-Voltage ICSP mode, the device requires two programmable power supplies: one for V_{DD} and one for the $\overline{MCLR}/V_{PP}$ pin.

1.3.2 Low-Voltage ICSP Programming

In Low-Voltage ICSP mode, the device can be programmed using a single V_{DD} source in the device operating range. The $\overline{MCLR}/V_{PP}$ pin does not have to be brought to programming voltage, but can instead be left at the normal operating voltage.

1.3.2.1 Single-Supply ICSP Programming

The device’s LVP Configuration bit enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a ‘1’ (enabled). The LVP bit may only be programmed to ‘0’ by entering the High-Voltage ICSP mode, where the $\overline{MCLR}/V_{PP}$ pin is raised to V_{IHH}. Once the LVP bit is programmed to a ‘0’, only the High-Voltage ICSP mode is available and can be used to program the device.

Important:
- The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying V_{IHH} to the $\overline{MCLR}/V_{PP}$ pin.
- While in Low-Voltage ICSP mode, $\overline{MCLR}$ is always enabled, regardless of the MCLRE bit. Also, the $\overline{MCLR}$ pin can no longer be used as a general purpose input.

1.4 Write and/or Erase Selection

Erasing or writing is selected according to the command used to begin operation (see Table 3-1). The terminologies used in this document, related to erasing/writing to the program memory, are defined in Table 1-2.

Table 1-2. Programming Terms

Term	Definition
Programmed Cell	A memory cell at logic '0'
Erased Cell	A memory cell at logic '1'
Erase	Change memory cell from a '0' to a '1'
Write	Change memory cell from a '1' to a '0'
Program	Generic erase and/or write

1.4.1 Erasing Memory

Program Flash Memory (PFM) is erased by row or in bulk, where 'row' refers to the minimum number of words that can be programmed/erased, and 'bulk' includes many subsets of the total memory space. The duration of the erase is always determined internally, and is determined by the size of the memory. All Bulk ICSP Erase commands have minimum V_{DD} requirements, which are higher than the Row Erase and Write requirements.

Important: Bulk erasing is not supported in self-write operations.

1.4.2 Writing Memory

Program Flash Memory (PFM) is written one row at a time. Multiple 'Load Data for NVM' commands are used to fill the PFM's row data latches. The duration of the write is determined either internally or externally.

1.4.3 Multi-Word Programming Interface

PFM panels include a 32-word (one row) programming interface. The row to be programmed must first be erased with either a Bulk Erase or Row Erase command.

2. Memory Map

This section provides details about how the memory is organized for this device.

Table 2-1. Program Memory Map

Address	Device			
	PIC16F15213 PIC16F15223 PIC16F15243	PIC16F15214 PIC16F15224 PIC16F15244 PIC16F15254 PIC16F15274	PIC16F15225 PIC16F15245 PIC16F15255 PIC16F15275	PIC16F15256 PIC16F15276
0000h to 07FFh	Program Flash Memory (2 KW)(1)	Program Flash Memory (4 KW)(1)	Program Flash Memory (8 KW)(1)	Program Flash Memory (16 KW)(1)
8000h to 0FFFh	**Not Present**(2)			
1000h to 1FFFh		**Not Present**(2)		
2000h to 3FFFh			**Not Present**(2)	
4000h to 7FFFh				**Not Present**(2)
8000h to 8003h	User IDs (4 Words)(3)			
8004h	**Reserved**			
8005h	Revision ID (1 Word)(3)(4)(5)			
80006h	Device ID (1 Word)(3)(4)(5)			
8007h to 800Bh	Configuration Words(3)			
800Ch to 80FFh	**Reserved**			
8100h to 813Fh	Device Information Area (DIA)(3)(5)			
8140h to 81FFh	**Reserved**			
8200h to 82FFh	Device Configuration Information(3)(4)(5)			
8300h to FFFFh	**Reserved**			

Note:

1. Storage Area Flash (SAF) is implemented as the last 128 words of Program Flash Memory, if enabled.
2. The addresses do not roll over. The region is read as '0'. When accessing these areas using the NVMCON registers, reads and/or writes will set the NVMERR bit.
3. Not code-protected.
4. Hard-coded in silicon.
5. This region cannot be written by the user, and is not affected by a Bulk Erase.

2.1 User ID Locations

A user may store identification information (User ID) in four locations. The User ID locations are mapped to 8000h - 8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with or without code protection enabled.

2.2 Device/Revision ID

The 14-bit Device ID register is located at 8006h and the 14-bit Revision ID register is located at 8005h. These locations are read-only and cannot be erased or modified.

2.3 Device Information Area (DIA)

The Device Information Area (DIA) is a dedicated region in the Program Flash Memory. The data is mapped from address 8100h to 813Fh. These locations are read-only and cannot be erased or modified. The DIA contains the Microchip Unique Identifier words, and the Fixed Voltage Reference (FVR) voltage readings in millivolts (mV). The table below holds the DIA information for the PIC16F152XX family of microcontrollers.

Table 2-2. Device Information Area

Address Range	Name of Region	Standard Device Information
8100h-8108h	MUI0	Microchip Unique Identifier (9 Words)
	MUI1	
	MUI2	
	MUI3	
	MUI4	
	MUI5	
	MUI6	
	MUI7	
	MUI8	
8109h	MUI9	Reserved (1 Word)
810Ah-8111h	EUI0	Optional External Unique Identifier (8 Words)
	EUI1	
	EUI2	
	EUI3	
	EUI4	
	EUI5	
	EUI6	
	EUI7	
8112h-8117h	Reserved	Reserved (6 Words)
8118h	FVRA1X	ADC FVR1 Output voltage for 1x setting (in mV)
8119h	FVRA2X	ADC FVR1 Output Voltage for 2x setting (in mV)
811Ah	FVRA4X	ADC FVR1 Output Voltage for 4x setting (in mV)
811Bh-811Fh	Reserved	Reserved (5 Words)

2.4 Device Configuration Information (DCI)

The Device Configuration Information (DCI) is a dedicated region in the memory that holds information about the device, which is useful for programming and bootloader applications. The data stored in this region is read-only and cannot be modified/erased. Refer to the table below for complete DCI table addresses and description.

Table 2-3. Device Configuration Information

Address	Name	Description	Value				Units
			PIC16F15213 PIC16F15223 PIC16F15243	PIC16F15214 PIC16F15224 PIC16F15244 PIC16F15254 PIC16F15274	PIC16F15225 PIC16F15245 PIC16F15255 PIC16F15275	PIC16F15256 PIC16F15276	
8200h	ERSIZ	Erase Row Size	32				Words
8201h	WLSIZ	Number of write latches per row	32				Words
8202h	URSIZ	Number of user erasable rows	64	128	256	512	Rows
8203h	EESIZ	Data EEPROM memory size	0				Bytes
8204h	PCNT	Pin Count	8/14/20	8/14/20/28/40	14/20/28/40	28/40	Pins

2.5 Configuration Words

The devices have five Configuration Words, starting at address 8007h. Configuration bits enable or disable specific features, placing these controls outside the normal software process, and they establish configured values prior to the execution of any software.

In terms of programming, these important Configuration bits should be considered:

1. **LVP: Low-Voltage Programming Enable bit**
   - `1 = ON`: Low-Voltage Programming is enabled. $\overline{MCLR}/V_{PP}$ pin function is $\overline{MCLR}$. MCLRE Configuration bit is ignored.
   - `0 = OFF`: High voltage on $\overline{MCLR}/V_{PP}$ must be used for programming.

Important: The LVP bit cannot be written (to '0') while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the Configuration state. For more information, see Low-Voltage Programming (LVP) Mode.

2. **MCLRE: Master Clear ($\overline{MCLR}$) Enable bit**
   - If LVP = `1`: RA3 pin function is $\overline{MCLR}$
   - If LVP = `0`
     - `1` = $\overline{MCLR}$ pin is $\overline{MCLR}$
     - `0` = $\overline{MCLR}$ pin function is a port-defined function
3. **$\overline{CP}$: User NVM Program Memory Code Protection bit**

- 1 = OFF: User NVM code protection is disabled
- 0 = ON: User NVM code protection is enabled

For more information on code protection, see Code Protection.

2.6 Device ID

Name: DEVICEID
Offset: 8006h

Device ID Register

Bit	15	14	13	12	11	10	9	8
			Reserved	Reserved	DEV[11:8]			
Access			R	R	R	R	R	R
Reset			1	1	q	q	q	q

Bit	7	6	5	4	3	2	1	0
	DEV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	q	q	q	q	q	q	q	q

Bit 13 – Reserved Reserved - Read as 1

Bit 12 – Reserved Reserved - Read as 1

Bits 11:0 – DEV[11:0] Device ID

Device	Device ID
PIC16F15213	30E3h
PIC16F15214	30E6h
PIC16F15223	30E4h
PIC16F15224	30E7h
PIC16F15225	30E9h
PIC16F15243	30E5h
PIC16F15244	30E8h
PIC16F15245	30EAh
PIC16F15254	30F0h
PIC16F15255	30EFh
PIC16F15256	30EBh
PIC16F15274	30EEh
PIC16F15275	30EDh
PIC16F15276	30ECh

2.7 Revision ID

Name: REVISIONID
Offset: 8005h

Revision ID Register

Bit	15	14	13	12	11	10	9	8
			Reserved	Reserved	MJRREV[5:2]			
Access			R	R	R	R	R	R
Reset			1	0	q	q	q	q

Bit	7	6	5	4	3	2	1	0
	MJRREV[1:0]		MNRREV[5:0]					
Access	R	R	R	R	R	R	R	R
Reset	q	q	q	q	q	q	q	q

Bit 13 – Reserved Reserved - Read as 1

Bit 12 – Reserved Reserved - Read as 0

Bits 11:6 – MJRREV[5:0] Major Revision ID
These bits are used to identify a major revision. (A0, B0, C0, etc.).

Bits 5:0 – MNRREV[5:0] Minor Revision ID
These bits are used to identify a minor revision.

3. Programming Algorithms

3.1 Program/Verify Mode

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted MSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK pins are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state, all I/Os are automatically configured as high-impedance inputs and the Program Counter (PC) is cleared.

3.1.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different modes of entering Program/Verify mode via high voltage:

- V_{PP}-First Entry mode
- V_{DD}-First Entry mode

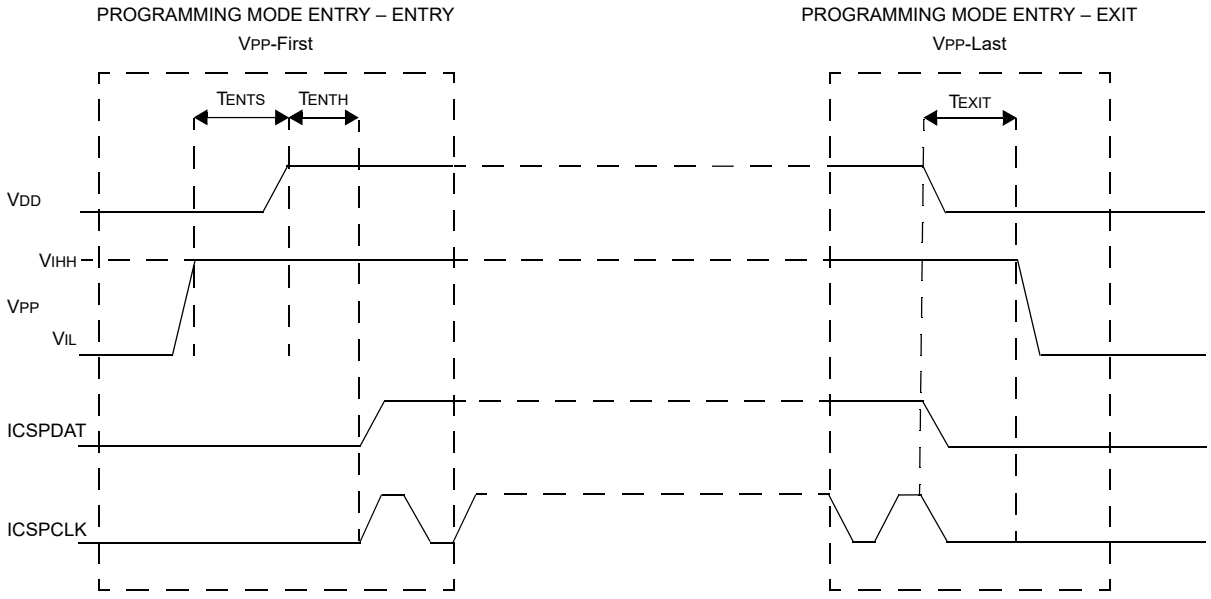
3.1.1.1 V_{PP}-First Entry Mode

To enter Program/Verify mode via the V_{PP}-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on $\overline{MCLR}$ from 0V to V_{IHH}.
3. Raise the voltage on V_{DD} from 0V to the desired operating voltage.

The V_{PP}-First Entry mode prevents the device from executing code prior to entering Program/Verify mode. For example, when the Configuration Byte has already been programmed to have $\overline{MCLR}$ disabled (MCLRE = 0), the Power-up Timer disabled ($\overline{PWRTE}$ = 0) and the internal oscillator selected, the device will execute code immediately. V_{PP}-First Entry mode is strongly recommended as it prevents user code from executing. See the timing diagram in Figure 3-1.

Figure 3-1. PROGRAMMING ENTRY AND EXIT MODES – V_{PP}-First and Last



3.1.1.2 V_{DD}- First Entry Mode

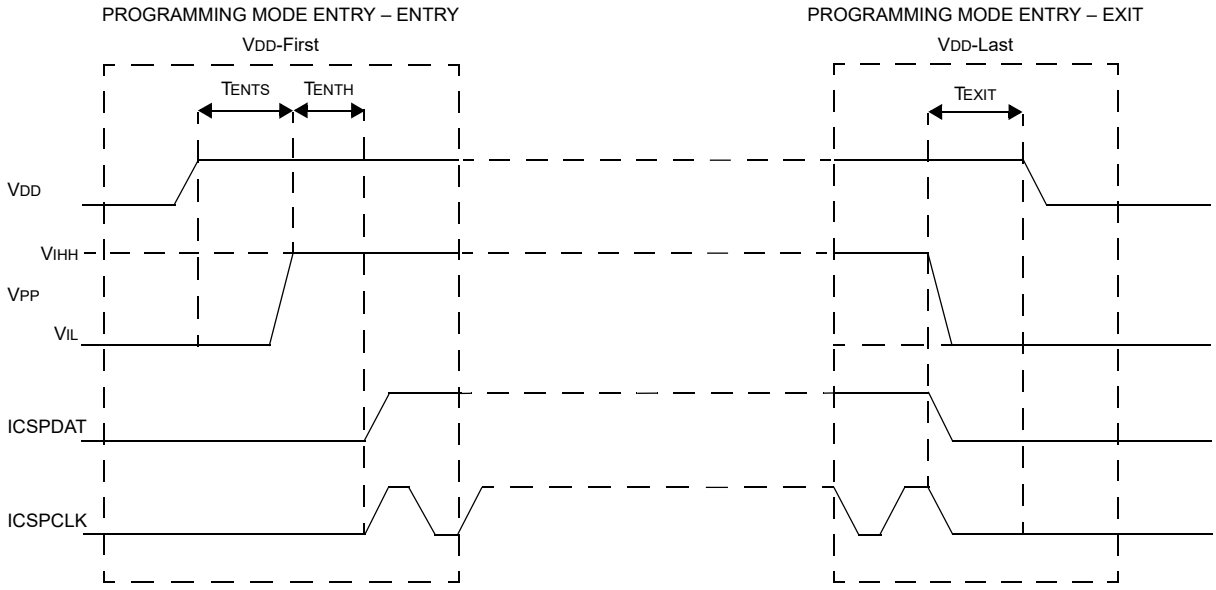
To enter Program/Verify mode via the V_{DD}-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.

2. Raise the voltage on V_{DD} from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{MCLR}$ from V_{DD} or below to V_{IHH}.

The V_{DD}-First Entry mode is useful for programming the device when V_{DD} is already applied, for it is not necessary to disconnect V_{DD} to enter Program/Verify mode. See the timing diagram in Figure 3-2.

Figure 3-2. PROGRAMMING ENTRY AND EXIT MODES – V_{DD}-First and Last



3.1.1.3 Program/Verify Mode Exit

To exit Program/Verify mode, lower $\overline{MCLR}$ from V_{IHH} to V_{IL}. V_{PP}-First Entry mode should use V_{PP}-Last Exit mode (see Figure 3-1). V_{DD}-First Entry mode should use V_{DD}-Last Exit mode (see Figure 3-2).

3.1.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the devices to be programmed using V_{DD} only, without high voltage. When the LVP bit in the Configuration Word 4 register is set to '1', the Low-Voltage ICSP Programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify mode requires the following steps:

1. $\overline{MCLR}$ is brought to V_{IL}.
2. A **32-bit key sequence** is presented on ICSPDAT, clocked by ICSPCLK. The LSb of the pattern is a "don't care X". The Program/Verify mode entry pattern detect hardware verifies only the first 31 bits of the sequence and the last clock is required before the pattern detect goes active.

The key sequence is a specific 32-bit pattern, '32'h4d434850' (more easily remembered as **MCHP** in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit of the Most Significant Byte must be shifted in first. Once the key sequence is complete, $\overline{MCLR}$ must be held at V_{IL} for as long as Program/Verify mode is to be maintained. For Low-Voltage Programming timing, see Figure 3-3 and Figure 3-4.

Figure 3-3. LVP Entry (Powered)

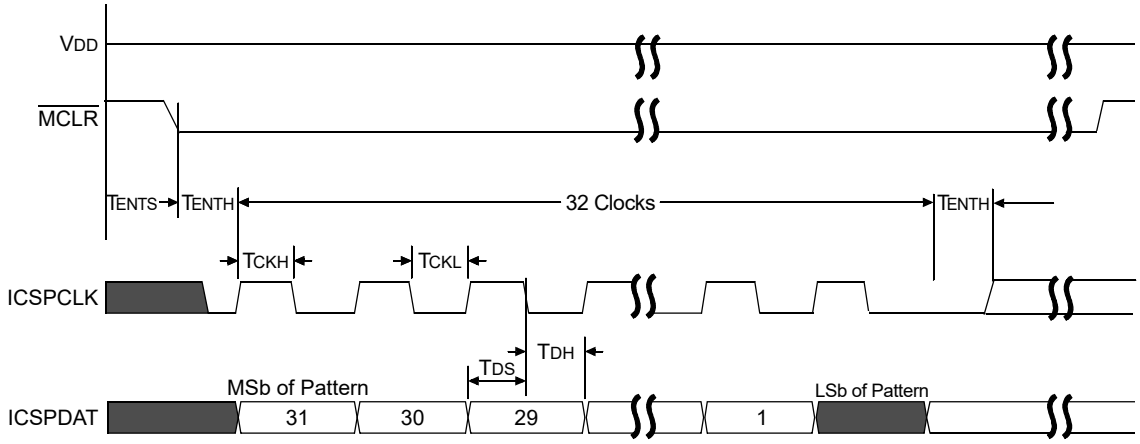
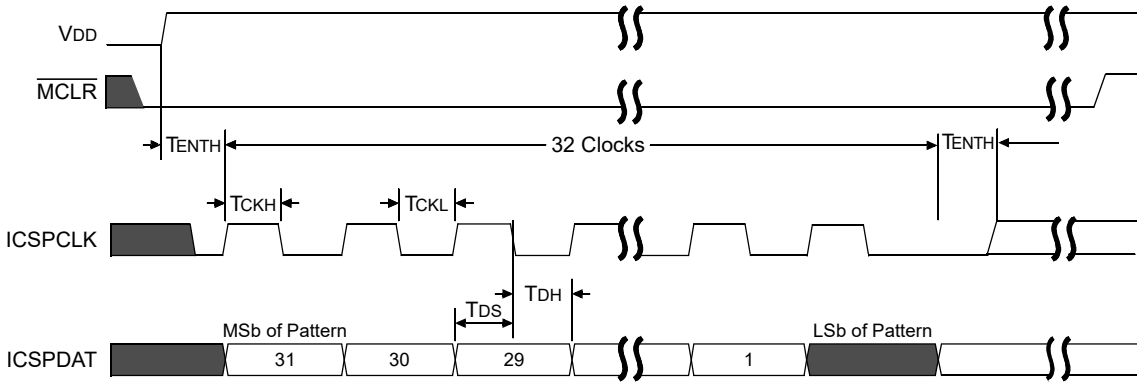


Figure 3-4. LVP Entry (Powering Up)



Exiting Program/Verify mode is done by raising $\overline{MCLR}$ from below V_{IL} to V_{IH} level (or higher, up to V_{DD}).

Important:
To enter LVP mode, the MSb of the Most Significant nibble must be shifted in first. This differs from entering the key sequence on some other device families.

3.2 Program/Verify Commands

Once a device has entered ICSP Program/Verify mode (using either high-voltage or LVP entry), the programming host device may issue commands to the microcontroller, each eight bits in length. The commands are summarized in Table 3-1. The commands are used to erase or program the device based on the location of the Program Counter (PC).

Some of the 8-bit commands also have an associated data payload (such as Load PC Address and Read Data from NVM).

If the host device issues an 8-bit command byte that has an associated data payload, the host device is responsible for sending an additional 24 clock pulses (for example, three 8-bit bytes) in order to send or receive the payload data associated with the command.

The payload field size is compatible with many 8-bit SPI-based systems. Within each 24-bit payload field, the first bit transmitted is always a Start bit, followed by a variable number of Pad bits, followed by the useful data payload bits and ending with one Stop bit. The useful data payload bits are always transmitted Most Significant bit (MSb) first.

When the programming device issues a command that involves a host to microcontroller payload (for example, Load PC Address), the Start, Stop and Pad bits should all be driven by the programmer to '0'. When the programming host device issues a command that involves microcontroller to host payload data (for example, Read Data from NVM), the Start, Stop and Pad bits should be treated as "don't care" bits and the values should be ignored by the host.

When the programming host device issues an 8-bit command byte to the microcontroller, the host should wait a specified minimum amount of delay (which is command-specific) prior to sending any additional clock pulses (associated with either a 24-bit data payload field or the next command byte).

Table 3-1. ICSP™ COMMAND SET SUMMARY

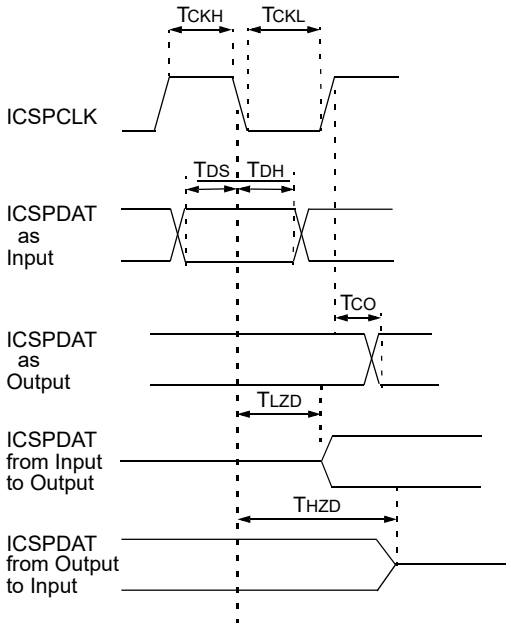
Command Name	Command Value		Payload Expected	Delay after Command	Data/Note
	Binary (MSb … LSb)	Hex			
Load PC Address	1000 0000	80	Yes	T_{DLY}	Payload Value = PC
Bulk Erase Program Memory	0001 1000	18	No	T_{ERAB}	The PC value is used to identify the regions that need to be bulk erased.
Row Erase Program Memory	1111 0000	F0	No	T_{ERAS}	The row addressed by the MSbs of the PC is erased; LSbs are ignored.
Load Data for NVM	0000 00J0	00/02	Yes - Data In	T_{DLY}	Data is loaded to the data latch addressed by the LSb's of the PC; MSb's are ignored. J = 0: PC is unchanged J = 1: PC = PC + 1 after writing
Read Data from NVM	1111 11J0	FC/FE	Yes - Data Out	T_{DLY}	Data output '0' if code-protect is enabled. J = 0: PC is unchanged J = 1: PC = PC + 1 after reading
Increment Address	1111 1000	F8	No	T_{DLY}	PC = PC + 1

.....continued

Command Name	Command Value		Payload Expected	Delay after Command	Data/Note
	Binary (MSb ... LSb)	Hex			
Begin Internally Timed Programming	1110 0000	E0	No	T_{PINT}	Commits latched data to NVM (self-timed).
Begin Externally Timed Programming	1100 0000	C0	No	T_{PEXT}	Commits latched data to NVM (externally timed). After P_{TEXT}, "End Externally Timed Programming" command must be used.
End Externally Timed Programming	1000 0010	82	No	T_{DIS}	Should be issued within required time delay (T_{PEXT}) after "Begin Externally Timed Programming" command.

Important: All clock pulses for both the 8-bit commands and the 24-bit payload fields are generated by the host programming device. The microcontroller does not drive the ICSPCLK line. The ICSPDAT signal is a bidirectional data line. For all commands and payload fields, except the Read Data from NVM payload, the host programming device continuously drives the ICSPDAT line. Both the host programmer device and the microcontroller should latch received ICSPDAT values on the falling edge of the ICSPCLK line. When the microcontroller receives ICSPDAT line values from the host programmer, the ICSPDAT values must be valid a minimum of T_{DS} before the falling edges of ICSPCLK and should remain valid for a minimum of T_{DH} after the falling edge of ICSPDAT. See Figure 3-5.

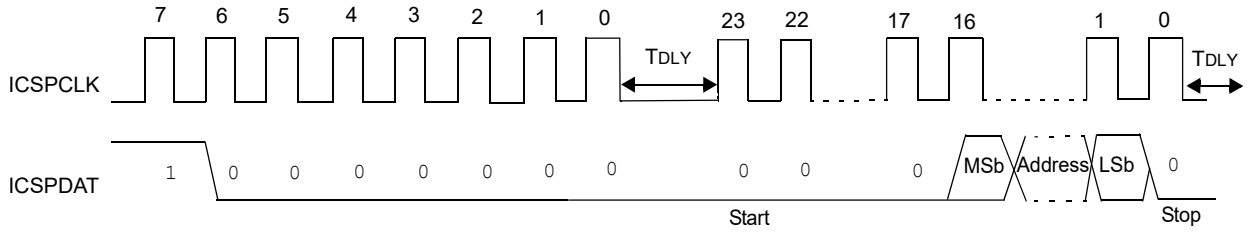
Figure 3-5. Clock and Data Timing



3.2.1 Load PC Address

The PC value is set using the supplied data. The address implies the memory panel to be accessed (see Figure 3-6).

Figure 3-6. Load PC Address



3.2.2 Bulk Erase Program Memory

The Bulk Erase Program Memory command performs different functions dependent on the current PC address. The Bulk Erase command affects specific portions of the memory depending on the initial value of the Program Counter. Whenever a Bulk Erase Program Memory command is executed, the device will erase all bytes within the regions listed in Table 3-2. While a programming command is in progress, this command executes as a `NOP`.

After receiving the Bulk Erase Program Memory command, the erase will not complete until the time interval, T_{ERAB}, has expired (see Figure 3-7). The programming host device should not issue another 8-bit command until after the T_{ERAB} interval has fully elapsed.

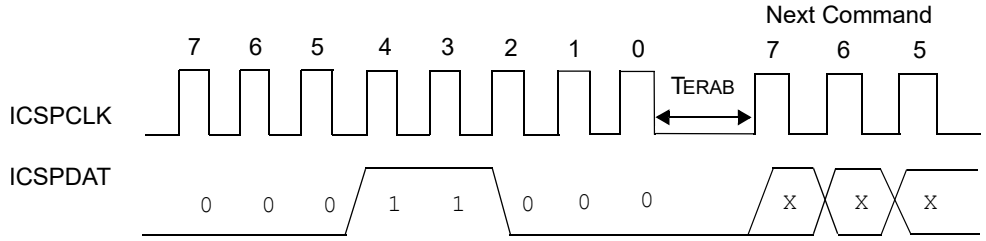
Table 3-2. Bulk Erase Table

Address	Area(s) Erased	
	$\overline{CP}$ = 1	$\overline{CP}$ = 0
0000h-7FFFh(1)	User Flash	User Flash
	Configuration Words	Configuration Words
8000h-80FDh	User Flash	User Flash
	Configuration Words	Configuration Words
	User ID words	User ID words
80FEh-80FFh	User Flash	User Flash
8100h-E7FFh	No Operation	No Operation

.....continued		
Address	Area(s) Erased	
	$\overline{CP}$ = 1	$\overline{CP}$ = 0
E800h-EFFFh	User Flash	User Flash
	Configuration Words	Configuration Words
	User ID words	User ID words

Note:
1. See Table 2-1 for device-specific PFM size and address locations.

Figure 3-7. Bulk Erase Memory

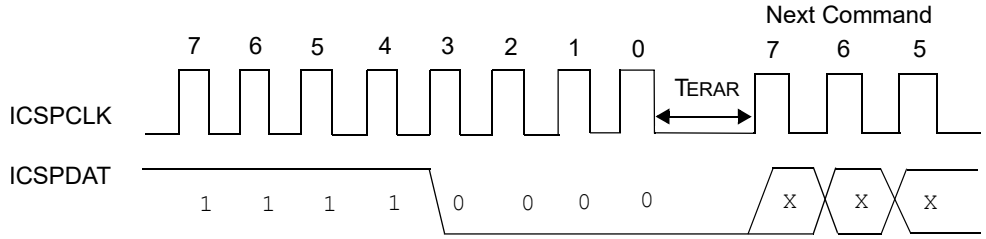


3.2.3 Row Erase Program Memory

The Row Erase Program Memory command will erase an individual row. If the program memory is code-protected, the Row Erase Program Memory command will be ignored. When the address is 8000h-8004h, the Row Erase Program Memory command will only erase the User ID locations regardless of the setting of the $\overline{CP}$ Configuration bit. When write and erase operations are done on a row basis, the row size (number of 14-bit words) for erase operation is 32 and the row size (number of 14-bit latches) for the write operation is 32.

The Flash memory row defined by the current PC will be erased. The user must wait T_{ERAR} for erasing to complete (see Figure 3-8).

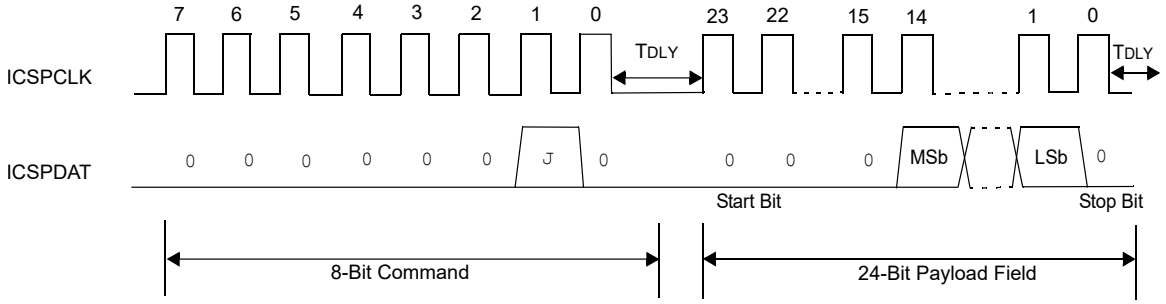
Figure 3-8. Row Erase Program Memory



3.2.4 Load Data for NVM

The Load Data for NVM command is used to load one programming data latch (for example, one 14-bit instruction word for program memory/configuration memory/User ID memory). The Load Data for NVM command can be used to load data for Program Flash Memory (see Figure 3-9). The word writes into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming commands write the entire row of data latches, not just one word. The lower five bits of the address are considered, while the other bits are ignored. Depending on the value of bit 1 of the command, the Program Counter (PC) may or may not be incremented (see Table 3-1).

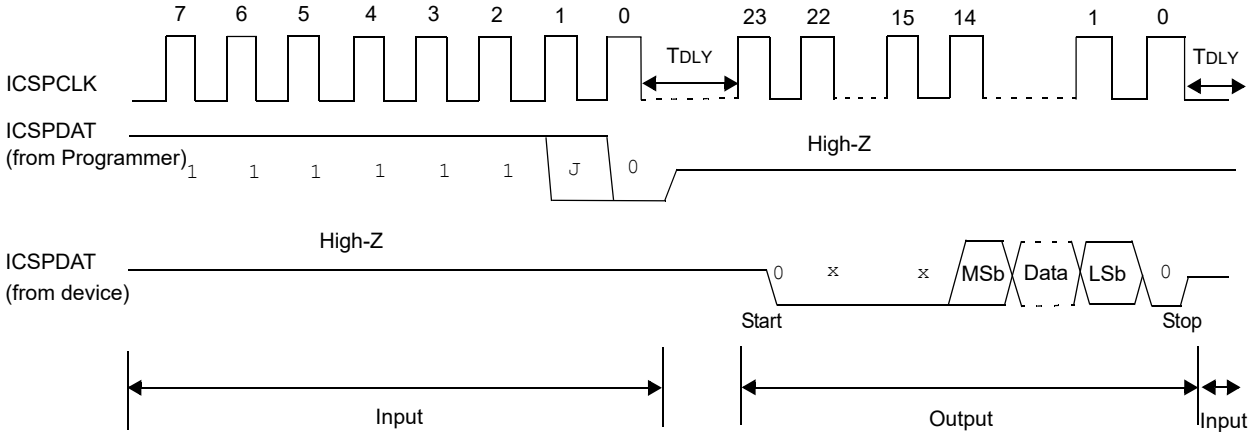
Figure 3-9. Load Data for NVM



3.2.5 Read Data from NVM

The Read Data from NVM command will transmit data bits out of the current PC address. The ICSPDAT pin will go into Output mode on the first falling edge of ICSPCLK, and it will revert to Input mode (high-impedance) after the 24th falling edge of the clock. The Start and Stop bits are only one half of a bit time wide, and should, therefore, be ignored by the host programmer device (since the latched value may be indeterminate). Additionally, the host programmer device should only consider the MSb to LSb payload bits as valid, and should ignore the values of the pad bits. If the program memory is code-protected ($\overline{CP}$ = 0), the data will be read as zeros (see Figure 3-10). Depending on the value of bit '1' of the command, the PC may or may not be incremented (see Table 3-1).

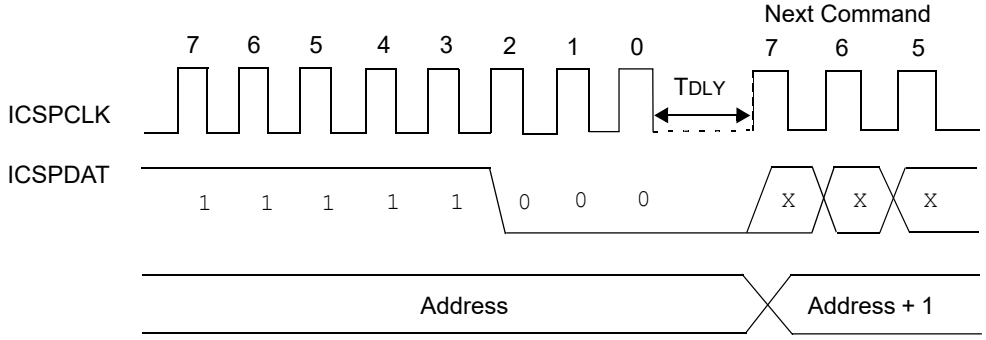
Figure 3-10. Read Data from NVM



3.2.6 Increment Address

The PC is incremented by one when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Load PC Address command. This command performs the same action as the J bit in the Load/Read commands. See Figure 3-11.

Figure 3-11. Increment Address

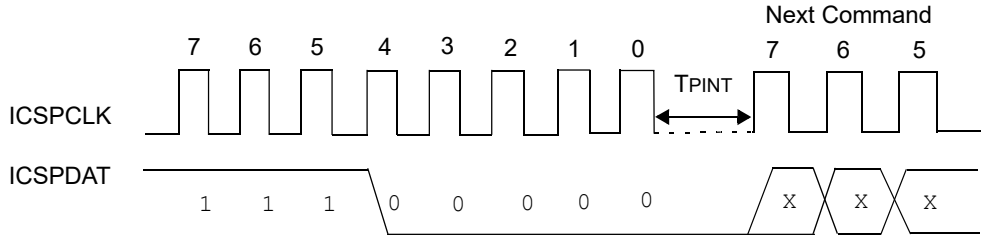


3.2.7 Begin Internally Timed Programming

The write programming latches must already have been loaded using the Load Data for NVM command, prior to issuing the Begin Internally Timed Programming command. Programming of the addressed memory row will begin after this command is received. The lower LSBs of the address are ignored. An internal timing mechanism executes the write. The user must allow for the Erase/Write cycle time, T_{PINT}, in order for the programming to complete, prior to issuing the next command (see Figure 3-12).

After the programming cycle is complete all the data latches are reset to '1'.

Figure 3-12. Begin Internally Timed Programming

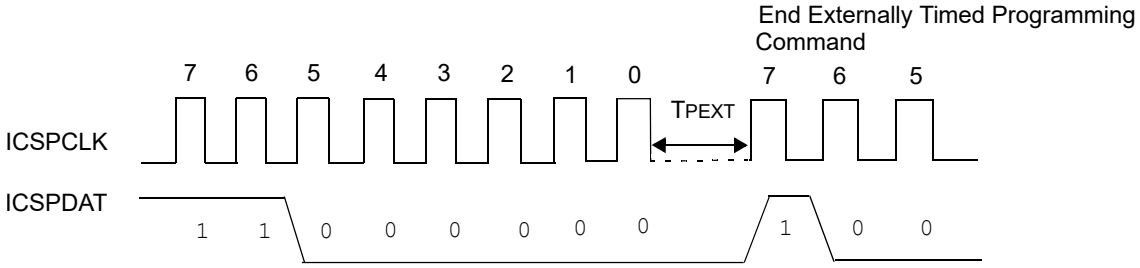


3.2.8 Begin Externally Timed Programming

Data to be programmed must be previously loaded by the Load Data for NVM command before every Begin Externally Timed Programming command. To complete the programming, the End Externally Timed Programming command must be sent in the specified time window defined by T_{PEXT} (see Figure 3-13). The lower LSBs of the address are ignored.

Externally timed writes are not supported for Configuration Words. Any externally timed write to the Configuration Words will have no effect on the targeted word.

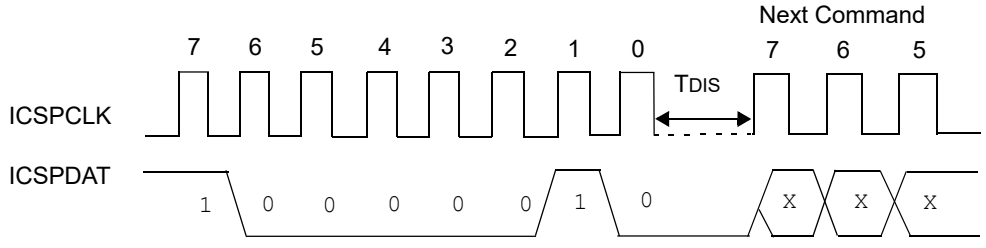
Figure 3-13. Begin Externally Timed Programming



3.2.9 End Externally Timed Programming

This command is required to terminate the programming sequence after a Begin Externally Timed Programming command is given. If no programming command is in progress or if the programming cycle is internally timed, this command will execute as a No Operation (NOP) (see Figure 3-14).

Figure 3-14. End Externally Timed Programming



3.3 Programming Algorithms

The device uses internal latches to temporarily store the 14-bit words used for programming. The data latches allow the user to program a full row with a single Begin Internally Timed Programming or Begin Externally Timed

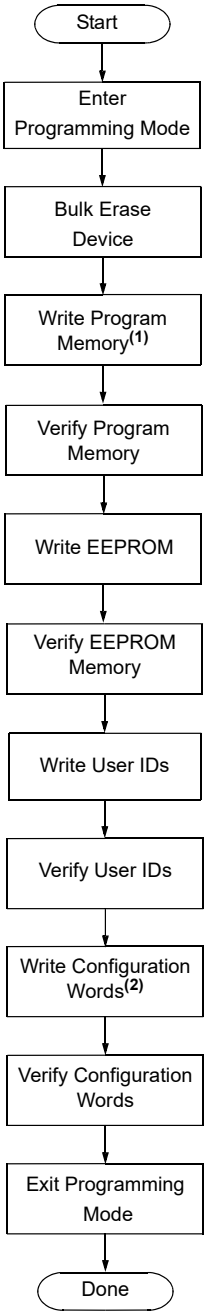
Programming command. The Load Data for NVM command is used to load a single data latch. The data latch will hold the data until the Begin Internally Timed Programming or Begin Externally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The address at the time the Begin Internally Timed Programming or Begin Externally Timed Programming command is given will determine which memory row is written. Writes cannot cross a physical row boundary. For example, attempting to write from address 0002h-0021h in a 32-latch device will result in data being written to 0020h-003Fh.

If more than the maximum number of latches are written without a Begin Internally Timed Programming or Begin Externally Timed Programming command, the data in the data latches will be overwritten. The following flowcharts show the recommended flowcharts for programming.

Important: The Program Flash Memory region is programmed one row (32 words) at a time (Figure 3-18), while the Configuration Words are programmed one word at a time (Figure 3-17). The value of the PC at the time of issuing the Begin Internally Timed Programming or Begin Externally Timed Programming command determines what row (of Program Flash Memory), or what word (of Configuration Word) will get programmed.

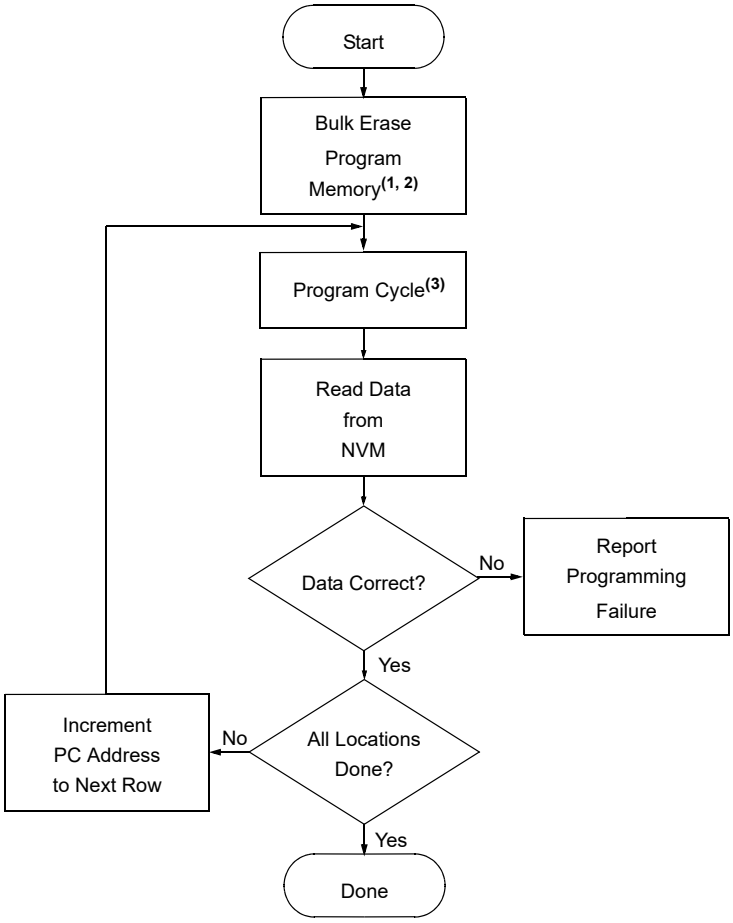
Figure 3-15. Device Program/Verify Flowchart



Note:

1. See 3.2.1 Load PC Address.
2. See 3.2.3 Row Erase Program Memory.

Figure 3-16. Program Memory Flowchart



Note:

1. This step is optional if the device has already been erased or has not been previously programmed.
2. If the device is code-protected or must be completely erased, then Bulk Erase the device per Figure 3-20.
3. See 3.2.2 Bulk Erase Program Memory.

Figure 3-17. One-Word Program Cycle

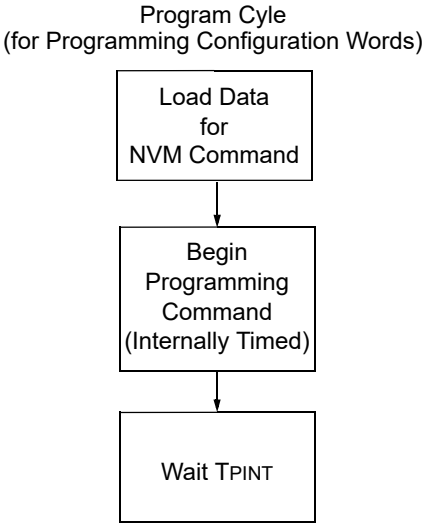


Figure 3-18. Multiple-Word Program Cycle

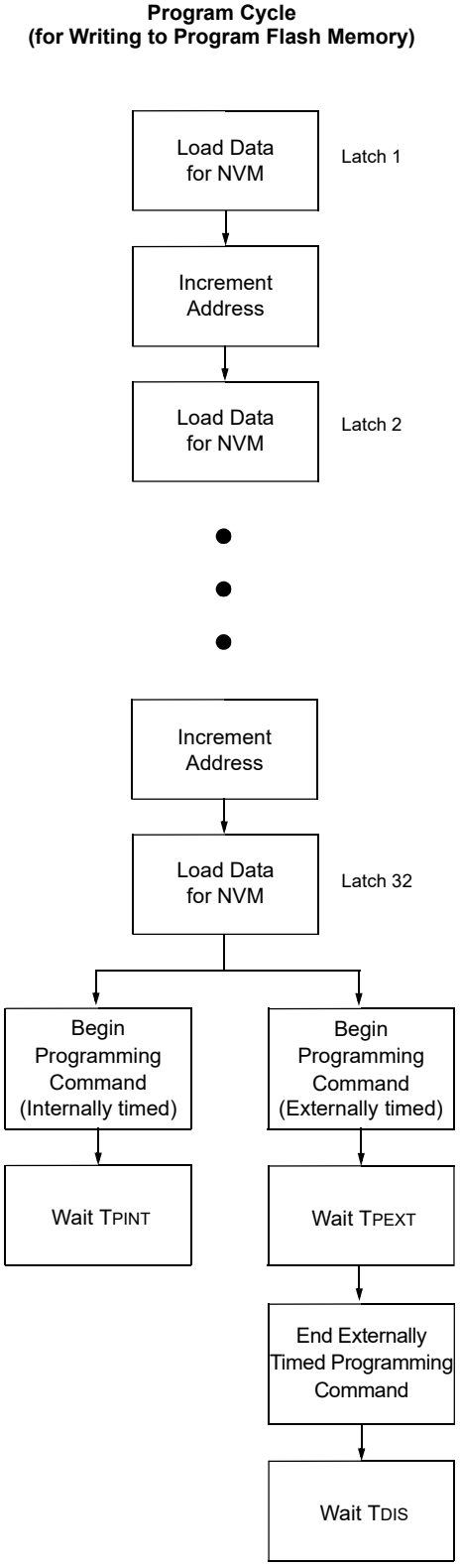
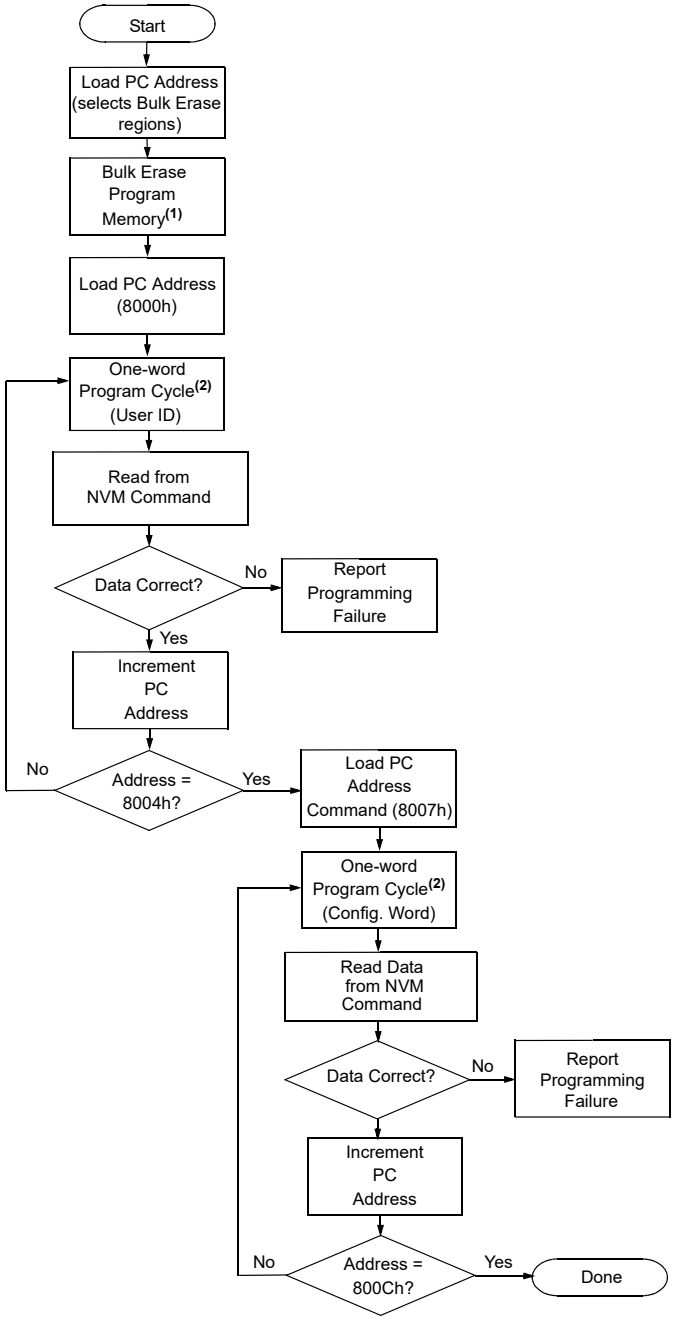


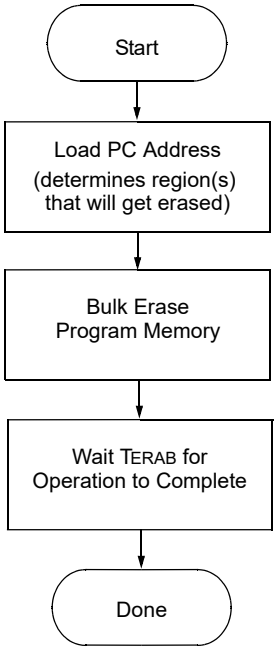
Figure 3-19. Configuration Memory Program Flowchart



Note:

1. This step is optional if the device is erased or not previously programmed.
2. See 3.2.7 Begin Internally Timed Programming.

Figure 3-20. Bulk Erase Flowchart



3.4 Code Protection

Code protection is controlled using the $\overline{CP}$ bit. When code protection is enabled, all program memory locations (0000h-7FFFh) read as '0'. Further programming is disabled for the program memory (0000h-7FFFh), until the next Bulk Erase operation is performed. Program memory can still be programmed and read during program execution.

The Revision ID, Device ID, Device Information Area, Device Configuration Information, User IDs, and Configuration Words can be programmed or read regardless of the code protection settings.

The only way to disable code protection is to use the Bulk Erase Program Memory command with a PC value of 80FDh or lower. This action will clear code protection and erase all memory locations.

3.5 Hex File Usage

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. For example, if the Configuration Word 1 is stored at 8007h, in the hex file this will be referenced as 1000Eh-1000Fh.

3.5.1 Configuration Words

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and User ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and User ID information should be included.

Important: Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

3.5.2 Device ID

If a Device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the Device ID against the value read from the part. On a mismatch condition, the programmer should generate a warning message.

3.6 CRC Checksum Computation

Unlike older PIC® devices, the Microchip toolchain runs a 32-bit CRC calculation on the entire hex file to calculate its checksum. The checksum uses the standard CRC-32 algorithm with the polynomial 0x4C11DB7 $\left(x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1\right)$.

4. Electrical Specifications

Refer to the device-specific data sheet for absolute maximum ratings.

Table 4-1. AC/DC Characteristic Timing Requirements for Program/Verify Mode

AC/DC Characteristics		Standard Operating Conditions Production tested at +25°C				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/ Comments**
Programming Supply Voltages and Currents						
V_{DD}	Supply Voltage (V_{DDMIN}, V_{DDMAX})	1.80	—	5.50	V	**(Note 1)**
V_{PEW}	Read/Write and Row Erase Operations	V_{DDMIN}	—	V_{DDMAX}	V	
V_{BE}	Bulk Erase Operations	V_{BORMAX}	—	V_{DDMAX}	V	**(Note 2)**
I_{DDI}	Current on V_{DD}, Idle	—	—	1.0	mA	
I_{DDP}	Current on V_{DD}, Programming	—	—	10	mA	
I_{PP}	**V_{PP}**					
	Current on $\overline{MCLR}/V_{PP}$	—	—	600	µA	
V_{IHH}	High Voltage on $\overline{MCLR}/V_{PP}$ for Program/Verify Mode Entry	7.9	—	9.0	V	
T_{VHHR}	$\overline{MCLR}$ Rise Time (V_{IL} to V_{IHH}) for Program/Verify Mode Entry	—	—	1.0	µs	
V_{IH}	**I/O Pins**					
	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) Input High Level	0.8 V_{DD}	—	V_{DD}	V	
V_{IL}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) Input Low Level	V_{SS}	—	0.2 V_{DD}	V	
V_{OH}	ICSPDAT Output High Level	V_{DD}-0.7	—	—	V	I_{OH} = 3 mA, V_{DD} = 3.0V
V_{OL}	ICSPDAT Output Low Level	—	—	V_{SS} + 0.6	V	I_{OL} = 6 mA, V_{DD} = 3.0V
Programming Mode Entry and Exit						
T_{ENTS}	Programing Mode Entry Setup Time: ICSPCLK, ICSPDAT Setup Time before V_{DD} or $\overline{MCLR}$↑	100	—	—	ns	
T_{ENTH}	Programing Mode Entry Hold Time: ICSPCLK, ICSPDAT Hold Time before V_{DD} or $\overline{MCLR}$↑	250	—	—	µs	
Serial Program/Verify						
T_{CKL}	Clock Low Pulse Width	100	—	—	ns	
T_{CKH}	Clock High Pulse Width	100	—	—	ns	
T_{DS}	Data in Setup Time before Clock↓	100	—	—	ns	
T_{DH}	Data in Hold Time after Clock↓	100	—	—	ns	

.....continued

AC/DC Characteristics		Standard Operating Conditions Production tested at +25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/ Comments
T_{CO}	Clock↑ to Data Out Valid (during a Read Data from NVM command)	0	—	80	ns	
T_{LZD}	Clock↓ to Data Low-Impedance (during a Read Data from NVM command)	0	—	80	ns	
T_{HZD}	Clock↓ to Data High-Impedance (during a Read Data from NVM command)	0	—	80	ns	
T_{DLY}	Data Input not Driven to Next Clock Input (delay required between command/data or command/command)	1.0	—	—	µs	
T_{ERAB}	Bulk Erase Cycle Time	—	—	8.4	ms	Program, Config and ID
T_{ERAR}	Row Erase Cycle Time	—	—	2.8	ms	
T_{PINT}	Internally Timed Programming Operation Time	—	—	2.8	ms	Program Memory
		—	—	5.6	ms	Configuration Words
T_{PEXT}	Delay Required between Begin Externally Timed Programming and End Externally Timed Programming Commands	1.0	—	2.1	ms	**(Note 3)**
T_{DIS}	Delay Required after End Externally Timed Programming Command	300	—	—	µs	
T_{EXIT}	Time Delay when Exiting Program/Verify Mode	1	—	—	µs	

Note:

1. Bulk Erased devices default to Brown-out Reset enabled with BORV = 1 (low trip point). V_{DDMIN} is the V_{BOR} threshold (with BORV = 1) when performing Low-Voltage Programming on a Bulk Erased device to ensure that the device is not held in Brown-out Reset.
2. The hardware requires V_{DD} to be above the BOR threshold in order to perform Bulk Erase operations. This threshold does not depend on the BORV Configuration bit setting. Refer to the microcontroller device data sheet specifications for min./typ./max limits of the V_{BOR} level.
3. Externally timed writes are not supported for Configuration Words.

5. Appendix A: Revision History

Doc Rev.	Date	Comments
A	10/2019	Initial Document Release

6. Appendix B: Pinout Descriptions and Configuration Words

Table 6-1. Programming Pin Locations By Package Type

Device	Package	Package Code	V_{DD}	V_{SS}	$\overline{MCLR}$		ICSPCLK		ICSPDAT	
			PIN	PIN	PIN	PORT	PIN	PORT	PIN	PORT
PIC16F15213 PIC16F15214	8-Pin SOIC	(SN)	1	8	4	RA3	6	RA1	7	RA0
	8-Pin DFN	(MF)	1	8	4	RA3	6	RA1	7	RA0
PIC16F15223 PIC16F15224 PIC16F15225	14-Pin TSSOP	(ST)	1	14	4	RA3	12	RA1	13	RA0
	14-Pin SOIC	(SL)	1	14	4	RA3	12	RA1	13	RA0
	16-Pin VQFN	(ZPX)	16	13	3	RA3	11	RA1	12	RA0
PIC16F15243 PIC16F15244 PIC16F15245	20-Pin PDIP	(P)	1	20	4	RA3	18	RA1	19	RA0
	20-Pin SSOP	(SS)	1	20	4	RA3	18	RA1	19	RA0
	20-Pin SOIC	(SO)	1	20	4	RA3	18	RA1	19	RA0
	VQFN (3x3x0.9)	(REB)	18	17	1	RA3	15	RA1	16	RA0
PIC16F15254 PIC16F15255 PIC16F15256	28-pin SOIC	(SO)	20	8, 19	1	RE3	27	RB6	28	RB7
	28-pin SSOP	(SS)	20	8, 19	1	RE3	27	RB6	28	RB7
	28-pin VQFN	(4N)	17	5, 16	26	RE3	24	RB6	25	RB7
PIC16F15274 PIC16F15275 PIC16F15276	40-pin PDIP	(P)	11, 32	12, 31	1	RE3	39	RB6	40	RB7
	40-pin VQFN	(PNX)	7, 26	6, 27	16	RE3	14	RB6	15	RB7
	44-pin TQFP	(PT)	7, 28	6, 29	18	RE3	16	RB6	17	RB7

Note: The most current drawings are located in the Microchip Packaging Specification, DS00000049 (http://www.microchip.com/packaging).

6.1 CONFIG1

Name: CONFIG1
Offset: 0x8007

Configuration Word 1

Bit	15	14	13	12	11	10	9	8
				VDDAR				$\overline{\text{CLKOUTEN}}$
Access				R/W				R/W
Reset				1				1

Bit	7	6	5	4	3	2	1	0
			RSTOSC[1:0]				FEXTOSC[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	1			0	1

Bit 12 – VDDAR V_{DD} Analog Range Calibration Selection(1)

Value	Description
1	Internal analog systems are calibrated for operation between V_{DD} = 2.3V - 5.5V
0	Internal analog systems are calibrated for operation between V_{DD} = 1.8V - 3.6V

Bit 8 – $\overline{\text{CLKOUTEN}}$ Clock Out Enable

Value	Description
1	CLKOUT function is disabled; I/O function on CLKOUT pin
0	CLKOUT function is enabled; F_{OSC}/4 clock appears on CLKOUT pin

Bits 5:4 – RSTOSC[1:0] Power-up Default Value for COSC bits
Selects the oscillator source used by user software. Refer to COSC operation.

Value	Description
11	EXTOSC operating per the FEXTOSC bits
10	HFINTOSC with FRQ = 1 MHz
01	LFINTOSC
00	HFINTOSC with FRQ = 32 MHz

Bits 1:0 – FEXTOSC[1:0] External Oscillator Mode Selection

Value	Description
11	ECH (16 MHz and higher)
10	ECL (below 16 MHz)
01	Oscillator not enabled
00	Reserved

Note:

1. For the PIC16F152XX family, this bit only affects the SMBus 3.0 (1.35V) input threshold. If the SMBus 3.0 threshold is selected (see the RxyI2C registers for details), this bit should be configured according to the device's expected V_{DD} range.

6.2 CONFIG2

Name: CONFIG2
Offset: 0x8008

Configuration Word 2

Bit	15	14	13	12	11	10	9	8
			$\overline{\text{DEBUG}}$	STVREN	PPS1WAY		BORV	
Access			R/W	R/W	R/W		R/W	
Reset			1	1	1		1	

Bit	7	6	5	4	3	2	1	0
	BOREN[1:0]			WDTE[1:0]		PWRTS[1:0]		MCLRE
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	1	1		1	1	1	1	1

Bit 13 – $\overline{\text{DEBUG}}$ Debugger Enable(1)

Value	Description
1	Background debugger disabled
0	Background debugger enabled

Bit 12 – STVREN Stack Overflow/Underflow Reset Enable

Value	Description
1	Stack Overflow or Underflow will cause a Reset
0	Stack Overflow or Underflow will not cause a Reset

Bit 11 – PPS1WAY PPSLOCKED One-Way Set Enable

Value	Description
1	The PPSLOCKED bit can only be set once after an unlocking sequence is executed; once PPSLOCKED is set, all future changes to PPS registers are prevented
0	The PPSLOCKED bit can be set and cleared as needed (unlocking sequence is required)

Bit 9 – BORV Brown-out Reset (BOR) Voltage Selection(2)

Value	Description
1	Brown-out Reset voltage (V_{BOR}) set to 1.9V
0	Brown-out Reset voltage (V_{BOR}) set to 2.85V

Bits 7:6 – BOREN[1:0] Brown-out Reset (BOR) Enable(3)

Value	Description
11	Brown-out Reset enabled, SBOREN bit is ignored
10	Brown-out Reset enabled while running, disabled in Sleep; SBOREN bit is ignored
01	Brown-out Reset enabled according to SBOREN
00	Brown-out Reset disabled

Bits 4:3 – WDTE[1:0] Watchdog Timer (WDT) Enable

Value	Description
11	WDT enabled regardless of Sleep; SEN bit of WDTCON is ignored
10	WDT enabled while Sleep = 0, suspended when Sleep = 1; SEN bit if WDTCON is ignored
01	WDT enabled/disabled by the SEN bit of WDTCON
00	WDT disabled, SEN bit of WDTCON is ignored

Bits 2:1 – PWRTS[1:0] Power-Up Timer (PWRT) Selection

Value	Description
11	PWRT disabled

Value	Description
10	PWRT is set at 64 ms
01	PWRT is set at 16 ms
00	PWRT is set at 1 ms

Bit 0 – MCLRE Master Clear ($\overline{\text{MCLR}}$) Enable

Value	Condition	Description
x	If LVP = 1	$\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$
1	If LVP = 0	$\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$
0	If LVP = 0	$\overline{\text{MCLR}}$ pin function is port-defined function

Note:

1. The $\overline{\text{DEBUG}}$ bit is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.
2. The higher voltage selection is recommended for operation at or above 16 MHz.
3. When enabled, Brown-out Reset voltage (V_{BOR}) is set by the BORV bit.

6.3 CONFIG3

Name: CONFIG3
Offset: 0x8009

Configuration Word 3
Note: This register is Reserved and is not used in the PIC16F152XX family.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

6.4 CONFIG4

Name: CONFIG4
Offset: 0x800A

Configuration Word 4

Bit	15	14	13	12	11	10	9	8
			LVP		$\overline{\text{WRTSAF}}$		$\overline{\text{WRTC}}$	$\overline{\text{WRTB}}$
Access			R/W		R/W		R/W	R/W
Reset			1		1		1	1

Bit	7	6	5	4	3	2	1	0
	$\overline{\text{WRTAPP}}$			$\overline{\text{SAFEN}}$	$\overline{\text{BBEN}}$	BBSIZE[2:0]		
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	1			1	1	1	1	1

Bit 13 – LVP Low-Voltage Programming Enable(1)

Value	Description
1	Low-Voltage Programming is enabled. $\overline{\text{MCLR}}/V_{PP}$ pin function is $\overline{\text{MCLR}}$. The MCLRE bit is ignored.
0	High voltage (HV) on $\overline{\text{MCLR}}/V_{PP}$ must be used for programming.

Bit 11 – $\overline{\text{WRTSAF}}$ Storage Area Flash (SAF) Write Protection(2,3)

Value	Description
1	SAF is **NOT** write-protected
0	SAF is write-protected

Bit 9 – $\overline{\text{WRTC}}$ Configuration Registers Write-Protection(2)

Value	Description
1	Configuration registers are **NOT** write-protected
0	Configuration registers are write-protected

Bit 8 – $\overline{\text{WRTB}}$ Boot Block Write-Protection(2,4)

Value	Description
1	Boot Block is **NOT** write-protected
0	Boot Block is write-protected

Bit 7 – $\overline{\text{WRTAPP}}$ Application Block Write-Protection(2)

Value	Description
1	Application Block is **NOT** write-protected
0	Application Block is write-protected

Bit 4 – $\overline{\text{SAFEN}}$ Storage Area Flash (SAF) Enable(2)

Value	Description
1	SAF is disabled
0	SAF is enabled

Bit 3 – $\overline{\text{BBEN}}$ Boot Block Enable(2)

Value	Description
1	Boot Block is disabled
0	Boot Block is enabled

Bits 2:0 – BBSIZE[2:0] Boot Block Size Selection(5,6)

Table 6-2. Boot Block Size

$\overline{\text{BBEN}}$	BBSIZE	End Address of Boot Block	Boot Block Size (words)			
			PIC16F152x3	PIC16F152x4	PIC16F152x5	PIC16F152x6
1	xxx	–	–			
0	111	01FFh	512			
0	110	03FFh	1024			
0	101	07FFh	–(6)	2048		
0	100	0FFFh	–(6)		4096	
0	011	1FFFh	–(6)			8192
0	010	3FFFh	–(6)			
0	001	3FFFh	–(6)			
0	000	3FFFh	–(6)			

Note:

1. The LVP bit cannot be written (to zero) while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the Configuration state.
2. Once protection is enabled through ICSP™ or a self-write, it can only be reset through a Bulk Erase.
3. Applicable only if $\overline{\text{SAFEN}}$ = 0.
4. Applicable only if $\overline{\text{BBEN}}$ = 0.
5. BBSIZE[2:0] bits can only be changed when $\overline{\text{BBEN}}$ = 1. Once $\overline{\text{BBEN}}$ = 0, BBSIZE[2:0] can only be changed through a Bulk Erase.
6. The maximum boot block size is half of the user program memory size. Any selection that will exceed the half of a device's program memory will default to a maximum boot block size of half PFM. For example, all settings of BBSIZE from '110' to '000' for a PIC16F15213 (Max PFM = 2048 words) will result in a maximum boot block size of 1024 words.

6.5 CONFIG5

Name: CONFIG5
Offset: 0x800B

Configuration Word 5[1]

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								$\overline{CP}$
Access								R/W
Reset								1

Bit 0 – $\overline{CP}$ User Program Flash Memory (PFM) Code Protection[2]

Value	Description
1	User PFM code protection is disabled
0	User PFM code protection is enabled

Note:

1. Since device code protection takes effect immediately, this Configuration Word should be written last.
2. Once code protection is enabled it can only be removed through a Bulk Erase.

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