CY7C1345A/GVT71128E36

128K x 36 Synchronous Flow-Through Burst SRAM

Features

- **Fast access times: 7.5 and 8 ns**
- **Fast clock speed: 117 and 100 MHz**
- **Provide high-performance 2-1-1-1 access rate**
- **Fast OE access times: 4.0 ns**
- **3.3V –5% and +10% power supply**
- **2.5V or 3.3V I/O supply**
- **5V tolerant inputs except I/Os**
- **Clamp diodes to V_{SSQ} at all inputs and outputs**
- **Common data inputs and data outputs**
- **Byte Write Enable and Global Write control**
- **Three chip enables for depth expansion and address pipeline**
- **Address, data, and control registers**
- **Internally self-timed Write Cycle**
- **Burst control pins (interleaved or linear burst sequence)**
- **Automatic power-down for portable applications**
- **Low profile 119-lead, 14-mm x 22-mm BGA (Ball Grid Array) and 100-pin TQFP packages**

Functional Description

The Cypress Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1345A/GVT71128E36 SRAM integrates 131,072x36 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE}$), depth-expansion Chip Enables ($\overline{CE2}$ and CE2), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{WEL}$, $\overline{WEH}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$).

Asynchronous inputs include the Output Enable ($\overline{OE}$) and Burst Mode Control (MODE), and Sleep Mode Control (ZZ). The data outputs (DQ), enabled by $\overline{OE}$, are also asynchronous.

Addresses and chip enables are registered with either Address Status Processor ($\overline{ADSP}$) or Address Status Controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance pin ($\overline{ADV}$).

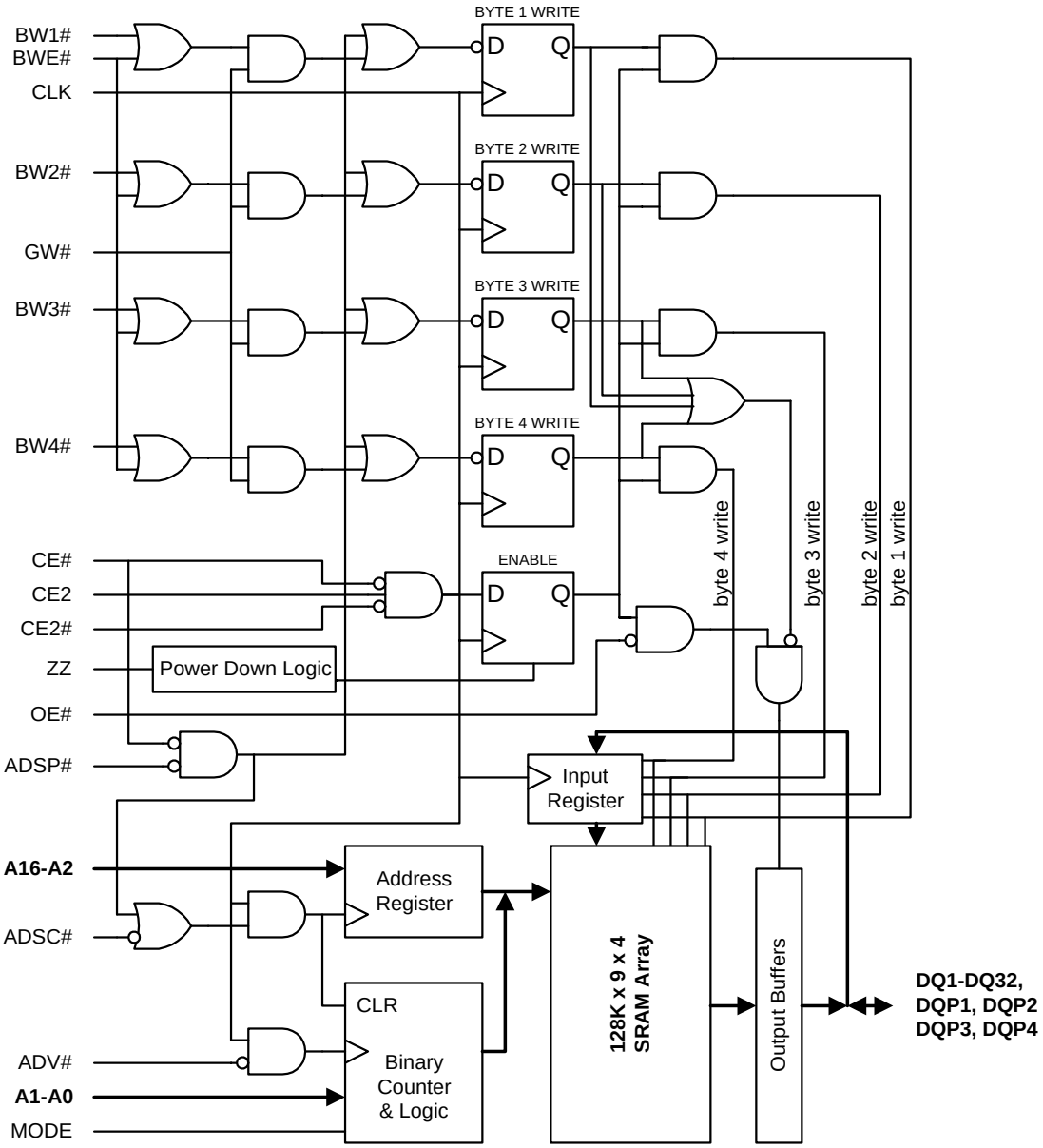
Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle. Write cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. BW1 controls DQ1–DQ8 and DQP1. $\overline{BW2}$ controls DQ9–DQ16 and DQP2. $\overline{BW3}$ controls DQ17–DQ24 and DQP3. $\overline{BW4}$ controls DQ25–DQ32 and DQP4. $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, and $\overline{BW4}$ can be active only with $\overline{BWE}$ being LOW. $\overline{GW}$ being LOW causes all bytes to be written.

The CY7C1345A/GVT71128E36 operates from a +3.3V power supply and all outputs operate on a +2.5V supply. All inputs and outputs are JEDEC standard JESD8-5 compatible. The device is ideally suited for 486, Pentium®, 680x0, and PowerPC™ systems and for systems that benefit from a wide synchronous data bus.

Selection Guide

	7C1345A-117 71128E36-7	7C1345A-100 71128E36-8	7C1345A-100 71128E36-9	7C1345A-100 71128E36-10
Maximum Access Time (ns)	7.5	8	8	8
Maximum Operating Current (mA)	370	320	320	320
Maximum CMOS Standby Current (mA)	10	10	10	10

128K x 36 (CY7C1345A/GVT71128E36) Functional Block Diagram[1]

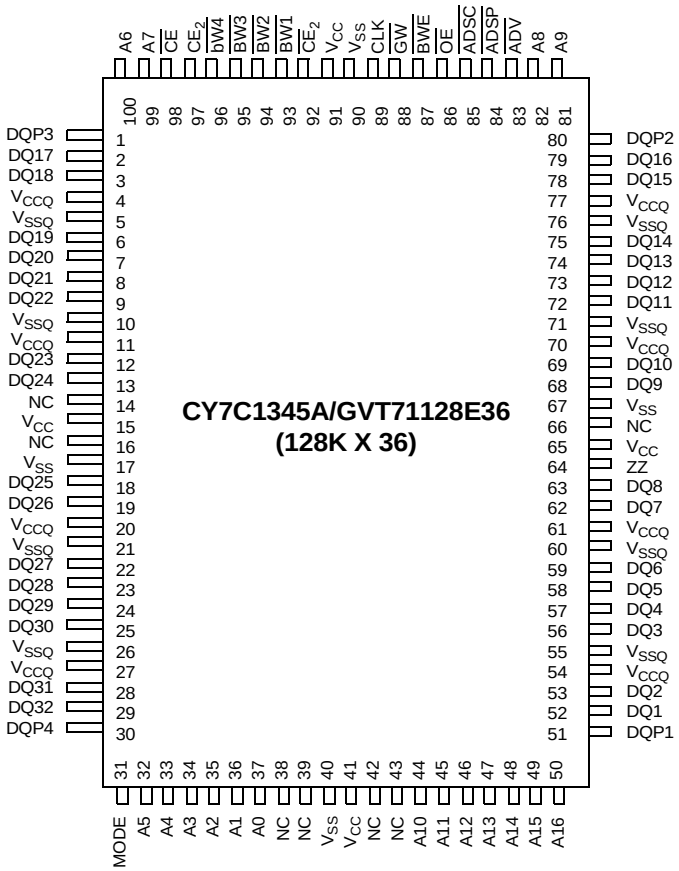


Note:

1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions, and timing diagrams for detailed information.

Pin Configurations

100-Pin TQFP
Top View



Pin Configurations (continued)

119-Ball Bump BGA

128Kx36—CY7C1345A/GVT71128E36
Top View

	1	2	3	4	5	6	7
A	V_{CCQ}	A6	A4	$\overline{ADSP}$	A8	A16	V_{CCQ}
B	NC	CE2	A3	$\overline{ADSC}$	A9	$\overline{CE2}$	NC
C	NC	A7	A2	V_{CC}	A12	A15	NC
D	DQ17	DQP3	V_{SS}	NC	V_{SS}	DQP2	DQ16
E	DQ18	DQ19	V_{SS}	$\overline{CE}$	V_{SS}	DQ14	DQ15
F	V_{CCQ}	DQ20	V_{SS}	$\overline{OE}$	V_{SS}	DQ13	V_{CCQ}
G	DQ21	DQ22	$\overline{BW3}$	$\overline{ADV}$	$\overline{BW2}$	DQ12	DQ11
H	DQ23	DQ24	V_{SS}	$\overline{GW}$	V_{SS}	DQ10	DQ9
J	V_{CCQ}	V_{CC}	NC	V_{CC}	NC	V_{CC}	V_{CCQ}
K	DQ25	DQ27	V_{SS}	CLK	V_{SS}	DQ7	DQ8
L	DQ26	DQ28	$\overline{BW4}$	NC	$\overline{BW1}$	DQ5	DQ6
M	V_{CCQ}	DQ29	V_{SS}	$\overline{BWE}$	V_{SS}	DQ4	V_{CCQ}
N	DQ30	DQ31	V_{SS}	A1	V_{SS}	DQ3	DQ2
P	DQ32	DQP4	V_{SS}	A0	V_{SS}	DQP1	DQ1
R	NC	A5	MODE	V_{CC}	NC	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ
U	V_{CCQ}	NC	NC	NC	NC	NC	V_{CCQ}

Pin Descriptions

BGA Pins	QFP Pins	Pin Name	Type	Description
4P, 4N, 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 3T, 4T, 5T	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49,50	A0–A16	Input-Synchronous	Addresses: These inputs are registered and must meet the set-up and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
5L, 5G, 3G, 3L	93,94,95,96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, BW4	Input-Synchronous	Byte Write: A byte write is LOW for a Write cycle and HIGH for a Read cycle. $\overline{BW1}$ controls DQ1–DQ8 and DQP1. $\overline{BW2}$ controls DQ9–DQ16 and DQP2. $\overline{BW3}$ controls DQ17–DQ24 and DQP3. $\overline{BW4}$ controls DQ25–DQ32 and DQP4. Data I/O are high impedance if either of these inputs are LOW, conditioned by $\overline{BWE}$ being LOW.
4M	87	$\overline{BWE}$	Input-Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the set-up and hold times around the rising edge of CLK.
4H	88	$\overline{GW}$	Input-Synchronous	Global Write: This active LOW input allows a full 36-bit Write to occur independent of the $\overline{BWE}$ and $\overline{BWn}$ lines and must meet the set-up and hold times around the rising edge of CLK.
4K	89	CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.

Pin Descriptions (continued)

BGA Pins	QFP Pins	Pin Name	Type	Description
4E	98	$\overline{CE}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device and to gate $\overline{ADSP}$.
6B	92	$\overline{CE2}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device.
2B	97	CE2	Input-Synchronous	Chip Enable: This active HIGH input is used to enable the device.
4F	86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
4G	83	$\overline{ADV}$	Input-Synchronous	Address Advance: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
4A	84	$\overline{ADSP}$	Input-Synchronous	Address Status Processor: This active LOW input, along with $\overline{CE}$ being LOW, causes a new external address to be registered and a Read cycle is initiated using the new address.
4B	85	$\overline{ADSC}$	Input-Synchronous	Address Status Controller: This active LOW input causes device to be deselected or selected along with new external address to be registered. A Read or Write cycle is initiated depending upon write control inputs.
3R	31	MODE	Input-Static	Mode: This input selects the burst sequence. A LOW on this pin selects Linear Burst. A NC or HIGH on this pin selects Interleaved Burst.
7T	64	ZZ	Input-Asynchronous	Snooze: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (No Connect).
7P, 7N, 6N, 6M, 6L, 7L, 6K, 7K, 7H, 6H, 7G, 6G, 6F, 6E, 7E, 7D, 1D, 1E, 2E, 2F, 1G, 2G, 1H, 2H, 1K, 1L, 2K, 2L, 2M, 1N, 2N, 1P	52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72-75, 78, 79, 2, 3, 6-9, 12, 13, 18, 19, 22-25, 28, 29	DQ1–DQ32	Input/Output	Data Inputs/Outputs: First Byte is DQ1–DQ8. Second Byte is DQ9–DQ16. Third Byte is DQ17–DQ24. Fourth Byte is DQ25–DQ32. Input data must meet set-up and hold times around the rising edge of CLK.
6P, 6D, 2D, 2P	51, 80, 1, 30	DQP1–DQP4	Input/Output	Parity Inputs/Outputs: DQP1 is parity bit for DQ1–DQ8 and DQP2 is parity bit for DQ9–DQ16. DQP3 is parity bit for DQ17–DQ24 and DQP4 is parity bit for DQ25–DQ32.
4C, 2J, 4J, 6J, 4R	15, 41,65, 91	V_{CC}	Supply	Core power Supply: +3.3V –5% and +10%
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	17, 40, 67, 90	V_{SS}	Ground	Ground: GND
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	4, 11, 20, 27, 54, 61, 70, 77	V_{CCQ}	I/O Supply	Output Buffer Supply: +2.5V (from 2.375V to V_{CC})
	5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	I/O Ground	Output Buffer Ground: GND
1B, 7B, 1C, 7C, 4D, 3J, 5J, 4L, 1R, 5R, 7R, 1T, 2T, 6T, 2U, 3U, 4U, 5U, 6U	14, 16, 38, 39, 42, 43, 66	NC	-	No Connect: These signals are not internally connected.

Burst Address Table (MODE = NC/V_{CC})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

Burst Address Table (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

Truth Table[2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Notes:

2. X means "Don't Care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$ = L means [$\overline{BWE}$ + $\overline{BW1}$*$\overline{BW2}$*$\overline{BW3}$*$\overline{BW3}$]*$\overline{GW}$ equals LOW. $\overline{WRITE}$ = H means [$\overline{BWE}$ + BW1*BW2*BW3*BW3]*GW equals HIGH.
3. BW1 enables write to DQ1–DQ8 and DQP1. BW2 enables write to DQ9–DQ16 and DQP2. $\overline{BW3}$ enables write to DQ17–DQ24 and DQP3. $\overline{BW4}$ enables write to DQ25–DQ32 and DQP4.
4. All inputs except $\overline{OE}$ must meet set-up and hold times around the rising edge (LOW to HIGH) of CLK.
5. Suspending burst generates wait cycle.
6. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required set-up time plus High-Z time for $\overline{OE}$ and staying HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP LOW along with chip being selected always initiates a Read cycle at the L-H edge of CLK. A Write cycle can be performed by setting $\overline{WRITE}$ LOW for the CLK L-H edge of the subsequent wait cycle. Refer to Write timing diagram for clarification.

Partial Truth Table for Read/Write

FUNCTION	GW	BWE	BW1	BW2	BW3	BW4
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE one byte	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines only, not tested.)

Voltage on V_{CC} Supply Relative to V_{SS} ..... –0.5V to +4.6V

V_{IN}.....–0.5V to +V_{CC}+0.5V

Storage Temperature (plastic).....–55°C to +125°C

Junction Temperature .....+125°C

Power Dissipation..... 1.6W

Short Circuit Output Current ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}[9,10]
Com'l	0°C to +70°C	3.3V –5%/+10%

Electrical Characteristics Over the Operating Range[11]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IHD}	Input High (Logic 1) Voltage[12, 13]	Data Inputs (DQxx)	1.7	V_{CC}+0.3	V
V_{IH}		All other	1.7	4.6	V
V_{Il}	Input Low (Logic 0) Voltage[12, 13]		–0.3	0.7	V
IL_I	Input Leakage Current[14]	$0V \le V_{IN} \le V_{CC}$	–2	2	µA
IL_O	Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	–2	2	µA
V_{OH}	Output High Voltage[12, 15]	I_{OH} = –2.0 mA	1.7		V
V_{OL}	Output Low Voltage[12, 15]	I_{OL} = 2.0 mA		0.7	V
V_{CC}	Supply Voltage[12]		3.135	3.6	V
V_{CCQ}	I/O Supply Voltage		2.375	V_{CC}	V

Parameter	Description	Conditions	Typ.	-7 117 MHz	-8 100 MHz	-9 90 MHz	-10 50 MHz	Unit
I_{CC}	Power Supply Current: Operating[16, 17, 18]	Device selected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; cycle time $\ge t_{KC}$ Min.; V_{CC} = Max.; outputs open	150	370	320	290	200	mA
I_{SB2}	CMOS Standby[17, 18]	Device deselected; V_{CC} = Max.; all inputs $\le V_{SS}$ + 0.2 or $\ge V_{CC}$ – 0.2; all inputs static; CLK frequency = 0	5	10	10	10	10	mA
I_{SB3}	TTL Standby[17, 18]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; all inputs static; V_{CC} = Max.; CLK frequency = 0	10	20	20	20	20	mA
I_{SB4}	Clock Running[17, 18]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; V_{CC} = Max.; CLK cycle time $\ge t_{KC}$ Min.	40	80	70	60	40	mA

Notes:

9. Please refer to waveform (c)
10. Power Supply ramp-up should be monotonic.
11. Values in table are associated with the operating frequencies listed.
12. All voltages referenced to V_{SS} (GND).
13. Overshoot: $V_{IH} \le +6.0V$ for $t \le t_{KC}/2$.
    Undershoot: $V_{IL} \le –2.0V$ for $t \le t_{KC}/2$.
14. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±30 µA.
15. AC I/O curves are available upon request.
16. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
17. "Device Deselected" means the device is in Power-Down mode as defined in the truth table. "Device Selected" means the device is active.
18. Typical values are measured at 3.3V, 25°C and 20-ns cycle time.

Thermal Consideration

Parameter	Description	Conditions	TQFP Typ.	Unit
Θ_{JA}	Thermal Resistance - Junction to Ambient	Still air, soldered on 4.25 x 1.125 inch 4-layer PCB	25	°C/W
Θ_{JC}	Thermal Resistance - Junction to Case		9	°C/W

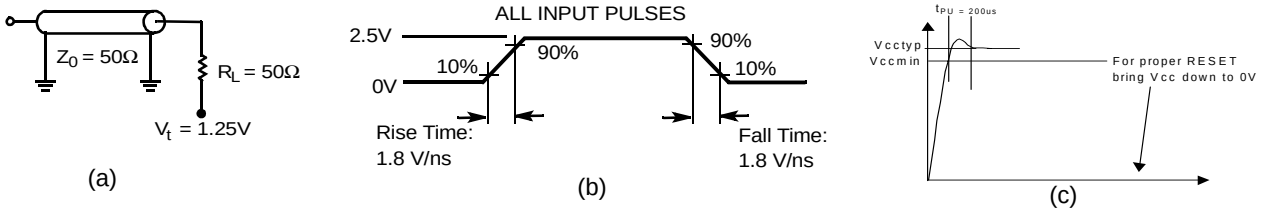
Capacitance

Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_I	Input Capacitance[19]	T_A = 25°C, f = 1 MHz, V_{CC}= 3.3V	4	5	pF
C_O	Input/Output Capacitance (DQ)[19]		7	8	pF

Typical Output Buffer Characteristics

Output High Voltage	Pull-up Current		Output Low Voltage	Pull-down Current	
V_{OH} (V)	I_{OH} (mA) Min.	I_{OH} (mA) Max.	V_{OL} (V)	I_{OL} (mA) Min.	I_{OL} (mA) Max.
–0.5	–38	–105	–0.5	0	0
0	–38	–105	0	0	0
0.8	–38	–105	0.4	10	20
1.25	–26	–83	0.8	20	40
1.5	–20	–70	1.25	31	63
2.3	0	–30	1.6	40	80
2.7	0	–10	2.8	40	80
2.9	0	0	3.2	40	80
3.4	0	0	3.4	40	80

AC Test Loads and Waveforms



Note:

19. This parameter is sampled.
20. Overshoot: VIH(AC) <VDD + 1.5V for t <tTCYC/2; undershoot: VIL(AC) < 0.5V for t <tTCYC/2; power-up: VIH < 2.6V and VDD <2.4V and VDDQ < 1.4V for t<200 ms.

Switching Characteristics Over the Operating Range[21]

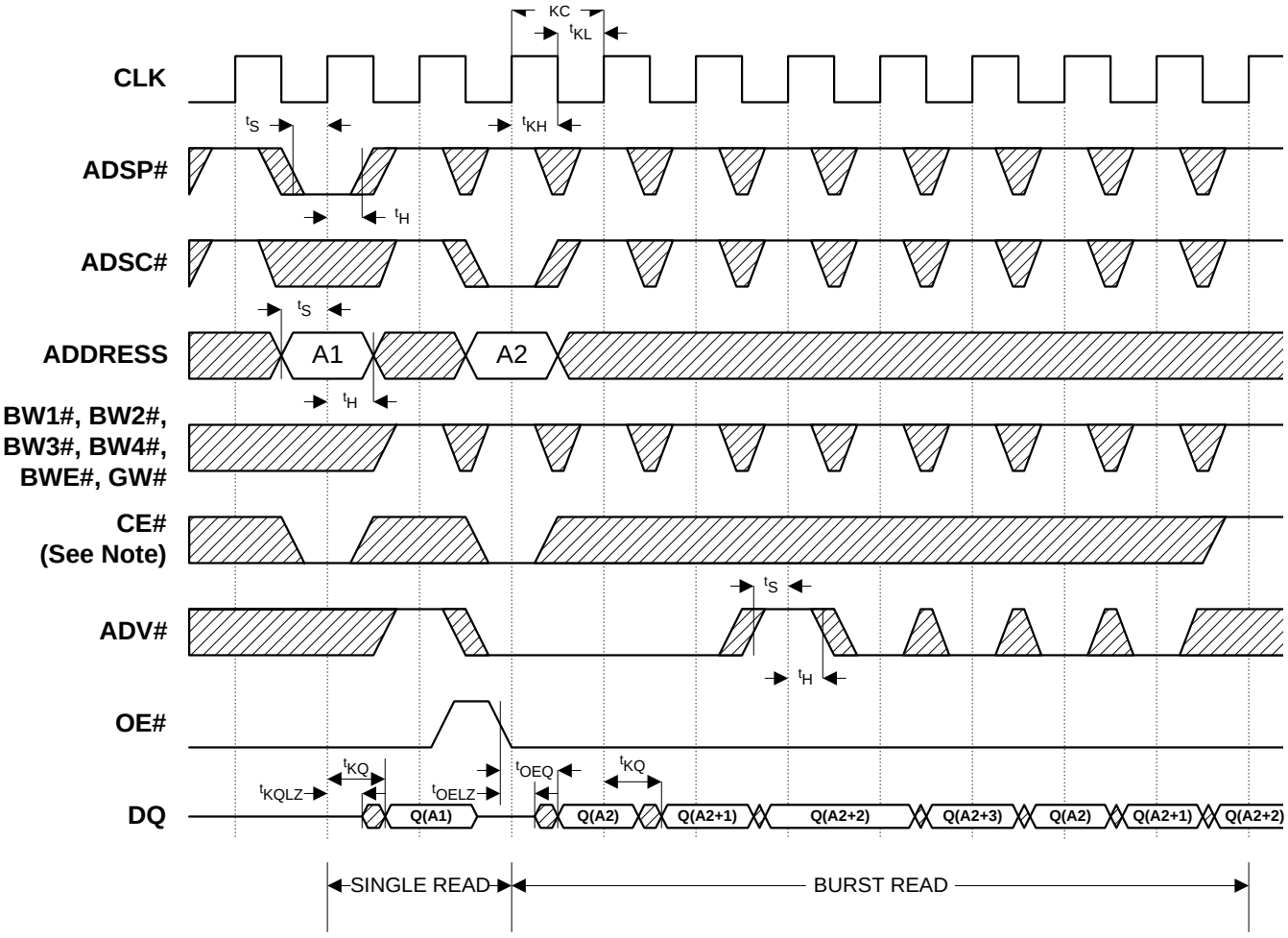
Parameter	Description	-7 117 MHz		-8 100 MHz		-9 90 MHz		-10 50 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock										
t_{KC}	Clock Cycle Time	8.5		10		11		20		ns
t_{KH}	Clock HIGH Time	3		4		4.5		4.5		ns
t_{KL}	Clock LOW Time	3		4		4.5		4.5		ns
Output Times										
t_{KQ}	Clock to Output Valid		7.5		8		8.5		10	ns
t_{KQX}	Clock to Output Invalid	2		2		2		2		ns
t_{KQLZ}	Clock to Output in Low-Z[19, 22, 23]	0		0		0		0		ns
t_{KQHZ}	Clock to Output in High-Z[19, 22, 23]	2	3.5	2	3.5	2	3.5	2	3.5	ns
t_{OEQ}	OE to Output Valid[24]		4.0		4.0		4.0		4.0	ns
t_{OELZ}	OE to Output in Low-Z[19, 22, 23]	0		0		0		0		ns
t_{OEHZ}	OE to Output in High-Z[19, 22, 23]		3.5		3.5		3.5		3.5	ns
Set-Up Times										
t_S	Address, Controls and Data In[25]	1.5		2.0		2.0		2.0		ns
Hold Times										
t_H	Address, Controls and Data In[25]	0.5		0.5		0.5		0.5		ns

Notes:

21. Test conditions as specified with the output loading as shown in AC Test Loads unless otherwise noted. Values in table are associated with the operating frequencies listed.
22. Measured at ±200 mV from steady state.
23. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
24. $\overline{OE}$ is a “Don’t Care” when a byte write enable is sampled LOW.
25. This is a synchronous device. All synchronous inputs must meet specified set-up and hold time, except for “Don’t Care” as defined in the truth table.

Timing Diagrams

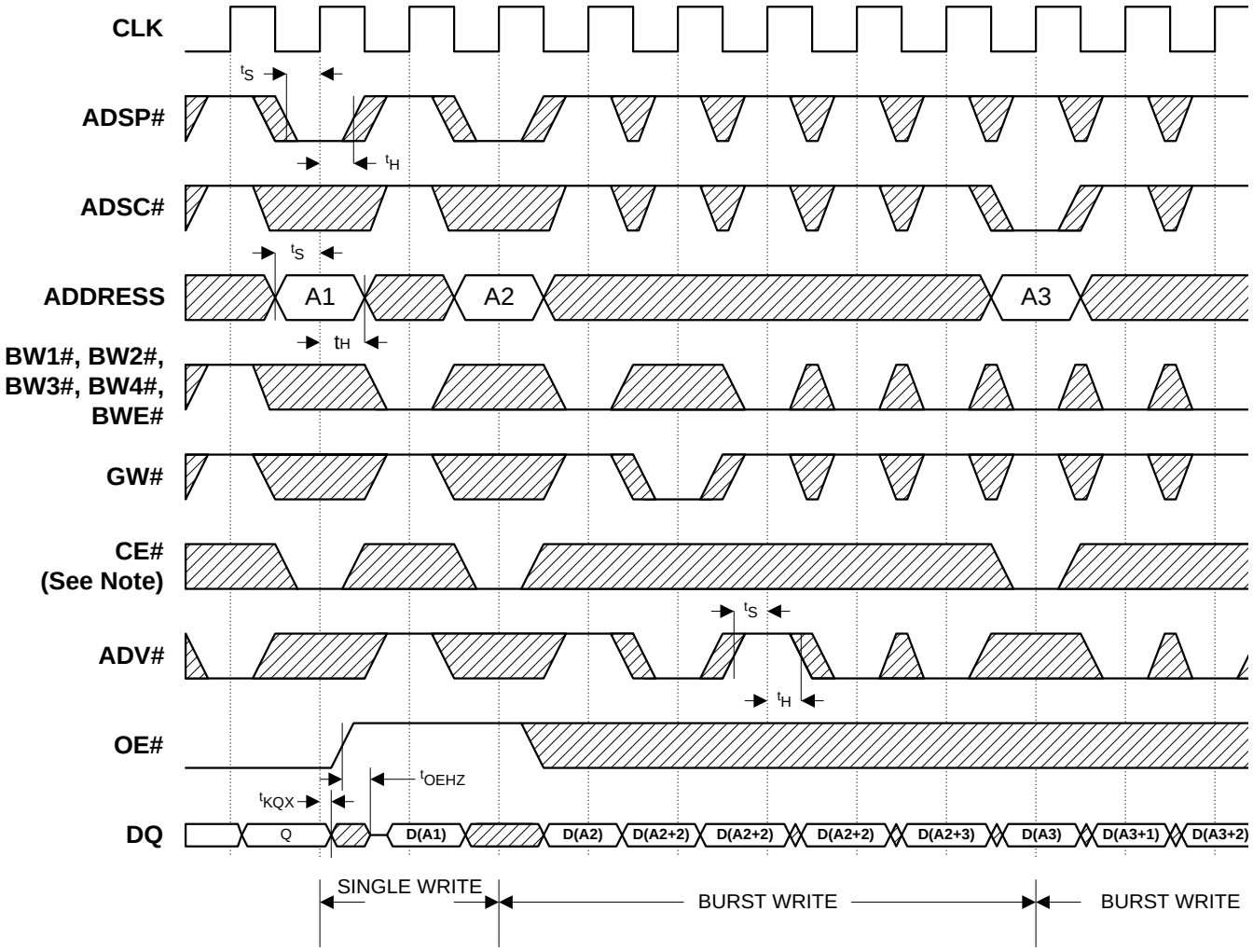
Read Timing[26]



Note:
26. $\overline{CE}$ active in this timing diagram means that all Chip Enables $\overline{CE}$, $\overline{CE2}$, and CE2 are active.

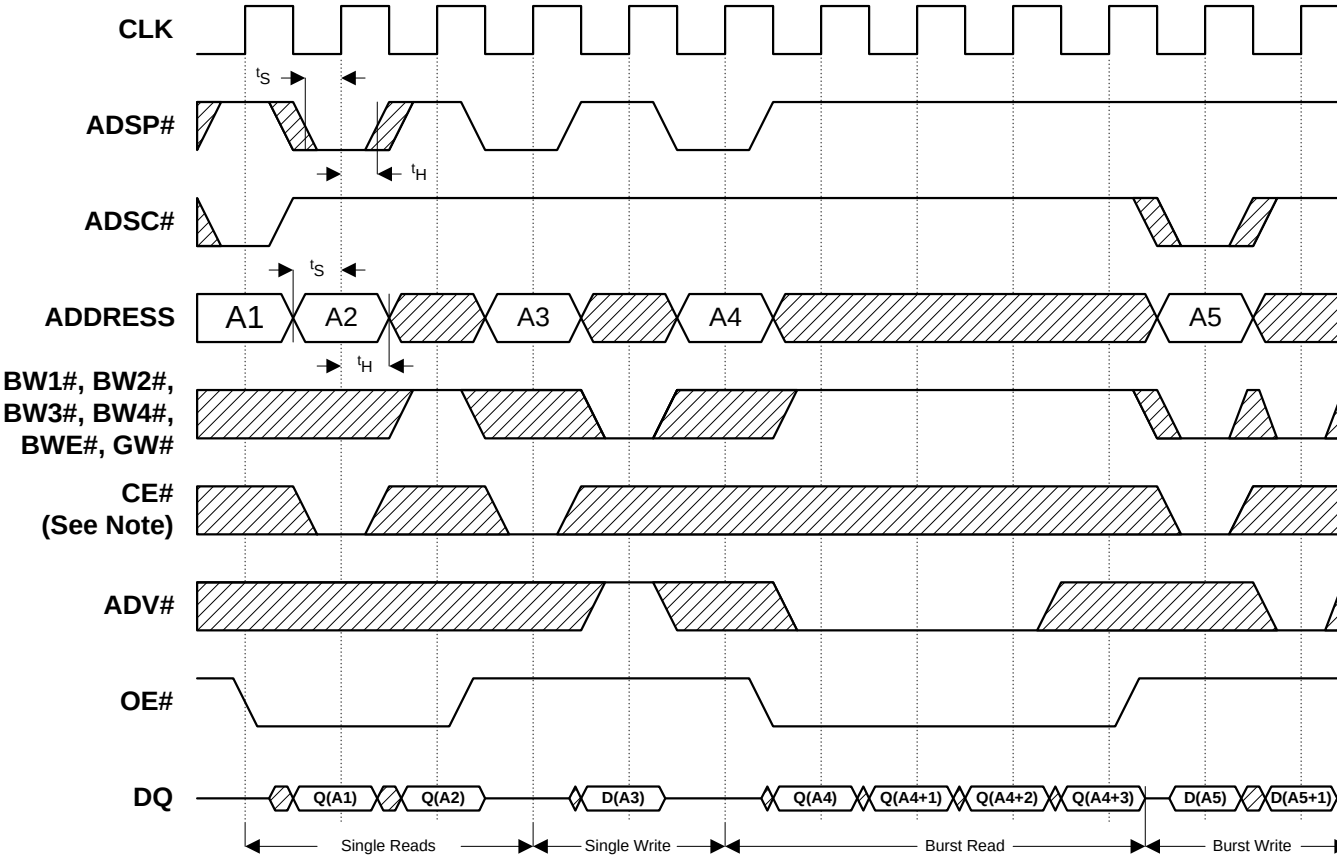
Timing Diagrams (continued)

Write Timing[26]



Timing Diagrams (continued)

Read/Write Timing[26]

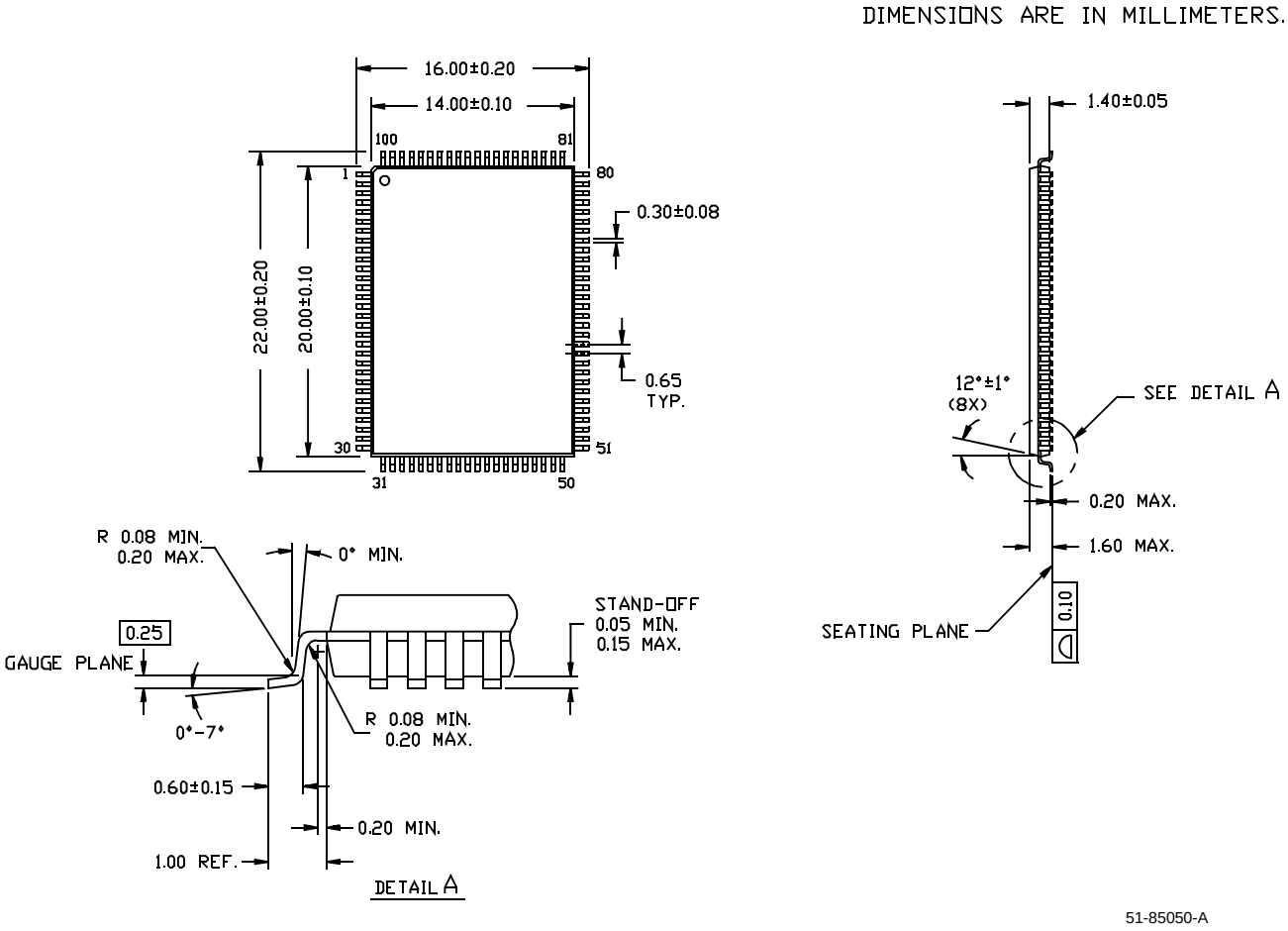


Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
117	CY7C1345A-117AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT71128E36T-7			
	CY7C1345A-117BGC	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
	GVT71128E36B-7			
100	CY7C1345A-100AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT71128E36T-8			
	CY7C1345A-100BGC	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
	GVT71128E36B-8			
100	CY7C1345A-100AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT71128E36T-9			
	CY7C1345A-100BGC	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
	GVT71128E36B-9			
100	CY7C1345A-100AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT71128E36T-10			
	CY7C1345A-100BGC	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
	GVT71128E36B-10			

Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



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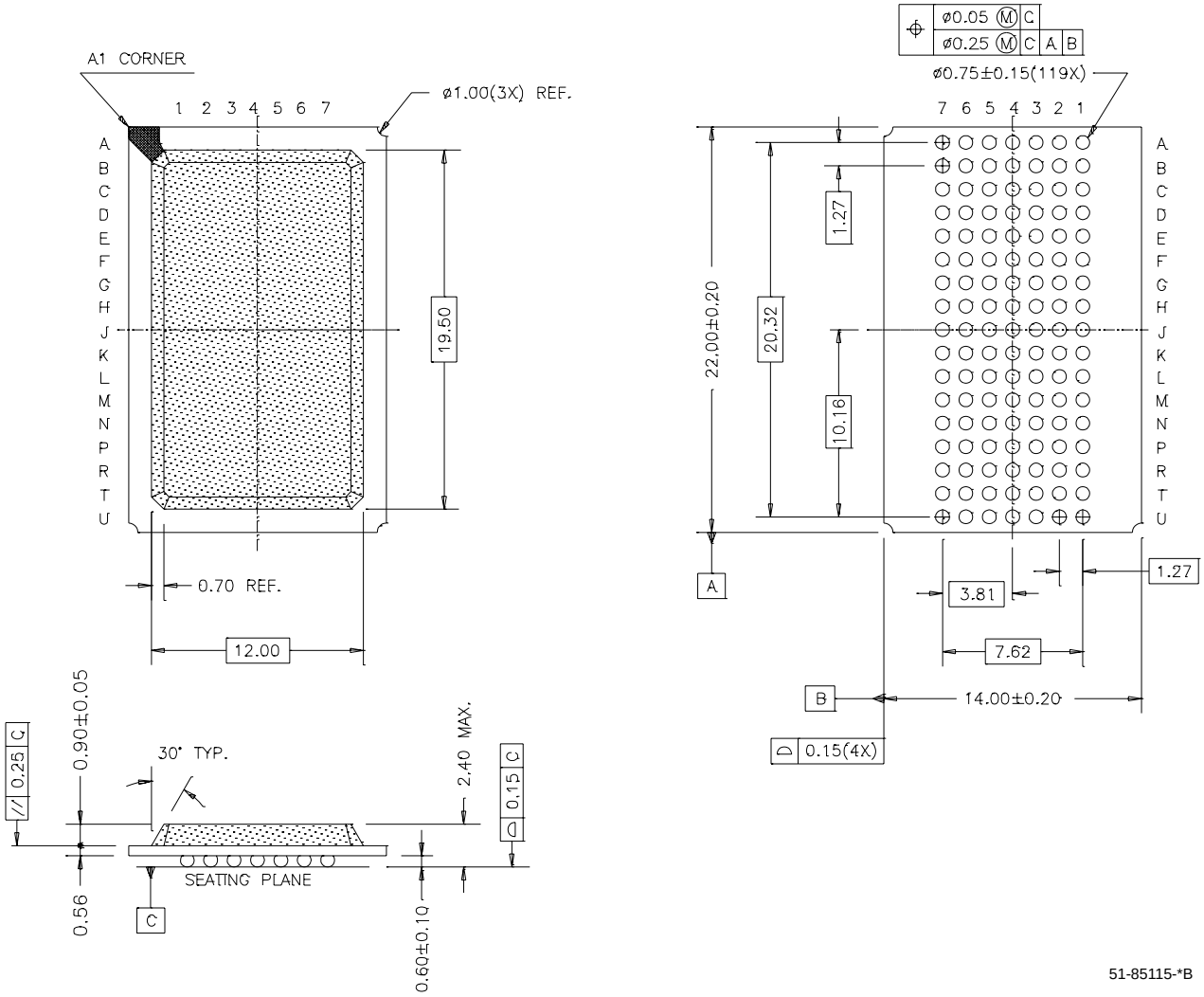
Package Diagrams (continued)

119-Lead PBGA (14 x 22 x 2.4 mm) BG119



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Document History Page

Document Title: CY7C1345A/GVT71128E36 128K x 36 Synchronous Flow-Through Burst SRAM Document Number: 38-05123				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	108314	09/25/01	BRI	New Cypress spec—converted from Galvantech format
*A	121069	11/13 /02	DSG	Updated package drawing 51-85115 (BG119) to rev. *B
*B	123136	01/19/03	RBI	Added power up requirements to operating conditions information.