

## DESCRIPTION

The MPQ2451-5/33 is a high-frequency, step-down, switching regulator with an integrated, high-voltage, high-side power MOSFET. It efficiently outputs up to 0.6A, with current-mode control for fast loop response.

The wide 3.3V-to-36V input range accommodates a variety of automotive step-down applications, and the 3 $\mu$ A shutdown-mode quiescent current allows use in battery-powered applications.

The MPQ2451-5/33 achieves high power-conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

Frequency fold-back prevents inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

The MPQ2451-5/33 is available in cost-effective SOT23-6L and QFN-6L packages.

## FEATURES

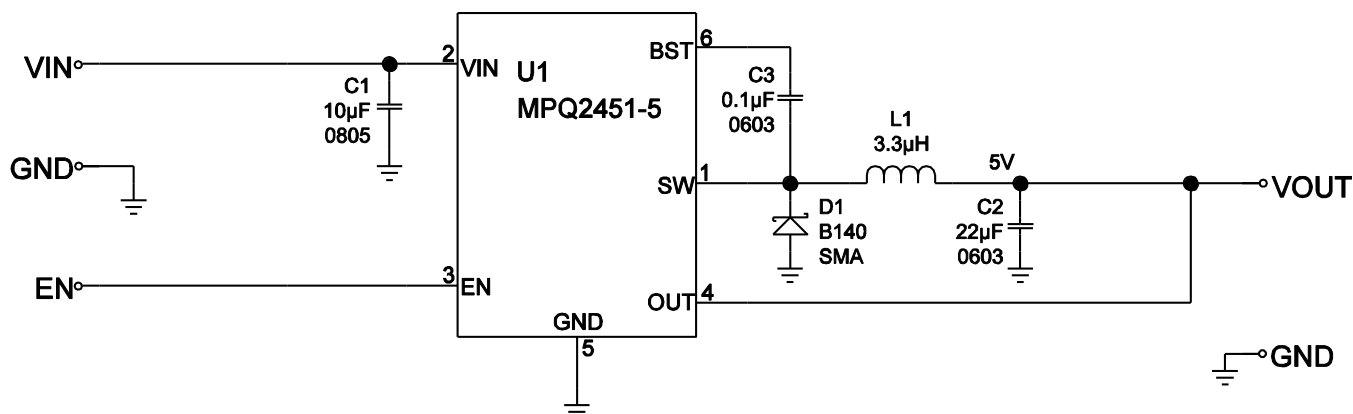
- Guaranteed Industrial/Automotive Temp. Ranges
- 130 $\mu$ A Operating Quiescent Current
- Wide 3.3V-to-36V Operating Input Range
- 500m $\Omega$  Internal Power MOSFET
- 2.2MHz Fixed Switching Frequency
- Internally Compensated
- Stable with Ceramic Output Capacitors
- Internal Soft-Start
- Precision Current Limit Without Current Sensing Resistor
- >90% Efficiency
- Fixed 5V & 3.3V Outputs
- 6-Lead SOT23 and QFN Packages
- Available in AEC-Q100 Grade 1

## APPLICATIONS

- High-Voltage Power Conversion, Including
  - Automotive Systems
  - Industrial Power Systems
  - Distributed Power Systems
  - Battery-Powered Systems

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## TYPICAL APPLICATION



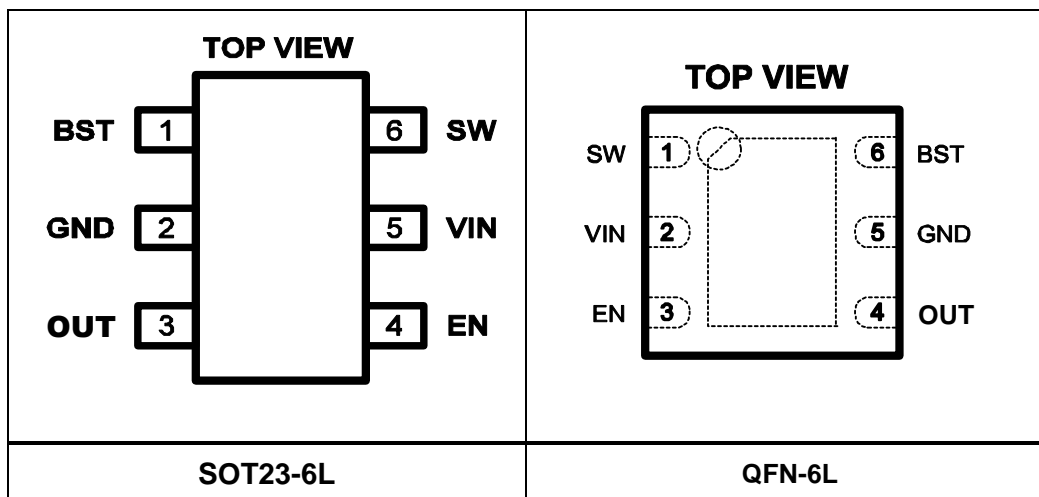
## ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ2451GT-5*	SOT23-6L	AGE
MPQ2451GT-5-AEC1		
MPQ2451GT-33**		AGF
MPQ2451GT-33-AEC1		
MPQ2451GG-5	QFN-6L	BP
MPQ2451GG-5-AEC1		
MPQ2451GG-33		BQ
MPQ2451GG-33-AEC1		

\* For Tape & Reel, add suffix -Z (e.g. MPQ2451GT-5-AEC1-Z)

\*\* For Tape & Reel, add suffix -Z (e.g. MPQ2451GT-33-Z)

## PACKAGE REFERENCE



### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Supply Voltage ( $V_{IN}$ )..... -0.3V to +40V  
 Switch Voltage ( $V_{SW}$ )..... -0.3V to ( $V_{IN}+0.3V$ )  
 BST to SW..... -0.3 to +5.0V  
 All Other Pins..... -0.3V to +5.0V  
 Continuous Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2)</sup>  
 SOT23-6L.....0.57W  
 QFN-6L.....1.56W  
 Junction Temperature..... 150°C  
 Lead Temperature..... 260°C  
 Storage Temperature..... -65°C to +150°C

### Recommended Operating Conditions <sup>(3)</sup>

Supply Voltage  $V_{IN}$ ..... 3.3V to 36V  
 Operating Junction Temp. ( $T_J$ ). -40°C to +125°C

### Thermal Resistance <sup>(4)</sup> $\theta_{JA}$ $\theta_{JC}$

SOT23-6L.....220 .... 110 ...°C/W  
 QFN-6L.....80 ..... 16 ...°C/W

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) = ( $T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_J = 25^{\circ}C$ .

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Voltage	MPQ2451-5	$6V < V_{IN} < 36V$	4.8	5	5.2	V
		$6V < V_{IN} < 36V$ , $T_J = 25^{\circ}C$	4.85	5	5.15	
	MPQ2451-33	$3.3V < V_{IN} < 36V$	3.168	3.3	3.432	V
		$3.3V < V_{IN} < 36V$ , $T_J = 25^{\circ}C$	3.2	3.3	3.4	
Upper Switch-On Resistance	$R_{DS(ON)}$	$V_{BST} - V_{SW} = 5V$ $T_J = 25^{\circ}C$		500		m $\Omega$
Upper Switch Leakage		$V_{EN} = 0V$ , $V_{SW} = 0V$		0.5	2	$\mu A$
Current Limit	$I_{LIM}$	$T_J = 25^{\circ}C$	0.75	1		A
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	0.65			
COMP to Current Sense Transconductance <sup>(5)</sup>	$G_{CS}$			3		A/V
$V_{IN}$ UVLO, Upper Threshold			2.7		3.29	V
$V_{IN}$ UVLO, Hysteresis				0.4		V
Soft-Start Time				0.5	1	ms
Oscillator Frequency	$f_{SW}$		1.8	2.2	2.6	MHz
Minimum Switch-On Time <sup>(5)</sup>	$\tau_{ON}$			80		ns
Shutdown Supply Current	$I_S$	$V_{EN} < 0.3V$			1	$\mu A$
Quiescent Supply Current	$I_Q$	No load, no switching		130	170	$\mu A$
Thermal Shutdown <sup>(5)</sup>				150		$^{\circ}C$
Enable Threshold, High	$V_{IH}$	Low-to-High	1.35	1.5	1.8	V
Enable Threshold, Hysteresis				400		mV

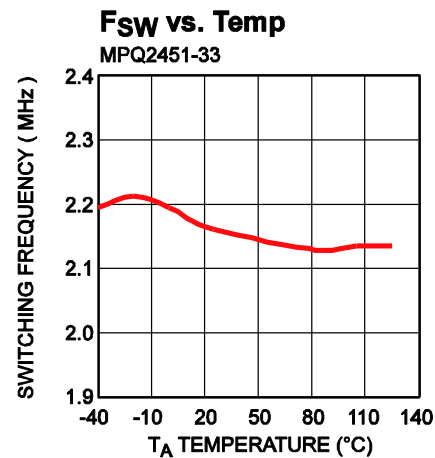
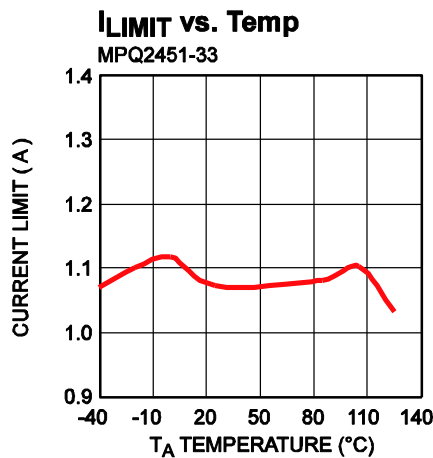
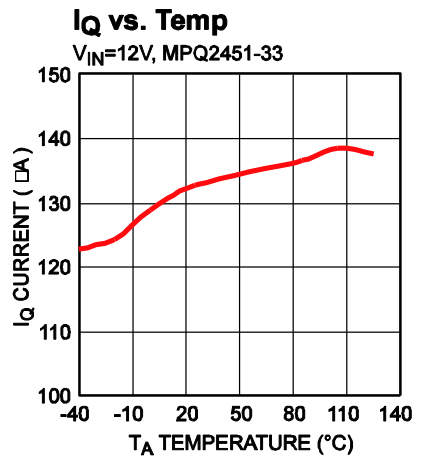
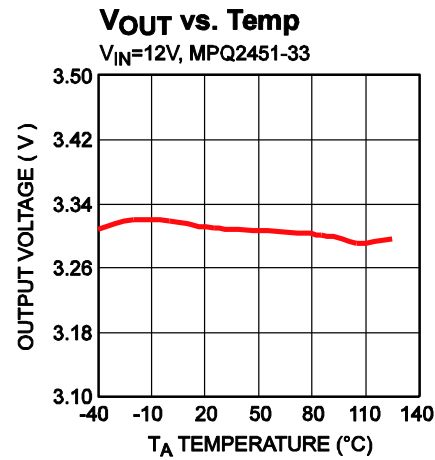
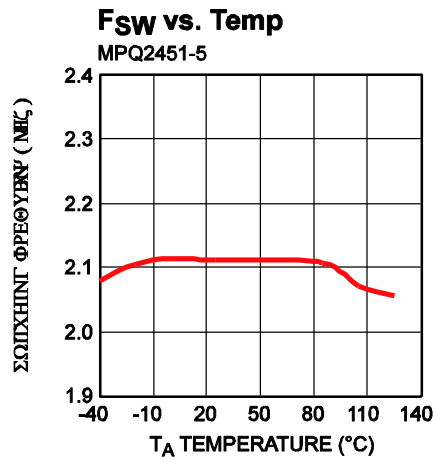
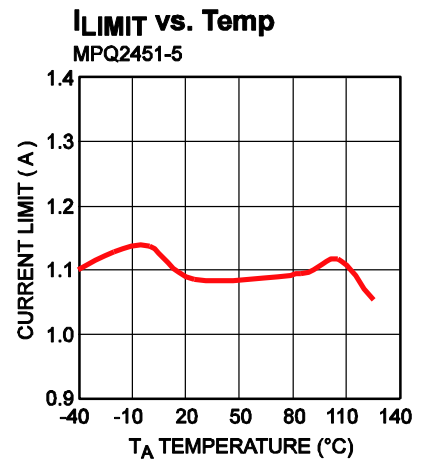
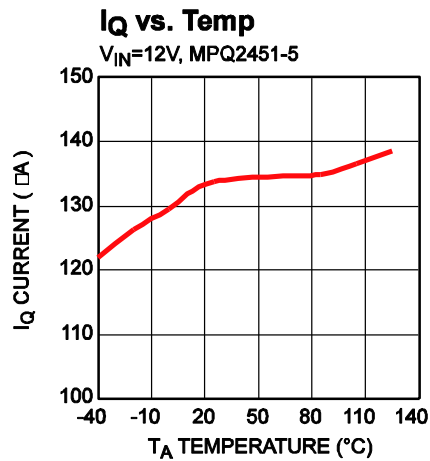
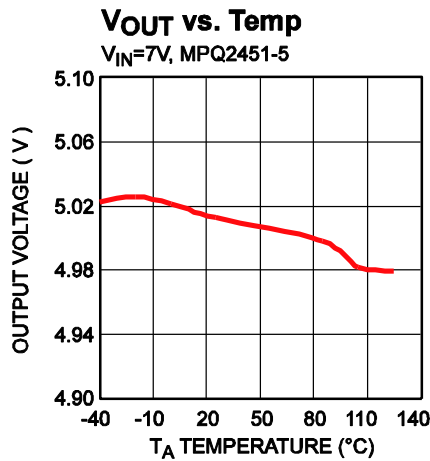
### Notes:

5) Derived from bench characterization, not tested in production.

## PIN FUNCTIONS

SOT23-6L Pin #	QFN-6L Pin #	Name	Description
1	6	BST	Bootstrap. Positive power supply for the internal, floating, high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.
2	5	GND	Ground. Connect the output capacitor as close to this pin as possible. Avoid routing near high-current switch paths.
3	4	OUT	Output-Voltage Sense. Connected to the tap of an internal resistor divider to set the output voltage.
4	3	EN	Enable. Pull this pin below the specified threshold to shut the chip down. Pull it above the specified threshold to enable the chip. Float this pin to disable the chip.
5	2	VIN	Input Supply. Supplies power to all internal control circuitry. Requires a decoupling capacitor to ground to reduce switching spikes.
6	1	SW	Switch Node. Output of the high-side switch. Requires a low- $V_F$ Schottky diode connected to ground to reduce switching spikes.

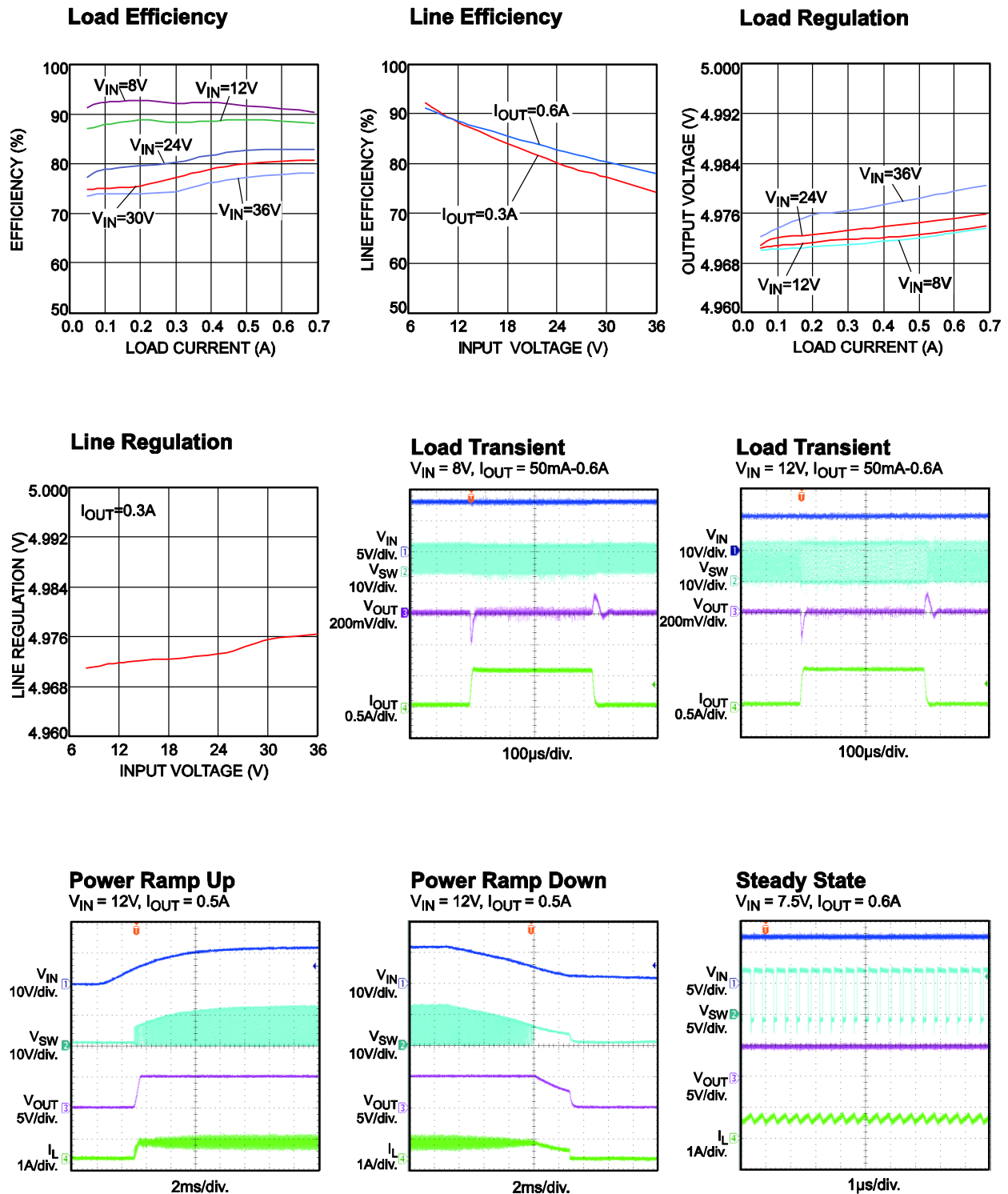
## TYPICAL CHARACTERISTICS



## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $C1 = 10\mu F$ ,  $C2 = 22\mu F$ ,  $L = 3.3\mu H$  and  $T_A = 25^\circ C$ , unless otherwise noted.

MPQ2451-5



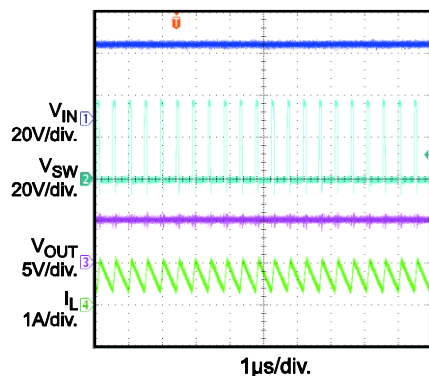
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $C_1 = 10\mu F$ ,  $C_2 = 22\mu F$ ,  $L = 3.3\mu H$  and  $T_A = 25^\circ C$ , unless otherwise noted.

### MPQ2451-5

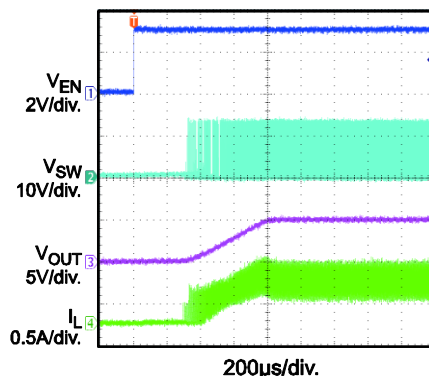
#### Steady State

$V_{IN} = 36V$ ,  $I_{OUT} = 0.6A$



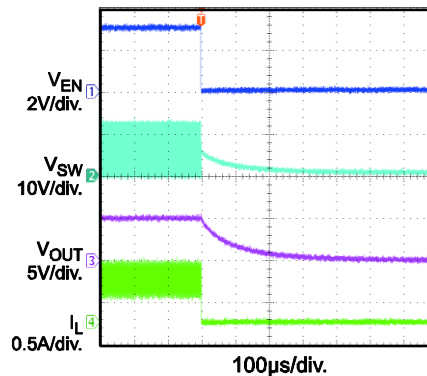
#### Enable On

$V_{IN} = 12V$ ,  $I_{OUT} = 0.5A$



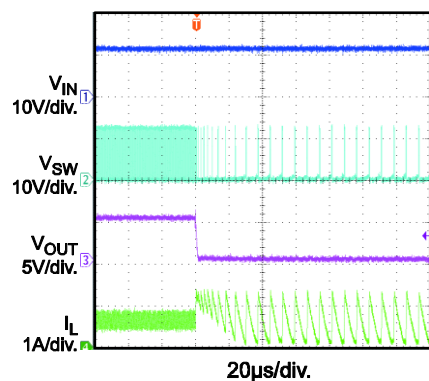
#### Enable Off

$V_{IN} = 12V$ ,  $I_{OUT} = 0.5A$



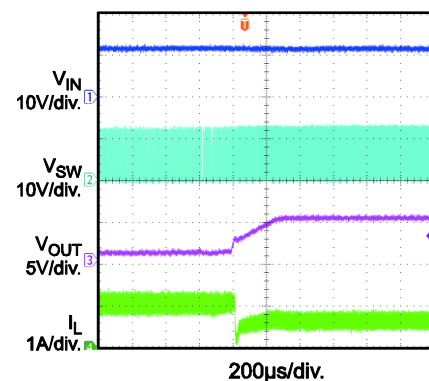
#### Short Output

$V_{IN} = 12V$ ,  $I_{OUT} = 0.5A$



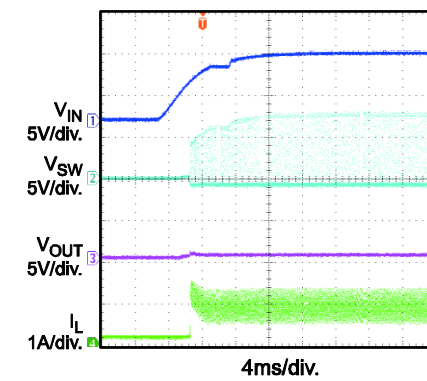
#### Short Output Recovery

$V_{IN} = 12V$ ,  $I_{OUT} = 0.5A$



#### Short Output Start Up

$V_{IN} = 8V$ ,  $I_{OUT} = 0.5A$



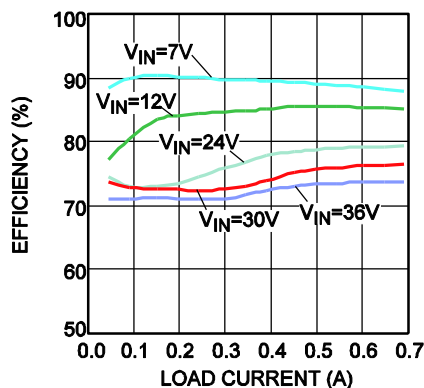


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

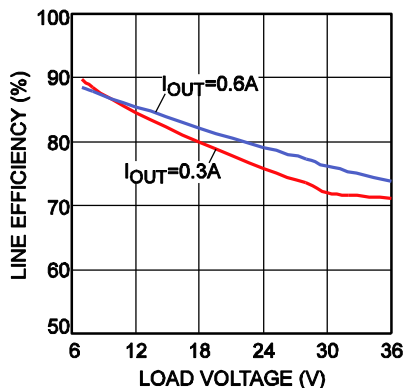
$V_{IN} = 12V$ ,  $C1 = 10\mu F$ ,  $C2 = 22\mu F$ ,  $L = 3.3\mu H$  and  $T_A = 25^\circ C$ , unless otherwise noted.

MPQ2451-33

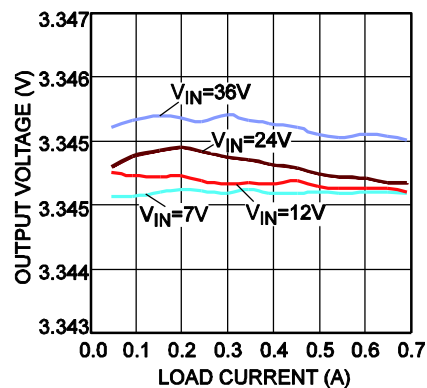
**Load Efficiency**



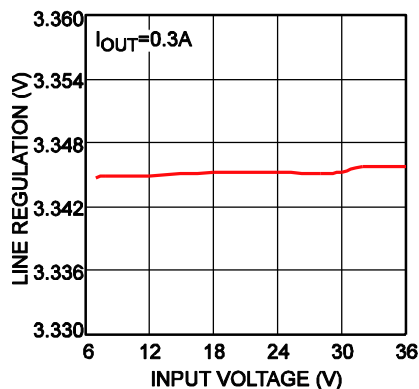
**Line Efficiency**



**Load Regulation**

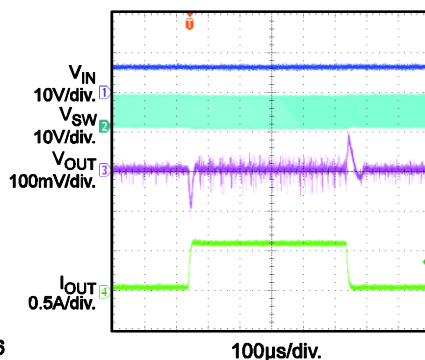


**Line Regulation**



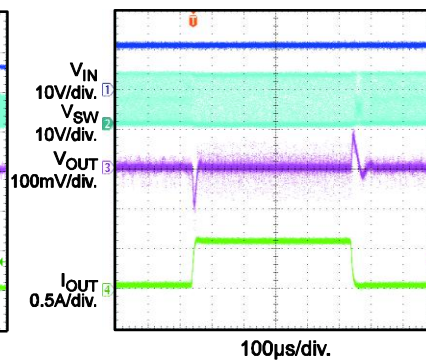
**Load Transient**

$V_{IN} = 7V$ ,  $I_{OUT} = 50mA-0.6A$



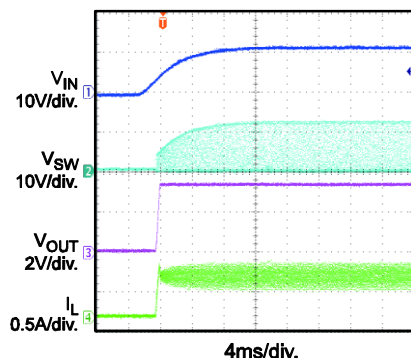
**Load Transient**

$V_{IN} = 12V$ ,  $I_{OUT} = 50mA-0.6A$



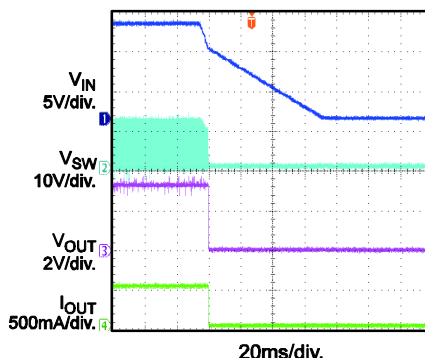
**Power Ramp Up**

$V_{IN} = 12V$ ,  $I_{OUT} = 0.5A$



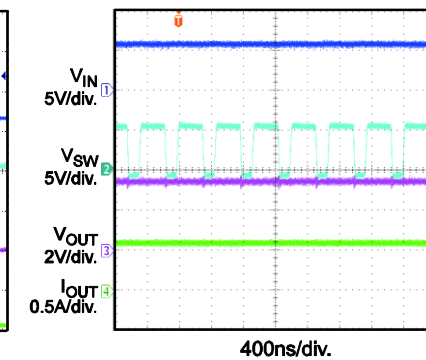
**Power Ramp Down**

$V_{IN} = 12V$ ,  $I_{OUT} = 0.5A$



**Steady State**

$V_{IN} = 5.7V$ ,  $I_{OUT} = 0.6A$





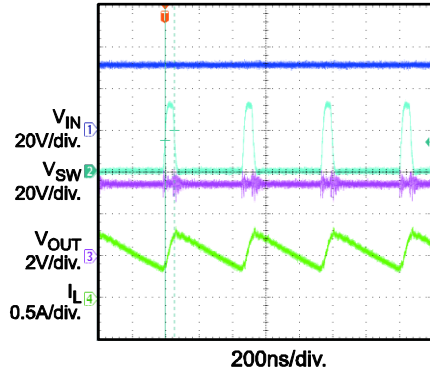
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $C1 = 10\mu F$ ,  $C2 = 22\mu F$ ,  $L = 3.3\mu H$  and  $T_A = 25^\circ C$ , unless otherwise noted.

MPQ2451-33

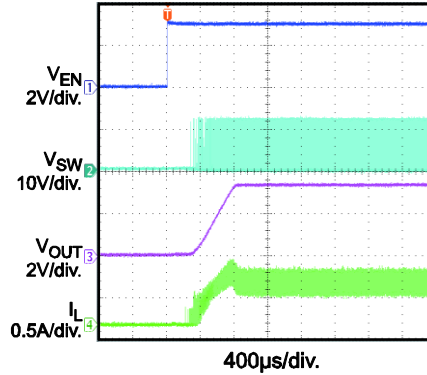
### Steady State

$V_{IN} = 32V$ ,  $I_{OUT} = 0.6A$



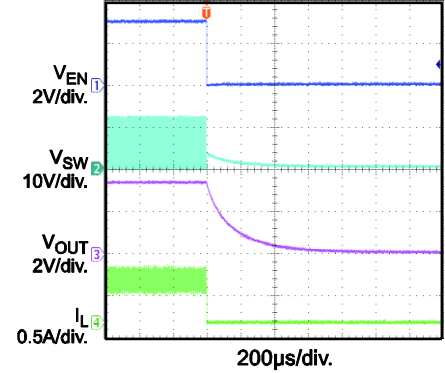
### Enable On

$V_{IN} = 12V$ ,  $I_{OUT} = 0.5A$



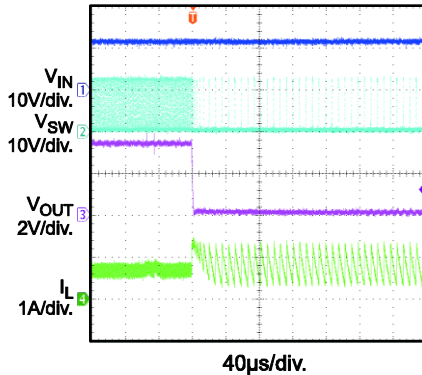
### Enable Off

$V_{IN} = 12V$ ,  $I_{OUT} = 0.5A$



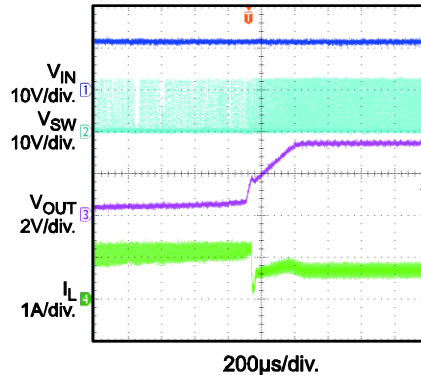
### Short Output

$V_{IN} = 12V$ ,  $I_{OUT} = 0.5A$



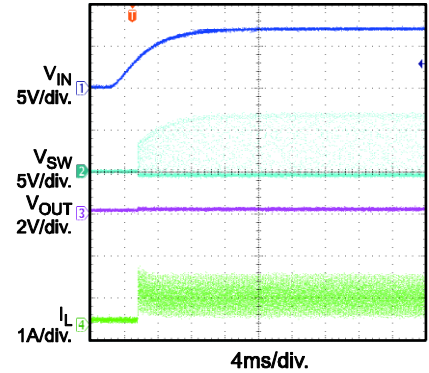
### Short Output Recovery

$V_{IN} = 12V$ ,  $I_{OUT} = 0.5A$



### Short Output Start Up

$V_{IN} = 7V$ ,  $I_{OUT} = 0.5A$



## FUNCTIONAL BLOCK DIAGRAM

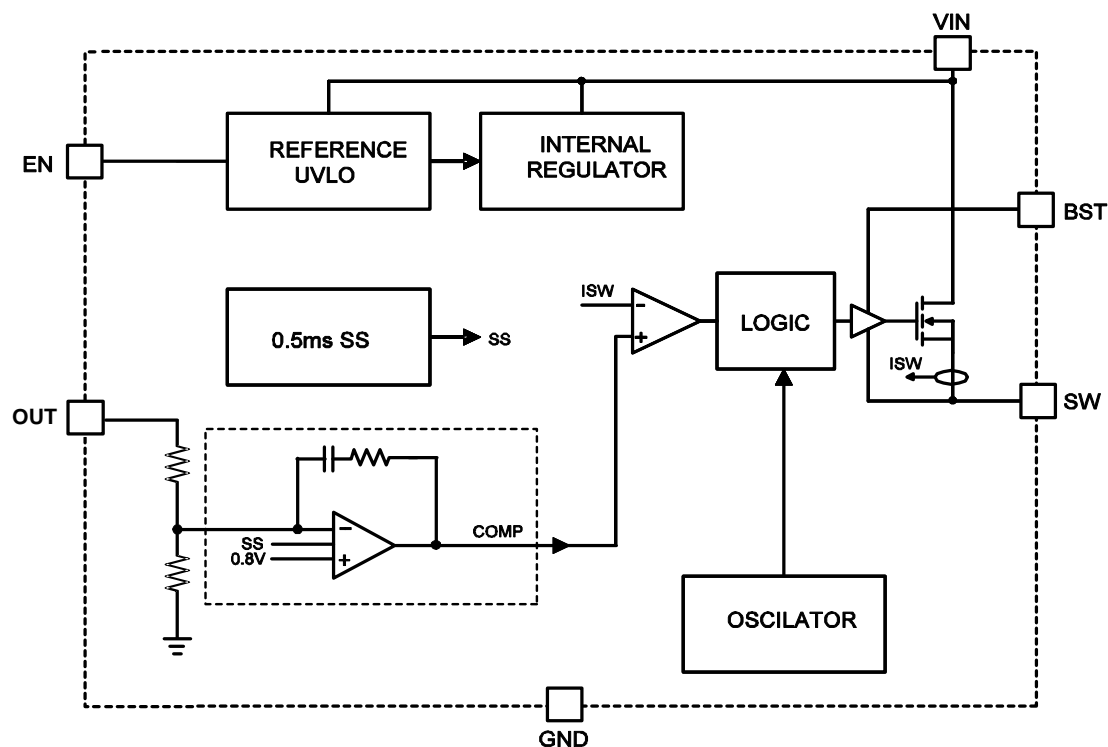


Figure 1: Functional Block Diagram

## OPERATION

The MPQ2451-5/33 is a 2.2MHz, asynchronous, step-down, switching regulator with an integrated high-side, high-voltage, power MOSFET. It provides an internally-compensated, highly-efficient output of up to 0.6A with current-mode control. It also features a wide input voltage range, internal soft-start control, and a precise current limit. Its very-low, operational, quiescent current makes it suitable for battery-powered applications.

### PWM Control

At moderate-to-high output current, the MPQ2451-5/33 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. A PWM cycle—initiated by the internal clock—turns the power MOSFET on, and the MOSFET remains on until its current reaches the value set by  $V_{COMP}$ . When the PWM signal goes low, the power switch turns off and remains off for at least 100ns before the next cycle starts.

If the current in the power MOSFET does not reach the COMP-set current value within one PWM cycle, the power MOSFET remains ON to avoid a turn-off operation.

### Pulse-Skipping Mode

Under light-load conditions, the MPQ2451-5/33 enters pulse-skipping mode to improve efficiency. Pulse-skipping occurs when  $V_{COMP}$  drops below the internal sleep threshold, which generates a PAUSE command to block the turn-on clock pulse so the power MOSFET does not turn ON; this procedure reduces gate driving and switching losses. This PAUSE command causes the whole chip to enter sleep mode, reducing the quiescent current to further improve light-load efficiency.

When  $V_{COMP}$  exceeds the sleep threshold, the PAUSE signal resets and the chip resumes normal PWM operation. Whenever the PAUSE changes state from LOW to HIGH, the PWM signal immediately goes HIGH and turns on the power MOSFET.

### Error Amplifier

The error amplifier is composed of an internal op-amp with an RC feedback network connected between its output node (COMP) and its negative input node (FB). When  $V_{FB}$  drops below the internal reference voltage ( $V_{REF}$ ), the op-amp

drives the COMP output high, driving the switch peak current to rise and deliver more energy to the output. Conversely, when  $V_{FB}$  rises above  $V_{REF}$ , the switch peak current output drops.

### Internal Regulator

The 2.6V internal regulator powers most of the internal circuitry. This regulator takes the  $V_{IN}$  input and operates in the full  $V_{IN}$  range. When  $V_{IN}$  exceeds 3.0V, the output of the regulator is in full regulation. When  $V_{IN}$  drops below 3.0V, the output degrades.

### Enable Control

The MPQ2451-5/33 has a dedicated enable control pin, EN. When  $V_{IN}$  rises above threshold, the EN pin can enable or disable the chip for HIGH effective logic. Its falling threshold is 1.2V, and its rising threshold is about 1.6V. When left floating, the EN pin is internally pulled down to GND to disable the chip.

When the EN voltage is pulled to 0V, the chip enters the lowest shutdown current mode. Between 0V and the rising threshold, the chip remains in shutdown mode with a slightly higher shutdown current.

### Under-Voltage Lockout (UVLO)

$V_{IN}$  under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO rising threshold is ~2.9V while its falling threshold is 2.6V.

### Internal Soft-Start

A reference-type soft-start (SS) prevents the converter-output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage ( $V_{SS}$ ) that ramps up from 0V over the SS time. When  $V_{SS}$  is less than  $V_{REF}$ ,  $V_{SS}$  overrides  $V_{REF}$  as the error amplifier reference.

The maximum  $V_{SS}$  is approximately the same as  $V_{FB}$ ; i.e. if  $V_{FB}$  falls, the maximum of  $V_{SS}$  falls. This accommodates short-circuit recovery; when the short-circuit is removed,  $V_{SS}$  ramps up to prevent output-voltage overshoot.

### Thermal Shutdown

Thermal shutdown prevents thermal runaway. When the silicon die temperature exceeds its upper threshold, the entire chip shuts down. When the temperature drops below its lower threshold, the chip is enabled again.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating-power-MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of about 2.4V and a falling threshold of about 300mV. During this UVLO,  $V_{SS}$  resets to 0V. When the UVLO is removed, the controller enters soft-start.

The dedicated internal-bootstrap regulator charges and regulates the bootstrap capacitor to about 5V. When the voltage between the BST and SW nodes falls below its regulation, a PMOS pass transistor connected from  $V_{IN}$  to BST turns on. The charging current path goes from  $V_{IN} \rightarrow \text{BST} \rightarrow \text{SW}$ . The external circuit must provide enough voltage headroom to facilitate charging.

If  $V_{IN}$  is sufficiently higher than  $V_{SW}$ , the bootstrap capacitor will charge. When the power MOSFET is ON,  $V_{IN}=V_{SW}$  so the bootstrap capacitor does not charge. Optimal charging occurs when  $V_{IN}-V_{SW}$  reaches its apex when the external freewheeling diode is on. When there is no current in the inductor,  $V_{SW}=V_{OUT}$  so  $V_{IN}-V_{OUT}$  can charge the bootstrap capacitor.

At a higher duty cycle, the bootstrap capacitor may not be charged sufficiently because of a shorter charging period. If there is insufficient voltage and time to charge the bootstrap capacitor, add an extra external circuit to ensure the bootstrap voltage in normal operation region.

The floating driver's UVLO is not communicated to the controller.

Make sure the bleed-through current at the SW node is at least higher than the floating driver's DC quiescent current of about 20 $\mu$ A.

### Current Comparator and Current Limit

A current-sense MOSFET senses the power MOSFET current. This value is the input to the high-speed-current comparator for current-mode control. When the power MOSFET turns on, the comparator is first blanked to limit noise, and then compares the power switch current to the

$V_{COMP}$ . When the sensed value exceeds  $V_{COMP}$ , the comparator output goes LOW to turn off the power MOSFET. The maximum current of the internal power MOSFET is internally limited cycle-by-cycle.

### Startup and Shutdown

If both  $V_{IN}$  and  $V_{EN}$  exceed their respective thresholds, the chip starts. The reference block starts first to generate a stable reference voltage and current, and then the internal regulator operates to provide a stable supply for the rest circuit.

While the internal supply rail is up, an internal timer turns the power MOSFET off for about 50 $\mu$ s to blank startup noise. When the internal soft-start block is enabled, it first holds its SS output low to ensure the rest of the circuit is ready before ramping up.

Three events shut down the chip: EN low,  $V_{IN}$  low, thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggering.  $V_{COMP}$  and the internal supply rail are then pulled low. The floating driver is not subject to this shutdown command but its charging path is disabled.

## APPLICATION INFORMATION

### COMPONENT SELECTION

#### Inductor

The inductor supplies constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current and lower output ripple voltage. However, the larger-value inductor is typically physically larger, has a higher series resistance, or has a lower saturation current.

To determine the inductance, allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. Also, choose a peak inductor current below the maximum switch current limit. The inductance value can be calculated by:

$$L1 = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Where  $V_{OUT}$  is the output voltage,  $V_{IN}$  is the input voltage,  $f_S$  is the switching frequency, and  $\Delta I_L$  is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L1} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Where  $I_{LOAD}$  is the load current.

Table 2 lists a number of suitable inductors from various manufacturers. The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI requirement.

**Table 1: Inductor Selection Guide**

Part Number	Inductance (μH)	Max DCR (Ω)	Current Rating (A)	Dimensions L × W × H (mm <sup>3</sup> )
<b>Würth Electronics</b>				
7440430022	2.2	0.028	2.5	4.8×4.8×2.8
744043003	3.3	0.035	2.15	4.8×4.8×2.8
7447785004	4.7	0.078	2.4	5.9×6.2×3.2
<b>TOKO</b>				
D63CB-#A916CY-2R0M	2.0	0.019	2.36	6.2×6.3×3.0
D62CB-#A916CY-3R3M	3.3	0.026	2.17	6.2×6.3×3.0
D62CB-#A916CY-4R7M	4.7	0.032	2.1	6.2×6.3×3.0
<b>TDK</b>				
LTF5022T-2R2N3R2	2.2	0.04	3.2	5.2×5.0×2.2
LTF5022T-3R3N2R5	3.3	0.06	2.5	5.2×5.0×2.2
LTF5022T-4R7N2R0	4.7	0.081	2.0	5.2×5.0×2.2
<b>COOPER BUSSMANN</b>				
SD25-2R2	2.2	0.031	2.8	5.2×5.2×2.5
SD25-3R3	3.3	0.038	2.21	5.2×5.2×2.5
SD25-4R7	4.7	0.047	1.83	5.2×5.2×2.5

The input capacitor (C1) can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high quality ceramic capacitor—for example, 0.1μF—as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

### Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right)$$

Where L is the inductor value and R<sub>ESR</sub> is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

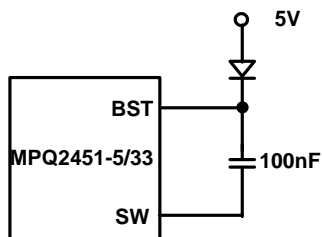
The characteristics of the output capacitor also affect the stability of the regulation system.



### External Bootstrap Diode

An external bootstrap diode from 5V to the BST pin may enhance the efficiency of the regulator if there is a 5V rail available to the system,  $V_{IN} \leq 6V$ , or for high-duty-cycle ( $V_{OUT}/V_{IN} > 65\%$ ) applications.

A low-cost bootstrap diode, such as IN4148 or BAT54, is suitable for such applications.



**Figure 2: External Bootstrap Diode**

At no load or light load, the converter may operate in pulse-skipping mode in order to regulate the output voltage and leave less time to refresh the BST voltage. To ensure sufficient gate voltage, select  $(V_{IN} - V_{OUT}) > 3V$ . To meet this requirement, the EN pin can be used to program the input UVLO voltage to  $V_{OUT}+3V$ .

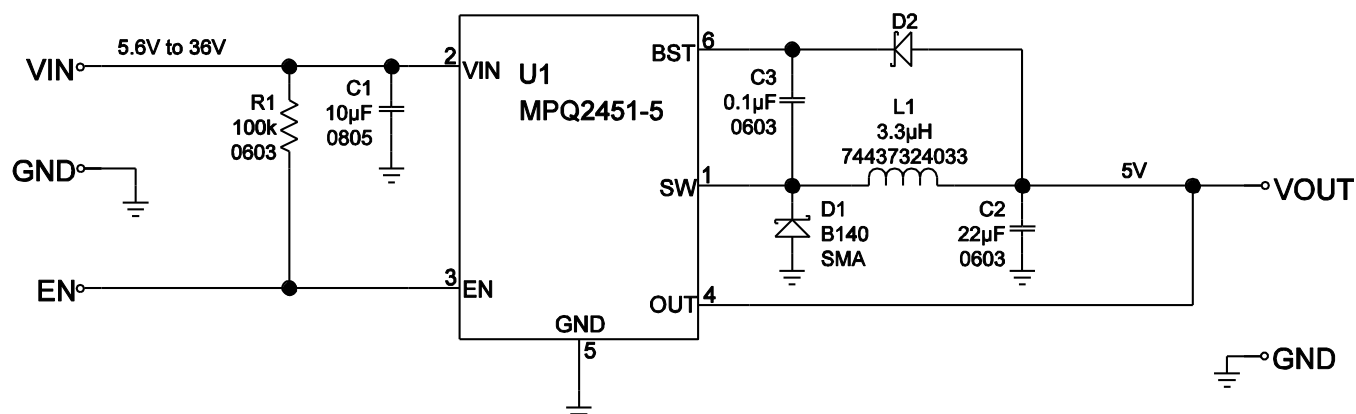
### PCB Layout

PCB layout requires high-frequency noise considerations to limit voltage spikes on the SW node and to limit EMI noise. Keep the path of the input decoupling capacitor, catch diode, the  $V_{IN}$  pin, SW pin, and PGND as short as possible using short and wide traces, with the passive components as close to the device as possible.

Run the feedback trace far from the inductor and noisy power traces: if possible, run the feedback trace on the opposite side of the PCB from the inductor, separated by a ground plane. Expect greater switching losses at high switching frequencies.

Add a grid of thermal vias under the exposed pad to improve thermal conductivity. Use small vias (15mil barrel diameter) so that the hole fills during the plating process, and to avoid solder wicking during the reflow process associated with larger vias. Use a pitch (distance between the centers) of approximately 40mil between the thermal vias. Please refer to the layout example on EVQ2451-G-33 datasheet.

## TYPICAL APPLICATION CIRCUITS (QFN-6L)



**Figure 3: 5V Output Typical Application Schematic**



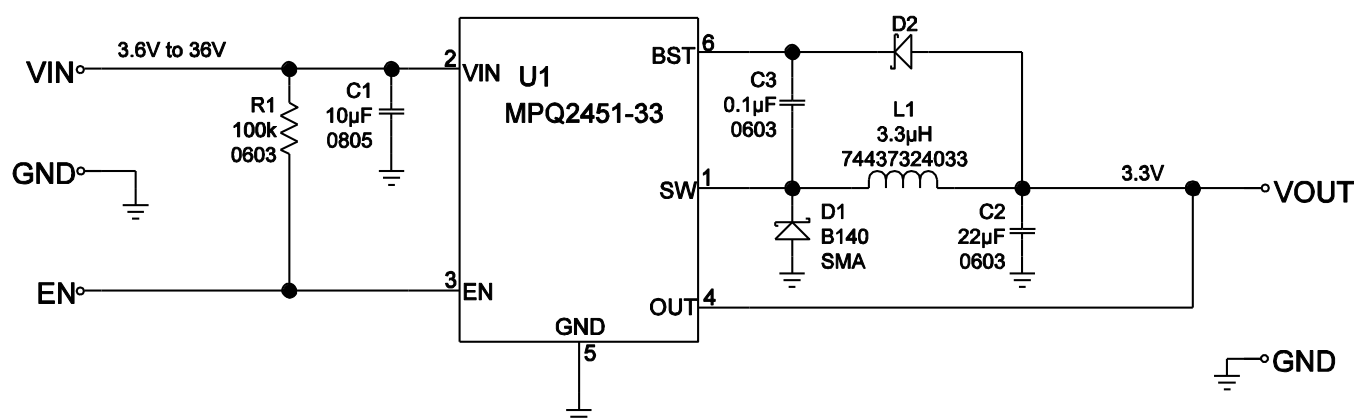
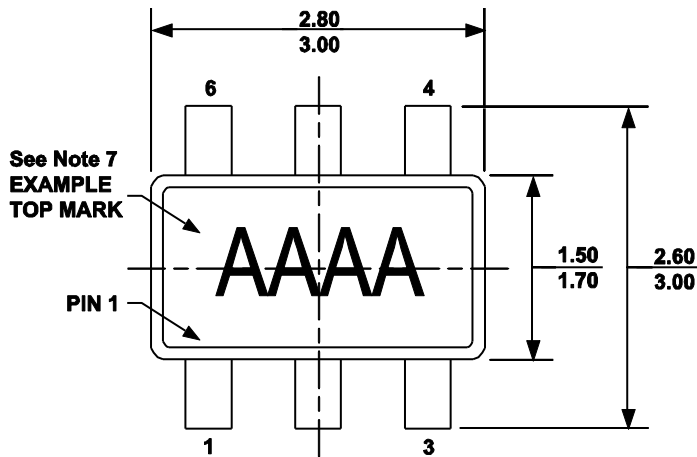


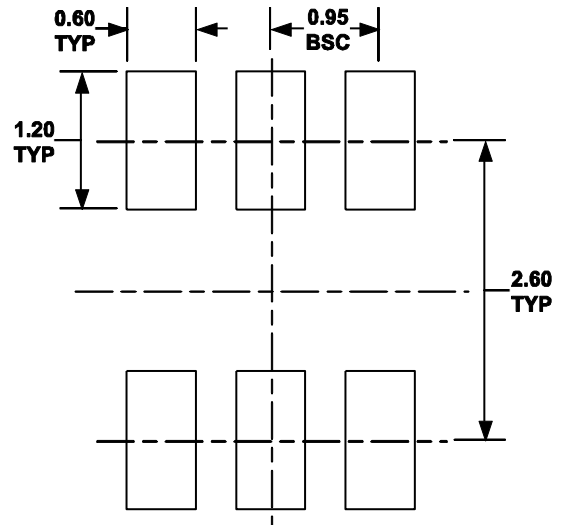
Figure 4: 3.3V Output Typical Application Schematic

## PACKAGE INFORMATION

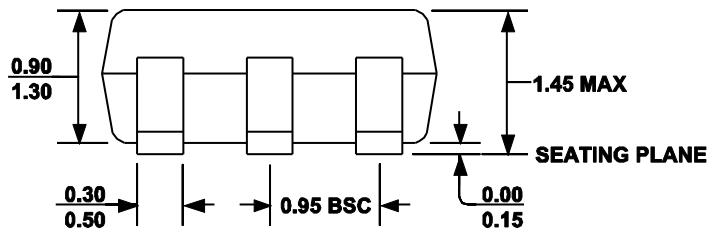
### SOT23-6L



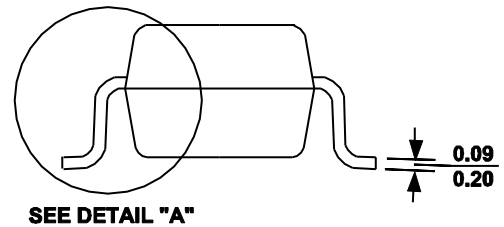
**TOP VIEW**



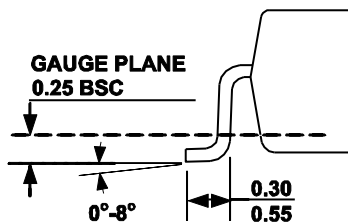
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**

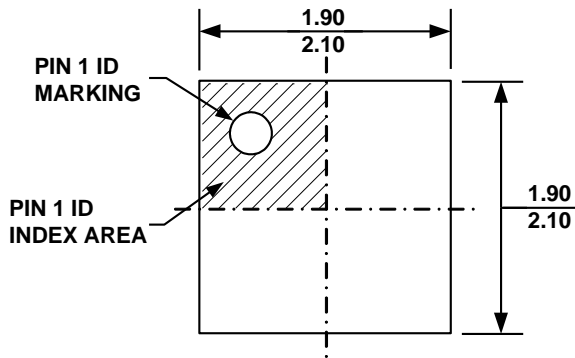


**DETAIL "A"**

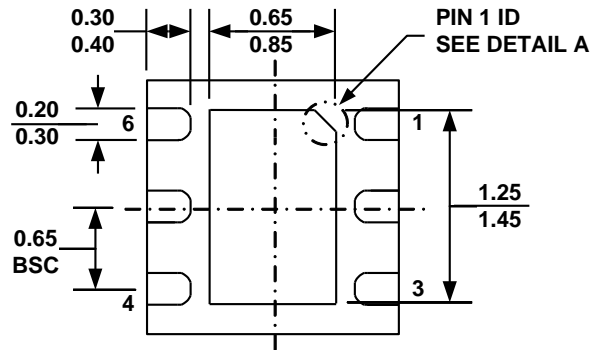
#### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
- 6) DRAWING IS NOT TO SCALE.
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

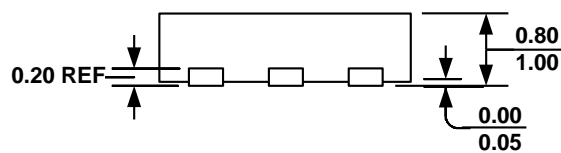
**QFN6 (2mmx2mm)**



**TOP VIEW**

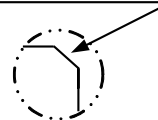


**BOTTOM VIEW**

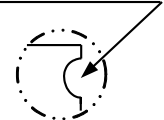


**SIDE VIEW**

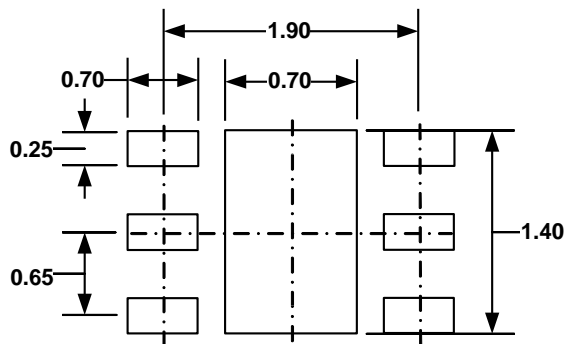
**PIN 1 ID OPTION A**  
0.30x45° TYP.



**PIN 1 ID OPTION B**  
R0.20 TYP.



**DETAIL A**



**RECOMMENDED LAND PATTERN**

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