MD1715

2-Channel 5-Level High-Speed Ultrasound Driver IC

Features

- Advanced CMOS Technology
- ±4.75 to 12.9V Gate Drive Voltage
- 2A Output Source and Sink Current
- 6.5 ns Rise and Fall Time with 1 nF Load
- 10 ns Propagation Delay
- ±2 ns Matched Delay Times
- 12 Matched Channels
- 1.8V to 3.3V CMOS Logic Interface
- Smart Logic Threshold
- Low-inductance Package

Applications

- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Metal Flaw Detection
- Non-destructive Testing (NDT)

General Description

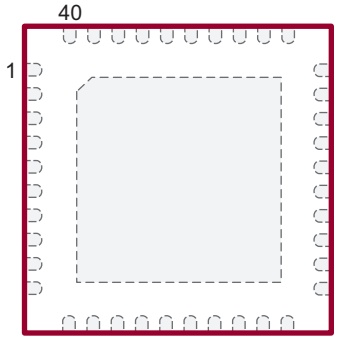
The MD1715, paired with Microchip's TC8020, forms a 2-channel five-level high-voltage high-speed transmit pulser chip set. The chip set is designed for medical ultrasound imaging applications but can also be used for metal flaw detection, NDT and piezoelectric transducer drivers.

The MD1715 is a 2-channel logic controller circuit with 12 low-impedance MOSFET gate drivers. There are two sets of control logic inputs—one for Channel A and one for Channel B. Each channel consists of three pairs of MOSFET gate drivers. These drivers are designed to match the drive requirements of Microchip's TC8020.

The TC8020 is the output stage of the pulser, with six pairs of MOSFETs. Each pair consists of a P-channel and an N-channel MOSFET. They are designed to have the same impedance and can provide typical peak currents of ±3.5A at 200V.

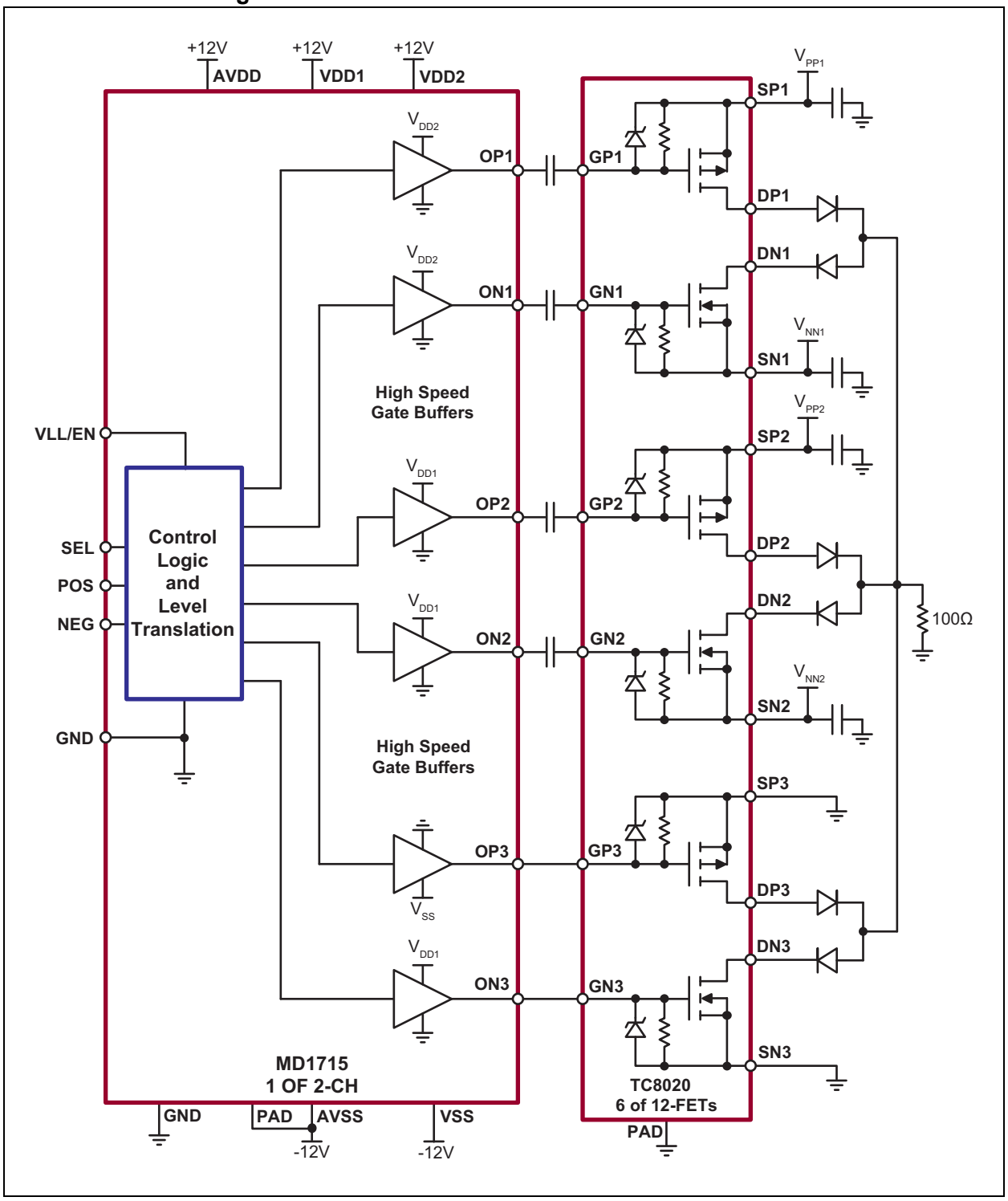
Package Type

40-lead QFN
(Top view)

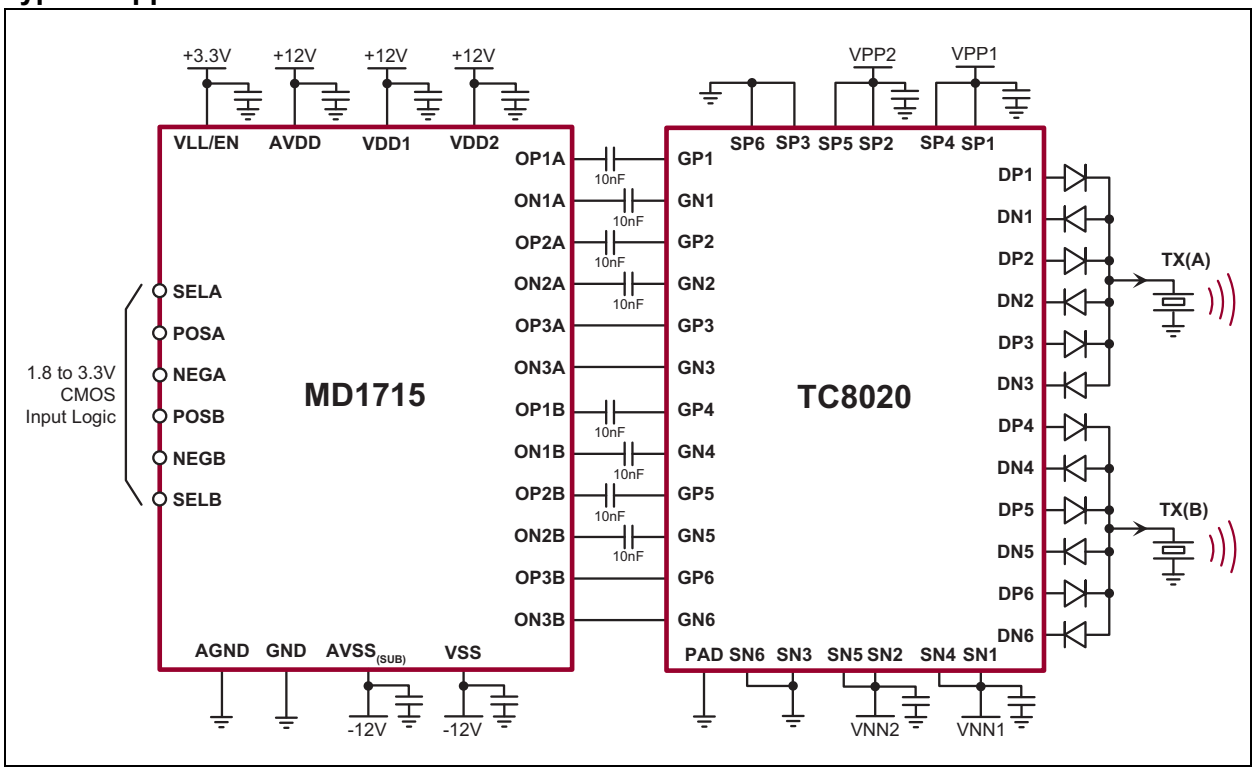


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

GND and AGND, Ground 0V
Logic Input Pin, V_{LL} ..... –0.5V to +5.5V
Positive Gate Drive Supply, AV_{DD}, $V_{DD}1$, $V_{DD}2$ ..... –0.5V to +14.5V
Negative Gate Drive Supply, AV_{SS}, V_{SS} ..... –14.5V to +0.5V
Operating Junction Temperature, T_J ..... 0°C to +125°C
Storage Temperature, T_S ..... –65°C to +150°C
Power Dissipation:
40-lead QFN (**Note 1**) 1.3W

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: 1 oz. four-layer 3 inches x 4 inches PCB

OPERATING SUPPLY VOLTAGES AND CURRENTS

Electrical Specifications for Operating Supply Currents: Over operating conditions unless otherwise specified, V_{LL} = 3.3V, AV_{DD} = V_{DD1} = V_{DD2} = +12V, AV_{SS} = V_{SS} = –12V, T_A = 25°C

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply	V_{LL}	1.8	3.3	3.6	V	
Positive Analog Supply	AV_{DD}	8	—	12.9	V	AV_{DD} ≥ ($V_{DD}1$ or $V_{DD}2$)
Positive Gate Drive Supply	$V_{DD}2$, $V_{DD}1$	4.75	—	12.9	V	
Negative Gate Drive Supply	AV_{SS}, V_{SS}	–12.9	—	–4.75	V	
Logic Reference Current	I_{VLL}	—	10	—	µA	V_{LL} = 3.3V
AV_{DD} Power-down Current	I_{AVDDQ}	—	0.4	—	mA	EN = 0, all inputs low
V_{SS} Power-down Current	I_{VSSQ}	—	0.1	—	mA	
V_{DD1} Power-down Current	I_{VDD1Q}	—	10	25	µA	EN = 0, all inputs low
V_{DD2} Power-down Current	I_{VDD2Q}	—	10	25	µA	
AV_{DD} Power-up Current	I_{AVDDEN}	—	2	3	mA	EN = 1, all inputs low
V_{SS} Power-up Current	I_{VSSEN}	—	0.7	1	mA	
$V_{DD}1$ Power-up Current	I_{VDD1EN}	—	10	—	µA	EN = 1, all inputs low
$V_{DD}2$ Power-up Current	I_{VDD2EN}	—	10	—	µA	
AV_{DD} CW 5 MHz Current	I_{AVDDCW}	—	10	—	mA	A and B Channels on at 5 MHz, no load, $V_{DD}1$ = 12V, $V_{DD}2$ = 5V
V_{SS} CW 5 MHz Current	I_{VSSCW}	—	5	—	mA	
$V_{DD}1$ CW 5 MHz Current	I_{VDD1CW}	—	25	—	mA	A and B Channels on at 5 MHz, no load, $V_{DD}1$ = 5V, $V_{DD}2$ = 12V
$V_{DD}2$ CW 5 MHz Current	I_{VDD2CW}	—	25	—	mA	A and B Channels on at 5 MHz, no load, $V_{DD}1$ = 12V, $V_{DD}2$ = 5V

DC ELECTRICAL CHARACTERISTICS

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
P-CHANNEL AND N-CHANNEL GATE DRIVER OUTPUTS							
Output Sink Resistance	P-Channel	R_{SINK}	—	5	6	Ω	I_{SINK} = 100 mA
	N-Channel		—	5	6	Ω	I_{SINK} = 100 mA
Output Source Resistance	P-Channel	R_{SOURCE}	—	5	6	Ω	I_{SOURCE} = 100 mA
	N-Channel		—	5	6	Ω	I_{SOURCE} = 100 mA
Peak Output Sink Current	P-Channel	I_{SINK}	1.7	2	—	A	
	N-Channel		1.7	2	—	A	
Peak Output Source Current	P-Channel	I_{SOURCE}	1.7	2	—	A	
	N-Channel		1.7	2	—	A	
LOGIC INPUTS							
Chip Disable Low Voltage		V_{ENL}	0	—	0.3	V	VLL/EN is a dual function pin
Input Logic High Voltage		V_{IH}	0.8 V_{LL}	—	V_{LL}	V	
Input Logic Low Voltage		V_{IL}	0	—	0.2 V_{LL}	V	
Input Logic High Current		I_{IH}	—	—	1	µA	
Input Logic Low Current		I_{IL}	–1	—	—	µA	

AC ELECTRICAL CHARACTERISTICS

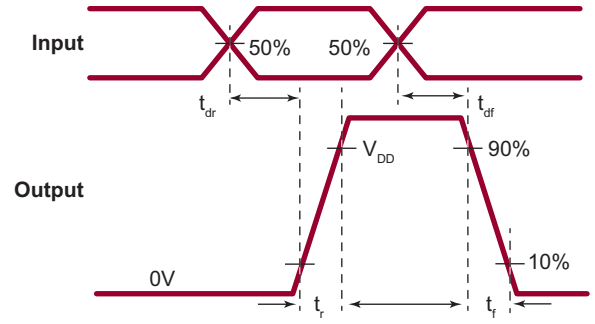
Electrical Specifications: Over operating conditions unless otherwise specified, V_{LL} = 3.3V, $AV_{DD} = V_{DD}1 = V_{DD}2$ = +12V, $AV_{SS} = V_{SS}$ = –12V, T_A = 25°C

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input Rise and Fall Time	t_{irf}	—	—	10	ns	Logic input edge speed requirement
Output Rise Time	t_r	—	6.5	—	ns	1 nF load, input signal rise/fall time 2 ns (**Timing Waveforms**)
Output Fall Time	t_f	—	6.5	—	ns	
Output Rise Delay	t_{dr}	—	10	—	ns	
Output Fall Delay	t_{df}	—	10	—	ns	
Rise and Fall Time Matching	$\lvert t_r – t_f \rvert$	—	1	—	—	For each channel
Propagation Delay Matching	$\lvert t_{dr} – t_{df} \rvert$	—	1	—	—	
Delay Time Matching	t_{dm}	—	±2	—	ns	Channel to channel and device to device
Output Jitter	Δt_j	—	20	—	ps	V_{DD} = 10V
IC Enable Time	t_{EN_ON}	—	25	50	µs	
IC Disable Time	t_{EN_OFF}	—	0.5	2	µs	
Second Harmonic Distortion	HD2	–40	—	—	dB	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	–0	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
40-lead QFN	θ_{JA}	—	24	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of MD1715 are listed on Table 2-1. See **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	SELA	SEL input logic control for Channel A. See Table 3-1.
2	POSA	POS input logic control for Channel A. See Table 3-1.
3	NEGA	NEG input logic control for Channel A. See Table 3-1.
4	VLL/EN	Logic High reference voltage and chip enable input
5	AVDD	Positive supply voltage of analog circuitry. AVDD should be at the same or higher potential than the highest voltages of VDD1 or VDD2.
6	AGND	Digital ground
7	AVSS	Negative supply voltage of analog circuitry and connection of IC substrate. Should be at the same potential as VSS.
8	SELB	SEL input logic control for Channel B. See Table 3-2.
9	POSB	POS input logic control for Channel B. See Table 3-2.
10	NEGB	NEG input logic control for Channel B. See Table 3-2.
11	VDD2	Positive supply voltage of the gate drivers for the output stages OP1 and ON1 in Channel A and Channel B. VDD2 can be at a different voltage than VDD1.
12	OP1B	First output P-channel gate driver for Channel B
13	VDD1	Positive supply voltage of the gate drivers for the output stages OP2, ON2 and ON3 in Channel A and Channel B. VDD1 can be at a different voltage than VDD2.
14	GND	Power ground
15	OP2B	Second output P-channel gate driver for Channel B
16	VDD2	Positive supply voltage of the gate drivers for the output stages OP1 and ON1 in Channel A and Channel B. VDD2 can be at a different voltage than VDD1.
17	ON1B	First output N-channel gate driver for Channel B
18	GND	Power ground
19	VDD1	Positive supply voltage of the gate drivers for the output stages OP2, ON2 and ON3 in Channel A and Channel B. VDD1 can be at a different voltage than VDD2.
20	ON2B	Second output N-channel gate driver for Channel B
21	GND	Power ground
22	ON3B	Damping output N-channel gate driver for Channel B
23	VSS	Negative supply voltage for the gate drive of OP3. Should be the same voltage as AVSS.
24	OP3B	Damping output P-channel gate driver for Channel B
25	GND	Power ground
26	VSS	Negative supply voltage for gate drive of OP3. Should be the same voltage as AVSS.
27	OP3A	Damping output P-channel gate driver for Channel A
28	GND	Power ground

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
29	GND	Power ground
30	ON3A	Damping output N-channel gate driver for Channel A
31	ON2A	Second output N-channel gate driver for Channel A
32	VDD1	Positive supply voltage of the gate drivers for the output stages OP2, ON2 and ON3 in Channel A and Channel B. VDD1 can be at a different voltage than VDD2.
33	GND	Power ground
34	ON1A	First output N-channel gate driver for Channel A
35	VDD2	Positive supply voltage of the gate drivers for the output stages OP1 and ON1 in Channel A and Channel B. VDD2 can be at a different voltage than VDD1.
36	OP2A	Second output P-channel gate driver for Channel A
37	GND	Power ground
38	VDD1	Positive supply voltage of the gate drivers for the output stages OP2, ON2 and ON3 in Channel A and Channel B. VDD1 can be at a different voltage than VDD2.
39	OP1A	First output P-channel gate driver for Channel A
40	VDD2	Positive supply voltage of the gate drivers for the output stages OP1 and ON1 in Channel A and Channel B. VDD2 can be at a different voltage than VDD1.
Center Pad	Thermal Pad	IC substrate, must connect to AVSS externally

3.0 FUNCTIONAL DESCRIPTION

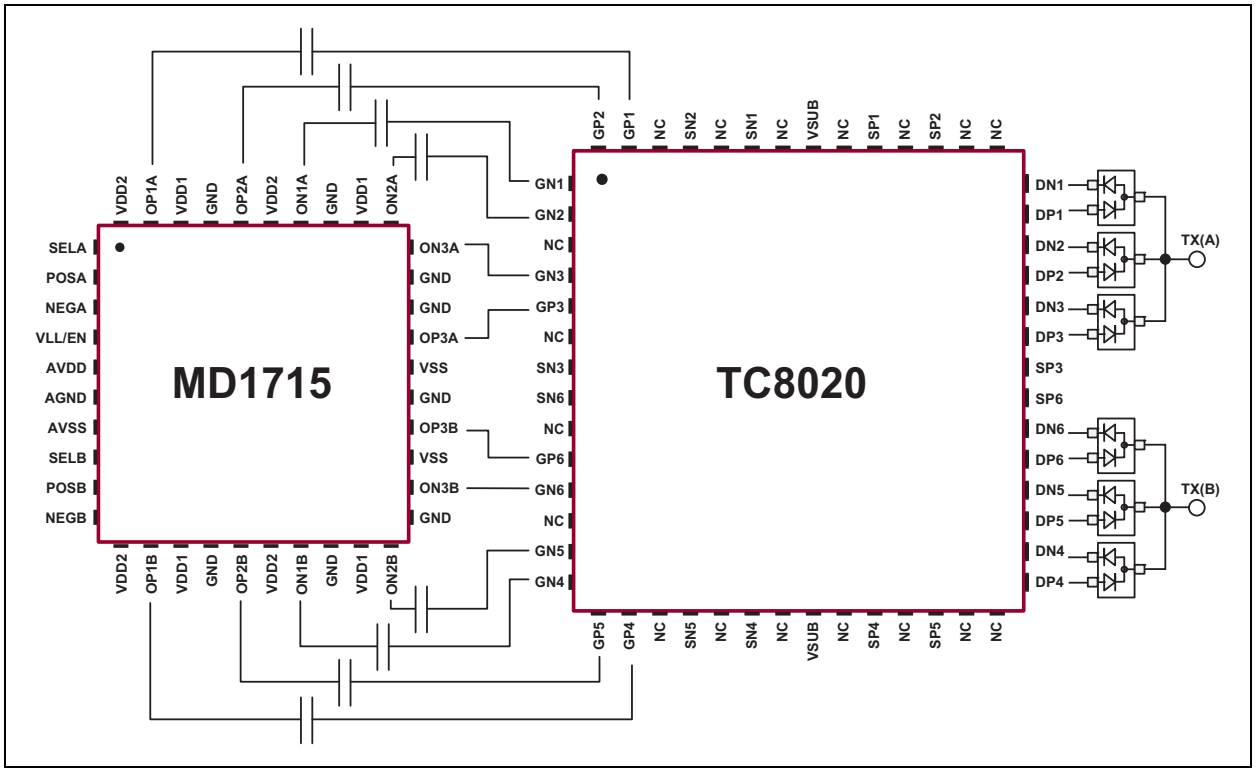


FIGURE 3-1: *Circuit Pin Layout.*

TABLE 3-1: TRUTH FUNCTION TABLE FOR CHANNEL A

EN	Logic Inputs A			SP1 to DP1	SN1 to DN1	SP2 to DP2	SN2 to DN2	SP3 to DP3	SN3 to DN3
	SELA	POSA	NEGA						
1	0	0	0	OFF	OFF	OFF	OFF	**ON**	**ON**
1	0	0	1	OFF	OFF	OFF	**ON**	OFF	OFF
1	0	1	0	OFF	OFF	**ON**	OFF	OFF	OFF
1	0	1	1	OFF	OFF	OFF	OFF	OFF	OFF
1	1	0	0	OFF	OFF	OFF	OFF	**ON**	**ON**
1	1	0	1	OFF	**ON**	OFF	OFF	OFF	OFF
1	1	1	0	**ON**	OFF	OFF	OFF	OFF	OFF
1	1	1	1	OFF	OFF	OFF	OFF	OFF	OFF

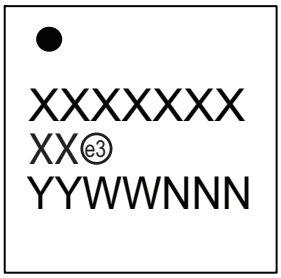
TABLE 3-2: TRUTH FUNCTION TABLE FOR CHANNEL B

EN	Logic Inputs B			SP4 to DP4	SN4 to DN4	SP5 to DP5	SN5 to DN5	SP6 to DP6	SN6 to DN6
	SELB	POSB	NEGB						
1	0	0	0	OFF	OFF	OFF	OFF	**ON**	**ON**
1	0	0	1	OFF	OFF	OFF	**ON**	OFF	OFF
1	0	1	0	OFF	OFF	**ON**	OFF	OFF	OFF
1	0	1	1	OFF	OFF	OFF	OFF	OFF	OFF
1	1	0	0	OFF	OFF	OFF	OFF	**ON**	**ON**
1	1	0	1	OFF	**ON**	OFF	OFF	OFF	OFF
1	1	1	0	**ON**	OFF	OFF	OFF	OFF	OFF
1	1	1	1	OFF	OFF	OFF	OFF	OFF	OFF
0	X	X	X	OFF	OFF	OFF	OFF	**ON**	**ON**
0→1	0	0	0	EN transitions from low to high or high to low should occur at all logic inputs low.					
1→0	0	0	0						

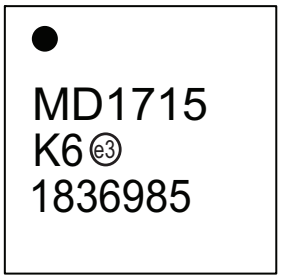
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

40-lead QFN



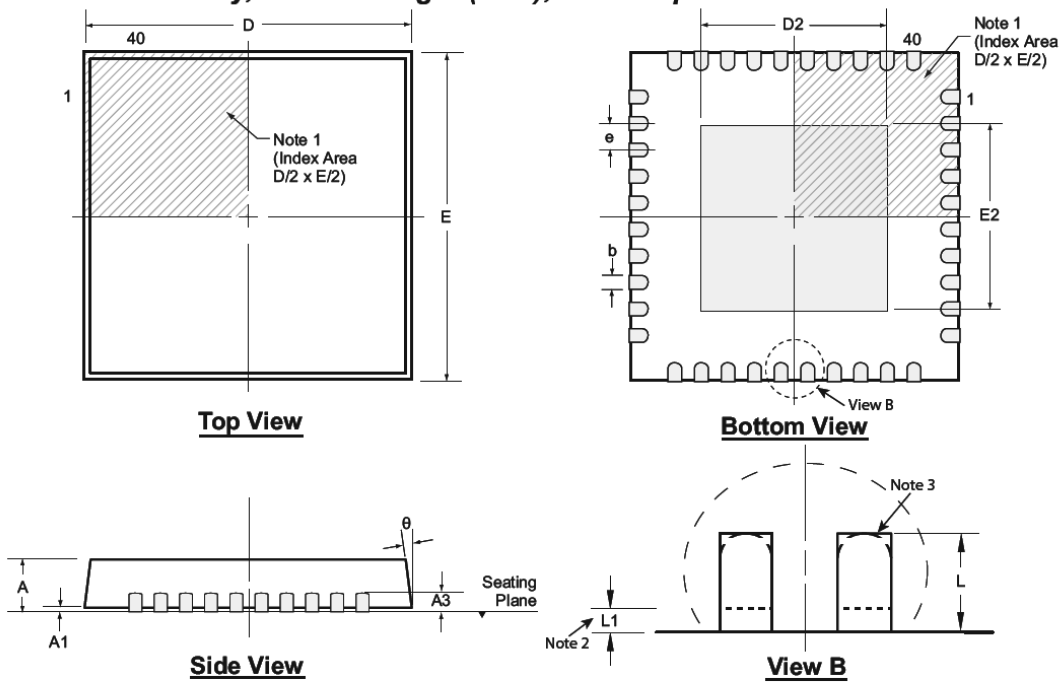
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

40-Lead QFN Package Outline (K6)

6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ°
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	5.85*	1.05	5.85*	1.05	0.50 BSC	0.30†	0.00	0
	NOM	0.90	0.02		0.25	6.00	-	6.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	6.15*	4.45	6.15*	4.45		0.50†	0.15	14

JEDEC Registration MO-220, Variation VJJD-6, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (January 2018)

- Converted Supertex Doc# DSFP-MD1715 to Microchip DS20005921A
- Changed the package marking format
- Changed the quantity of the 40-lead VQFN K6 M935 package from 2000/Reel to 3000/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	MD1715	=	2-Channel 5-Level High-Speed Ultrasound Driver IC
Package:	K6	=	40-lead VQFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	490/Tray for a K6 Package
	M935	=	3000/Reel for a K6 Package

Examples:

a) MD1715K6-G: 2-Channel 5-Level High-Speed Ultrasound Driver IC, 40-lead VQFN, 490/Tray

b) MD1715K6-G-M935: 2-Channel 5-Level High-Speed Ultrasound Driver IC, 40-lead VQFN, 3000/Reel

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KEELOQ, KEELOQ logo, Kleer, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

ISBN: 978-1-5224-2591-5

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820