Table of Contents

Chapter1. Introduction

1.1 General Description

AP3917C is an off-line universal AC Voltage input step-down regulator which provides accurate constant voltage (CV) output, outstanding low standby power, high efficiency@ light loading and excellent dynamic response based on non-isolated buck topology.
The AP3917C EV4 Evaluation Board provides a good design example for a cost-effective 2.1W single output 12V/175mA power application used in home appliances.

1.2 AP3917C Key Features

- Universal 85V to 265V V_{AC} Input
- Internal MOSFET 650V (16Ω)
- Maximum output Current: 270mA typ.@5V output
- Low Standby Power Consumption (<30mW at no load)
- High Light-Loading Efficiency and average efficiency can meet DOE IV and CoC V5 Tier 2
- Frequency Modulation to suppress EMI to meet EN55022 and FCC part 15 class B
- Rich Protection including: OTP, OLP, OLD,SCP
- Extremely low system component count
- Totally Lead-free & Fully RoHS Compliant (SO-7)
- Halogen and Antimony Free. "Green" Device

1.3 Applications

- Non-Isolated Home Appliances: AC Fans, Rice Cookers, Air conditioners, Coffee Machines, Soy Milk Machines, etc.
- Auxiliary Power for IoT Devices.

1.4 Board Pictures

Figure 1: Top View

Figure 2: Bottom View

Chapter2. Power Supply Specification

2.1 System Performance

The system performance contains input/output characters, specifications, EMC, protections, and etc.

		Min.	Typ.	Max.	Comments
Input Characters					
Input AC voltage rating		100V/60Hz	115/230	240V/50Hz	Two wires, no PE
Input AC voltage range		85V/60Hz	-	265V/50Hz	
Input AC frequency range		47Hz	50/60	63Hz	
Output Characters					
Output voltage		11.4V	12V	12.6V	Test at board terminal
Output tolerance		-		±5%	
loading current			175		mA
Performance Specifications					
Standby power		-		30mW	@230V/50Hz
Efficiency standard	10% load		76.62%	-	DoE VI: 71.97%
	Avg. eff.		81.06%	-	CoC V5 tier 2: 72.03%/62.03%
Load regulation		-	±2.47%	±5%	Tested at board terminal
Line regulation		-	±0.27%	±2%	Tested at board terminal
Ripple & Noise		-	70mV	100mV	@full load and full voltage range
Start up time		-	35ms	50ms	85V/60Hz
EMC Test					
ESD test	Air	15kV	-	-	@100ohm concrete resistor
	Contract	8kV	-	-	
EFT test		2kV	-	-	±5kHz/100kHz
Surge Test		1kV	-	-	Differential mode, 2ohm, 1.2/50us
Conduction EMI	110V	6dB margin	-	-	FCC Part 15 Class B
	230V	6dB margin	-	-	EN55022
Protection Functions					
SCP test		-	-		OK
OLD test		-	-	-	OK
OLP test		-	8.2V	-	OK
OTP test		135℃	150℃	165℃	OK

2.2 Environment

Operation temperature: -20℃~85℃
Operation Humidity: 20%~90% R.H.
Storage temperature: 0~40℃
Storage Humidity: 0%~95% R.H.

Chapter3. Schematic and Bill of Material

3.1 Schematic

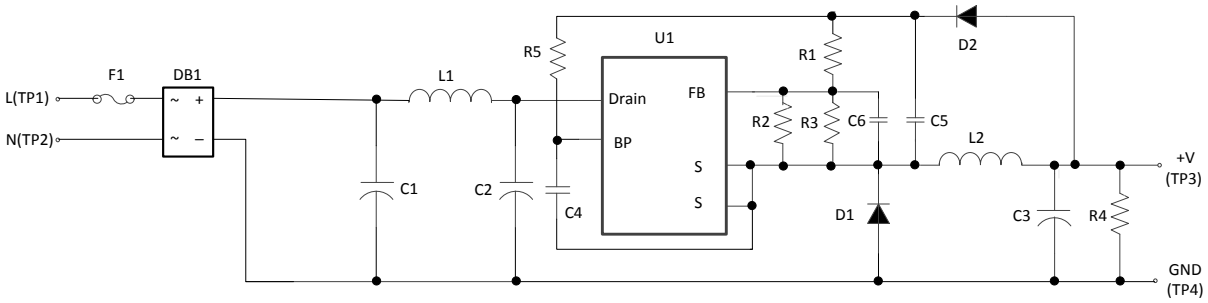

Figure 3: Evaluation Board Schematic

3.2 Bill of Material

Table 1: Bill of Material

Items	Designator	Description	Footprint	Qty.	Manufacturer
1	F1	10R, Fusible resistor	Φ3*10mm	1	OAHE
2	DB1	ABS10A	SOPA-4	1	Diodes
3	C1, C2	4.7uF/400V, Electrolytic capacitor	Φ8*12mm	2	Aishi
4	C3	150uF/25V, Electrolytic capacitor	Φ6*11mm	1	Aishi
5	C4	2.2uF/25V, X7R	SMD 0805	1	Telesky
6	C5	470nF/50V, X7R	SMD 0805	1	Telesky
7	C6	470pF/50V, X7R	SMD 0805	1	Telesky
8	D1	ES1J, Trr 35ns	SMA	1	Diodes
9	D2	RS1MSWFQ, Fast type diode, mark R1	SOD123F	1	Diodes
10	L1	1mH, Color ring inductor	DIP, 0510	1	Deloop
11	L2	1mH, Choke inductor	Φ9*12mm	1	Deloop
12	R1	22.1kΩ	SMD 0805, 1%	1	Panasonic
13	R2	5.62kΩ	SMD 0805, 1%	1	Panasonic
14	R3	NC	-	0	-
15	R4	20kΩ	SMD 0805, 5%	1	Panasonic
16	R5	27kΩ	SMD 0805, 5%	1	Panasonic
17	U1	AP3917C	SO-7	1	Diodes
Total		17pcs			

Chapter4. The Evaluation Board Connections

4.1 PCB Layout

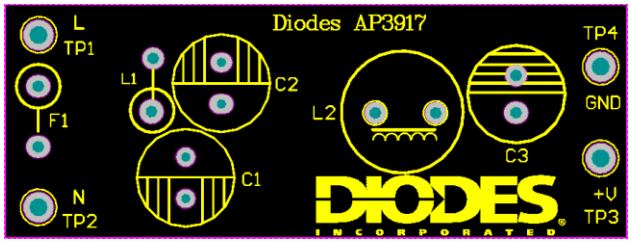

Figure 4: PCB Board Layout Top View

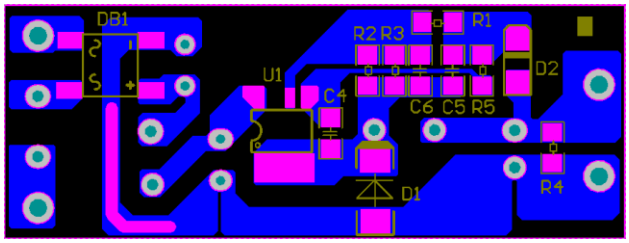

Figure 5: PCB Board Layout Bottom View

4.2 Circuit Description

4.2.1 Input EMI Filtering

The input stage is composed of fusible resistor F1, rectifier bridge DB1, filtering inductor L1, Capacitors C1 and C2. Resistor F1 is a flame proof, fusible, wire-wound resistor. It limits inrush current to safe levels for input rectifier diodes, provides differential mode noise reduction and acts as an input fuse in the event of short circuit.

4.2.2 Control IC

AP3917C co-packages a 650V power MOSFET and control circuitry into a cost-effective SO-7 package. The device is self-starting from the Drain pin with local supply decoupling provided by a small capacitor C4 (at least 100nF) connected to the BP pin when AC source is applied.

4.2.3 Output Rectification

During the ON time of U1, current ramps in L2 and is simultaneously delivered to the load. During the OFF time the inductor current ramps down via the free-wheeling diode D1, feedback diode D2, and the load. Diode D1 should be an ultra-fast diodes (Trr<50ns or lower). Capacitor C4 should be selected to have an adequate ripple margin (low ESR type).

4.2.4 Output Feedback

The voltage across L2 is rectified by C5 and D2 during the off-time of U1. For forward voltage drop of D1 and D2 is approximately equal, the voltage across C5 tracks the output voltage. To provide a feedback signal, the voltage across C5 is divided by R1 and R2. This voltage is specified for U1 at FB pin (2.5V). This allows the simple feedback to meet the required overall output tolerance of ±5% at rated output current.

4.3 Quick Start Guide

1. The evaluation board is preset at 12V/175mA from output.
2. Ensure that the AC source is switched OFF or disconnected before doing connection.
3. Connect the AC line wires of power supply to "L" & "N" connectors on the left side of the board.
4. Turn on the AC main switch.
5. Measure "+V" & "GND" connectors to ensure correct output voltage, 12V.

CAUTION: This EV board is non-isolated. Do not touch anywhere there are electrical connections because they are all coupled to high voltage potential.

Chapter 5. System Test

5.1 Input & Output Characteristics

5.1.1 Input Standby Power

Standby power and output voltage is measured after 10-minute aging. The voltage data is tested at the PCB terminal. All data is tested at ambient temperature.

Table 2: Standby Power and Output Voltage @no load

AC input Voltage	Pin (mW)	Vo (V)
85V/60Hz	19.2	12.478
115V/60Hz	21.1	12.485
230V/50Hz	27.0	12.415
265V/50Hz	28.7	12.410

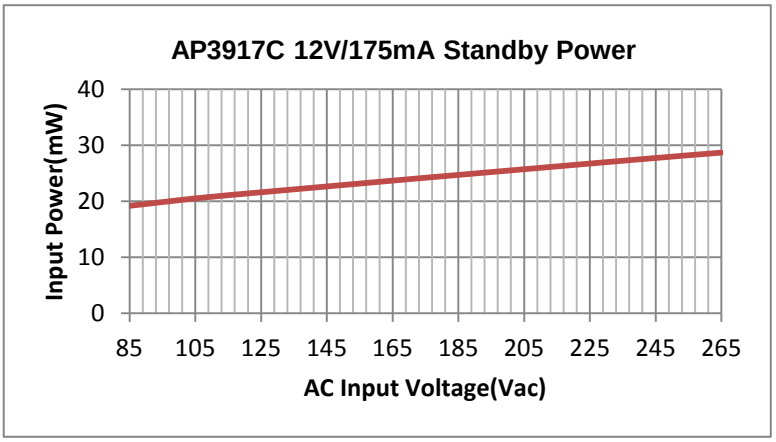

Figure 6: Standby Power versus Vin Curve

5.1.2 Efficiency

The efficiency data is measured after 10-minute aging, and it is tested at the PCB terminal. All the data is tested at ambient temperature.

Table 3: Conversion Efficiency

AC input voltage	Items	10%	25%	50%	75%	100%	Avg. Eff.
115V/60Hz	Vo (V)	12.101	12.016	11.944	11.920	11.878	**81.66**
	Io (mA)	17.50	43.75	87.50	108.75	175	
	Pin (W)	0.2683	0.6448	1.2776	1.5834	2.5522	
	Efficiency (%)	78.93	81.53	81.80	81.87	81.45	
230V/50Hz	Vo (V)	12.093	11.994	11.924	11.896	11.857	**81.06**
	Io (mA)	17.50	43.75	87.50	108.75	175	
	Pin (W)	0.2762	0.6555	1.2834	1.5755	2.5688	
	Efficiency (%)	76.62	80.05	81.30	82.12	80.78	

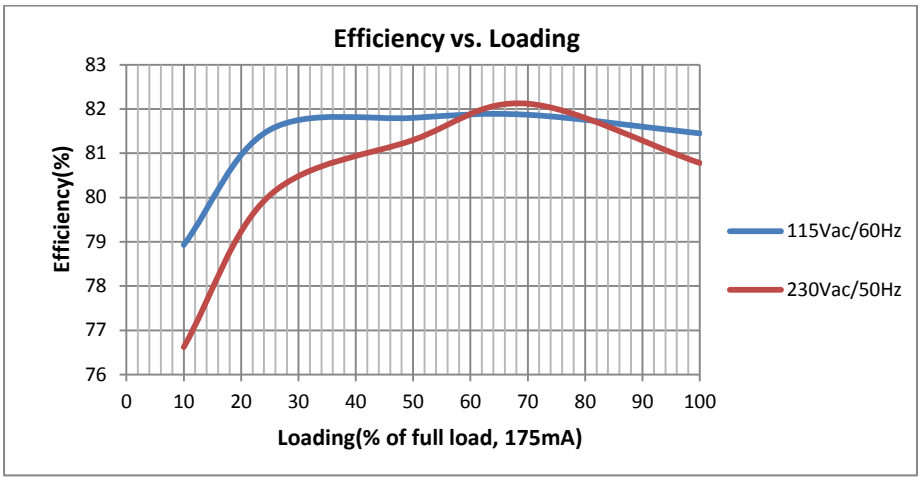

Figure 7: Efficiency versus Loading Curve

5.1.3 Line and Load Regulation

The line and load regulation data is measured after 10-minute aging. The voltage data is tested at the PCB terminal. All the data is tested at ambient temperature.

Table 4: Line and Load Regulation Data

AC input voltage	Loading(mA)						
	0	10	20	30	40	50	60
85Vac/60Hz	12.478	12.166	12.097	12.058	12.031	12.014	11.999
115Vac/60Hz	12.485	12.157	12.086	12.053	12.027	12.005	11.989
230Vac/50Hz	12.415	12.134	12.079	12.036	12.009	11.986	11.969
265Vac/50Hz	12.410	12.132	12.076	12.034	12.005	11.981	11.964
Line Regulation	±0.27%	±0.14%	±0.09%	±0.10%	±0.11%	±0.14%	±0.15%
AC input voltage	**Loading(mA)**						
	70	80	90	100	110	120	130
85Vac/60Hz	11.984	11.973	11.963	11.954	11.943	11.936	11.930
115Vac/60Hz	11.973	11.961	11.950	11.942	11.930	11.922	11.916
230Vac/50Hz	11.952	11.939	11.927	11.918	11.907	11.898	11.891
265Vac/50Hz	11.949	11.935	11.924	11.913	11.904	11.895	11.888
Line Regulation	±0.15%	±0.16%	±0.16%	±0.17%	±0.16%	±0.17%	±0.18%
AC input voltage	**Loading(mA)**					**Load Regulation**	**CV Regulation**
	140		160	170	175		
85Vac/60Hz	11.925	±2.38%	11.912	11.901	11.898	±2.38%	**±2.54%**
115Vac/60Hz	11.908	±2.47%	11.894	11.887	11.884	±2.47%	
230Vac/50Hz	11.883	±2.27%	11.871	11.866	11.864	±2.27%	
265Vac/50Hz	11.881	±2.27%	11.867	11.863	11.859	±2.27%	
Line Regulation	±0.18%	±0.18%	±0.19%	±0.16%	±0.16%	-	

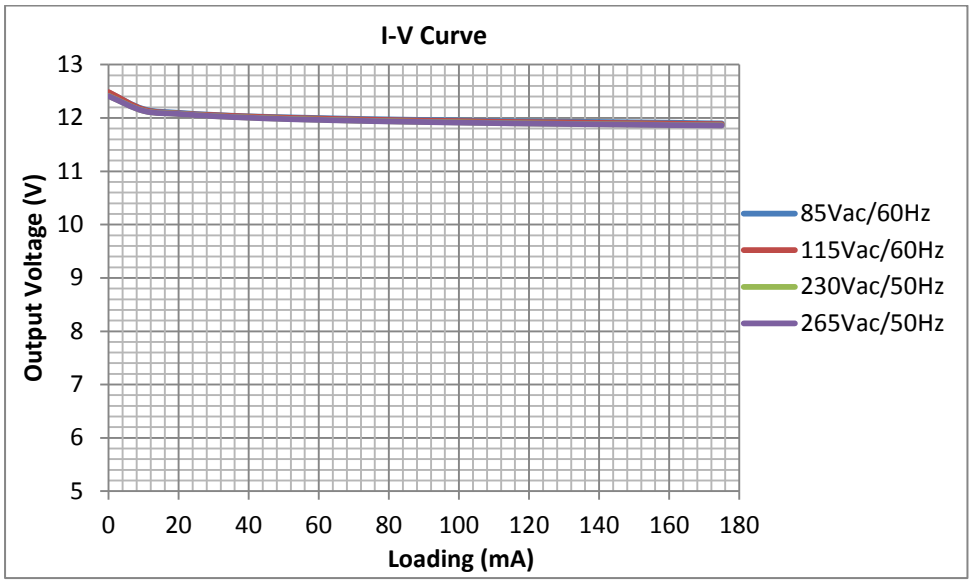

Figure 8: Output Voltage versus Loading Curve

5.2 Key Performance Test

5.2.1 Start up Performance

The start-up time is measured with a differential probe across AC inputs, "L" and "N" connectors and a common low-voltage probe across output terminals, "+V" and "GND" connectors. Before starting up, buck capacitors should be discharged.

Table 5: Start up Performance

AC input voltage	Loading conditions		Figures
	No load	Full load	
85Vac/60Hz	19.8ms	31.0ms	Fig. 9, Fig. 10
115Vac/60Hz	19.3ms	30.7ms	-
230Vac/50Hz	19.0ms	29.8ms	-
265Vac/50Hz	18.9ms	29.4ms	Fig. 11, Fig. 12

CH2:Vin; CH4:Vo

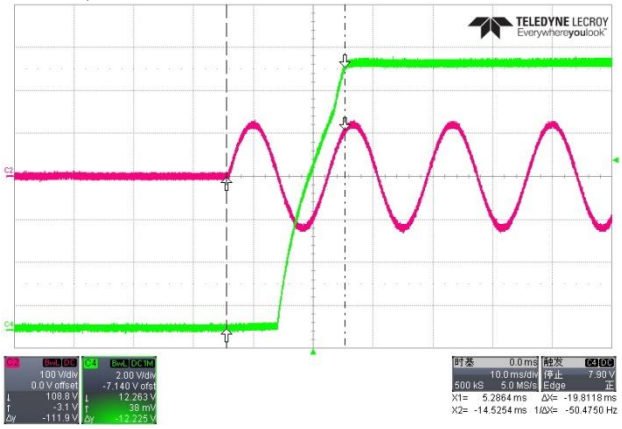

Figure 9: Start up time is 19.8ms @85Vac/60Hz, no load

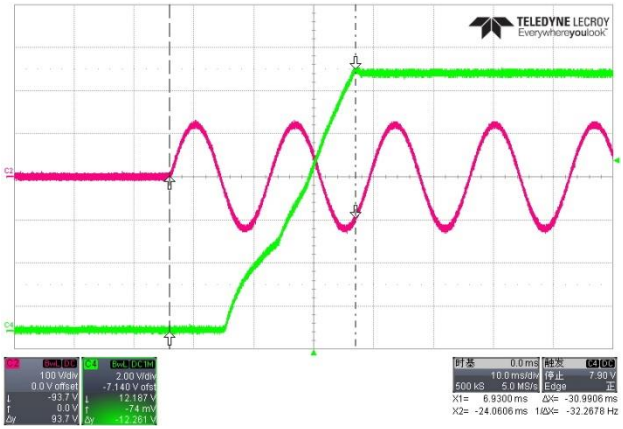

Figure 10: Start up time is 31.0ms @85Vac/60Hz, full load

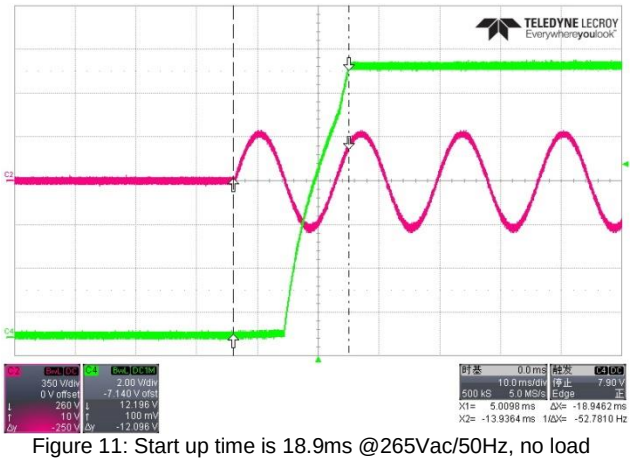

Figure 11: Start up time is 18.9ms @265Vac/50Hz, no load

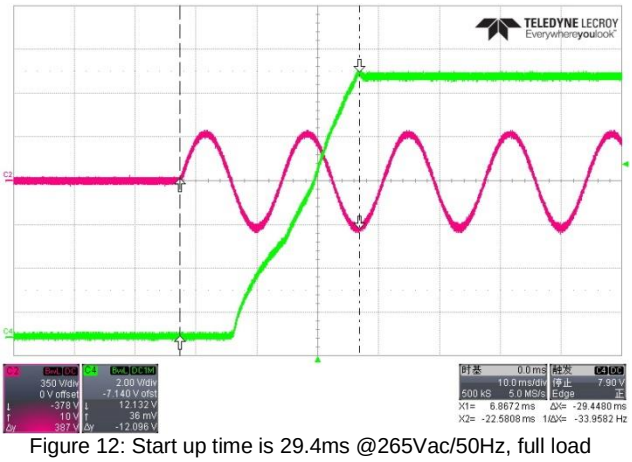

Figure 12: Start up time is 29.4ms @265Vac/50Hz, full load

5.2.2 Rise Time

The rise time is measured with a common low-voltage probe across output terminals, "+V" and "GND" connectors. Before starting up, output capacitors should be discharged.

Table 6: Rise Time

AC input voltage	Loading conditions		Figures
	No load	Full load	
85Vac/60Hz	11.3ms	21.8ms	Fig. 13, Fig.14
115Vac/50Hz	11.2ms	21.4ms	-
230Vac/50Hz	11.1ms	20.5ms	-
265Vac/50Hz	11.0ms	20.8ms	Fig. 15, Fig.16

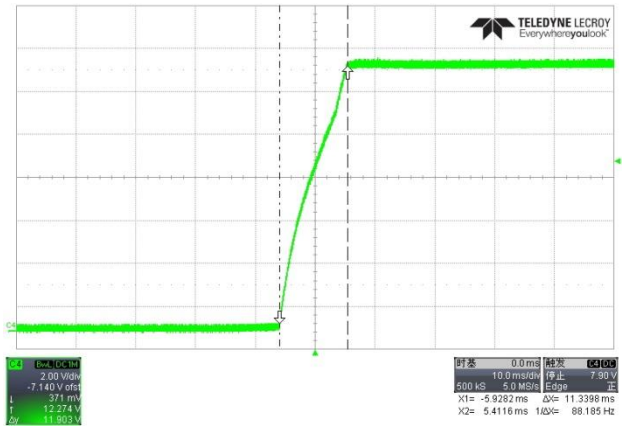

Fig. 13: Rise time is 11.3ms @85Vac/60Hz, no load

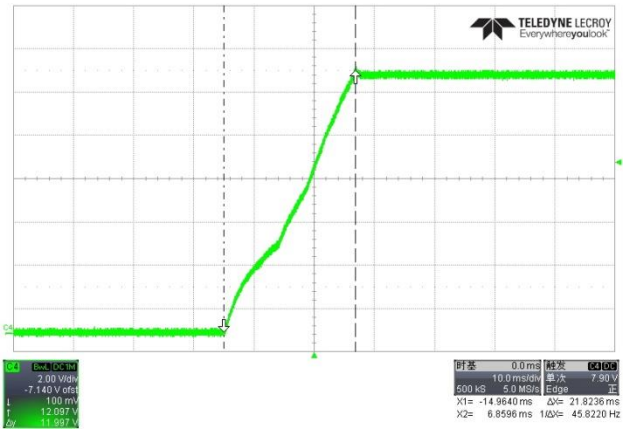

Fig 14: Rise time is 21.8ms @85Vac/60Hz, full load

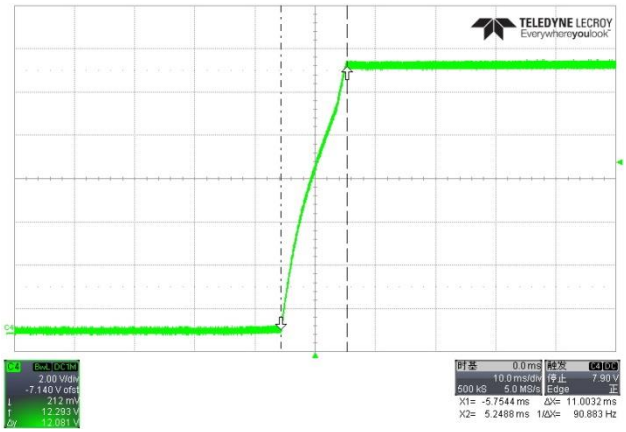

Figure 15: Rise time is 11.0ms @265Vac/50Hz, no load

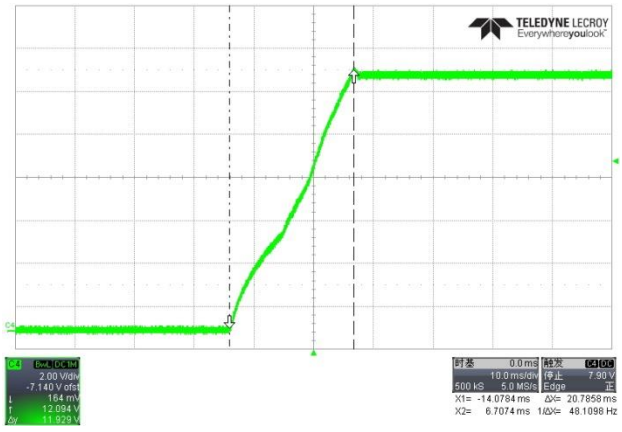

Figure 16: Rise time is 20.8ms @265Vac/50Hz, full load

5.2.3 Voltage Stress

The voltage is measured between the "Drain" and "S" pins of AP3917C. The test needs differential probes.

Table 7: Internal MOSFET Drain-Source Voltage Stress

AC input voltage	Loading conditions		Figures
	No load	Full load	
85Vac/60Hz	132V	138V	Fig. 17, Fig 18
115Vac/60Hz	181V	187V	-
230Vac/50Hz	354V	358V	-
265Vac/50Hz	406V	416V	Fig. 19, Fig. 20

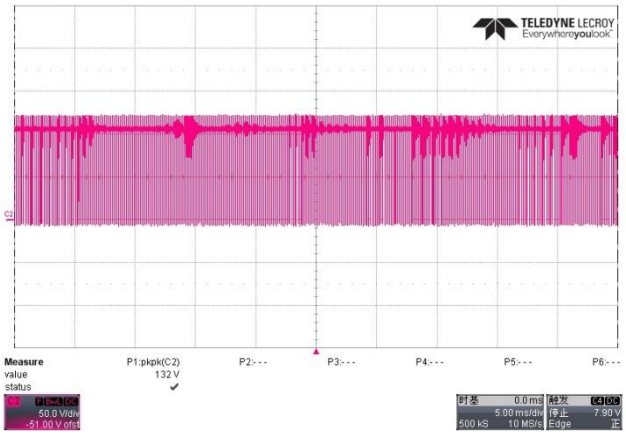

Figure 17: 132V@85Vac/60Hz, no load

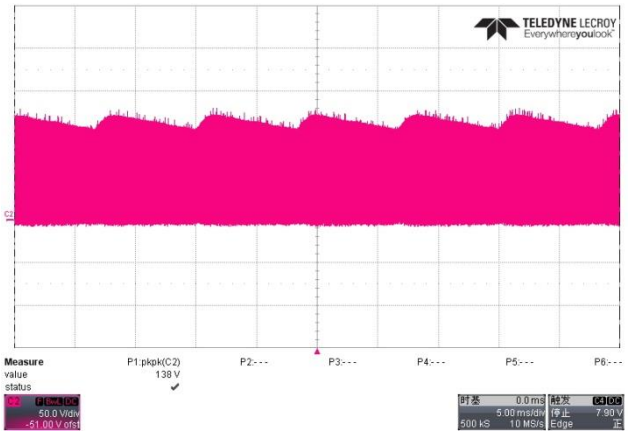

Figure 18: 138V@85Vac/60Hz, full load

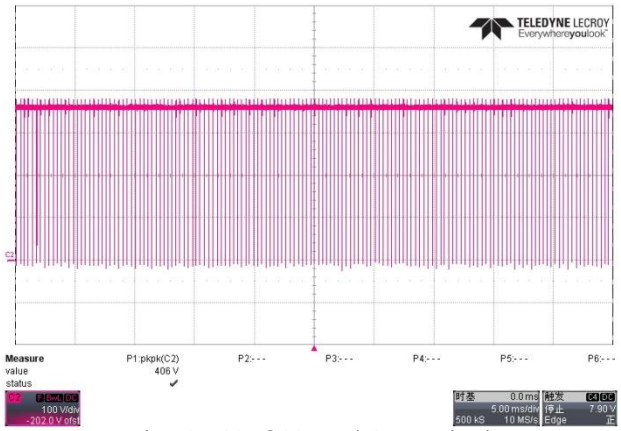

Fig. 19: 406V@265Vac/50Hz, no load

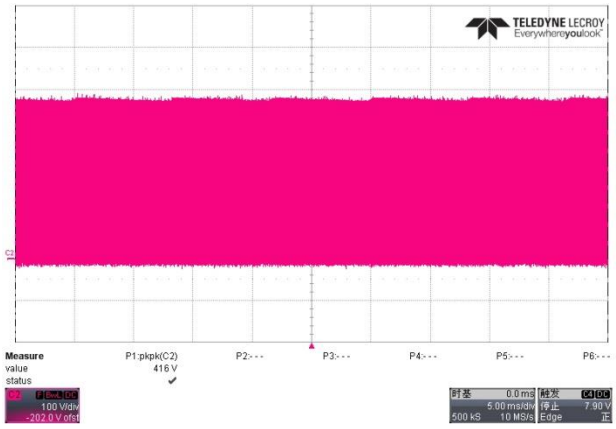

Fig. 20: 416V@265Vac/50Hz, full load

5.2.4 Output Ripple & Noise

The ripple and noise is tested at PCB terminal, using 10:1 probe without probe cap and ground clip. The bandwidth is limited to 20MHz. A 10uF electrolytic capacitor and a 100nF ceramic capacitor should be paralleled to the output terminal.

Table 8: Ripple & Noise

AC input voltage	Loading conditions		Figures
	No load	Full load	
85Vac/60Hz	15.4mV	68.5mV	Fig. 21, Fig.22
115Vac/60Hz	20.5mV	62.8mV	-
230Vac/50Hz	21.8mV	57.6mV	-
265Vac/50Hz	23.7mV	59.5mV	Fig. 23, Fig. 24

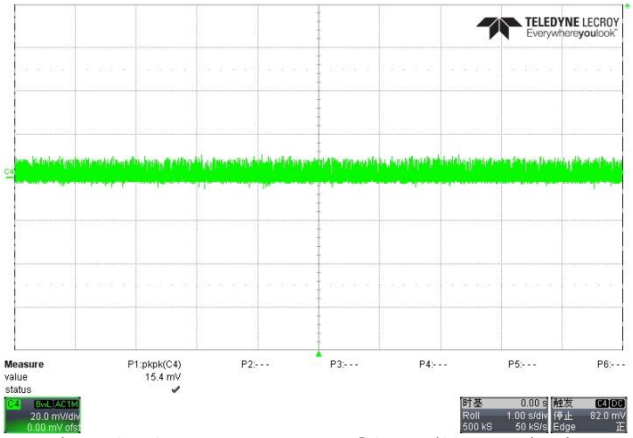

Figure 21: Output R&N, 15.4mV@85Vac/60Hz, no load,

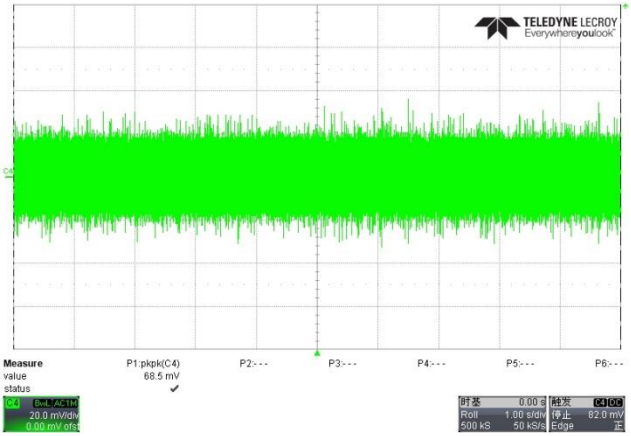

Figure 22: Output R&N, 68.5mV@85Vac/60Hz, full load,

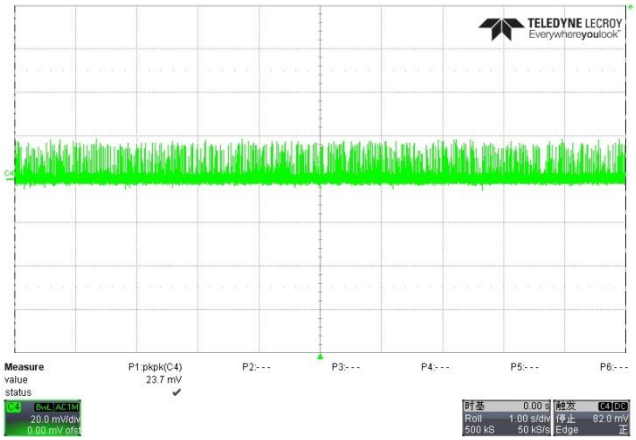

Figure 23: Output R&N, 23.7mV@265Vac/50Hz, no load

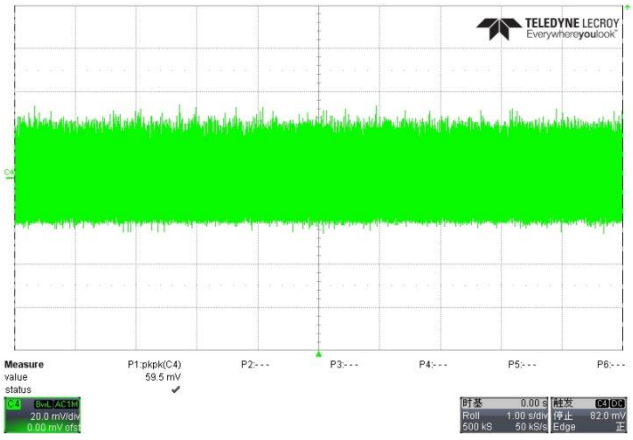

Figure 24: Output R&N, 59.5mV@265Vac/50Hz, full load

5.2.5 Dynamic Response

The dynamic response of output voltage is tested at the PCB terminal and the bandwidth is limited to 20MHz. Loading is set 0A as low load and 175mA as high load. Besides, the period is 2 seconds and the ramp is set at 250mA/us.

Table 9: Dynamic Response

AC input voltage	Output voltage			Figures
	Max Vo(V)	Min Vo(V)	Delta Vo(V)	
85Vac/60Hz	12.61	11.52	1.09	Fig. 25
115Vac/60Hz	12.67	11.46	1.21	-
230Vac/50Hz	12.54	11.46	1.08	-
265Vac/50Hz	12.54	11.46	1.08	Fig. 26

CH3: Io; CH4: Vo

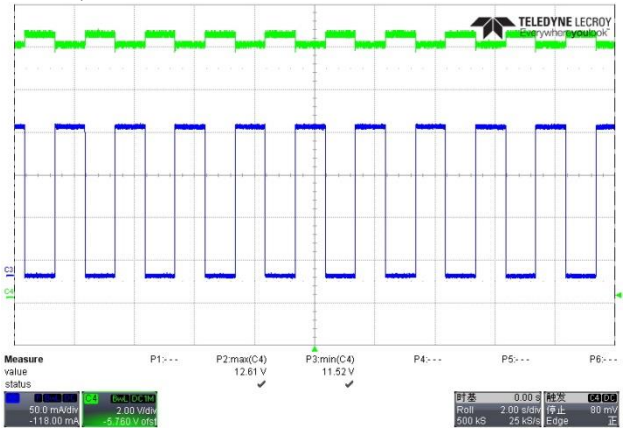

Figure 25: 12.61V~11.52V
@0~175mA,1s, 250mA/us, 85Vac/60Hz

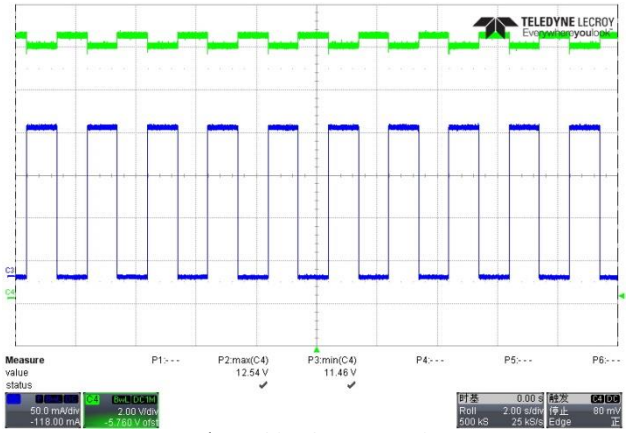

Figure 26: 12.54V~11.46V
@0~175mA,1s, 250mA/us, 265Vac/50Hz

5.3 Protection Test

5.3.1 Short Circuit Protection (SCP) Test

The SCP test is measured under the condition that output cable terminals are shorted. The resistance of output cable is 50mΩ.

Table 10: Short Circuit Protection Test

AC input voltage	Max Vo (mV)	Max Io(mA)	Vds(V)	Average input power (W)	Figures
85Vac/60Hz	320	349	134	0.480	Fig. 27
115Vac/60Hz	320	364	179	0.698	-
230Vac/50Hz	448	694	352	0.442	-
265Vac/50Hz	448	777	404	0.234	Fig. 28

CH2: Vds; CH3 :Io; CH4: Vo

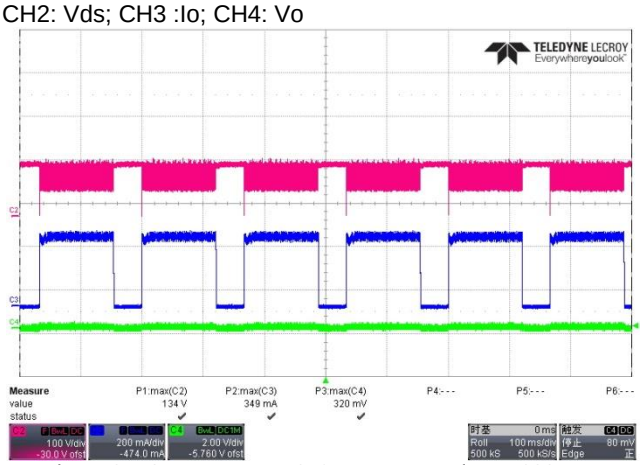

Figure 27: Output current, 349mA; output voltage, 320mV; Vds, 134V@output is shorted, 85Vac/60Hz

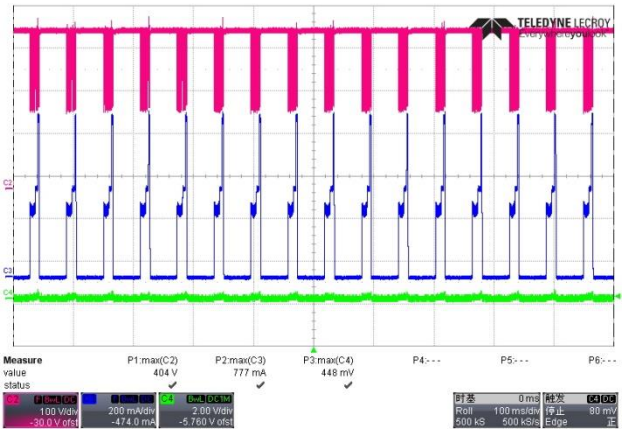

Figure 28: Output current, 777mA; output voltage, 448mV; Vds, 404V@output is shorted, 265Vac/50Hz

5.3.2 Open Loop Detection (OLD) Protection Test

The open loop detection protection is measured when FB pin is connected to Source pin.

Table 11: Open Loop Detection Test

AC input voltage	The peak of output voltage(V)	Figures
85Vac/60Hz	3.01	Fig. 29
115Vac/60Hz	3.07	-
230Vac/50Hz	3.20	-
265Vac/50Hz	3.20	Fig. 30

CH2: Vds; CH3 :Io; CH4 :Vo

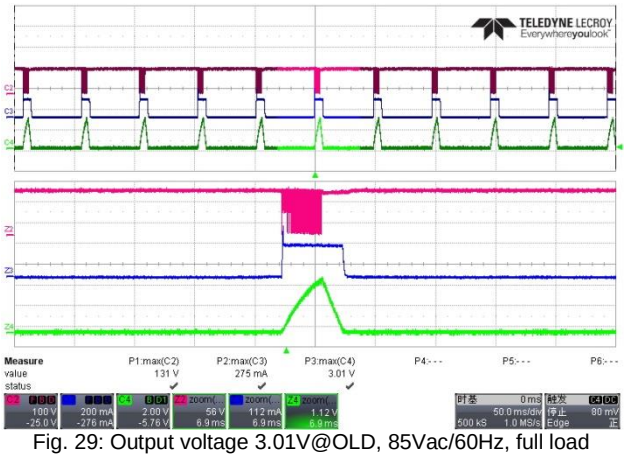

Fig. 29: Output voltage 3.01V@OLD, 85Vac/60Hz, full load

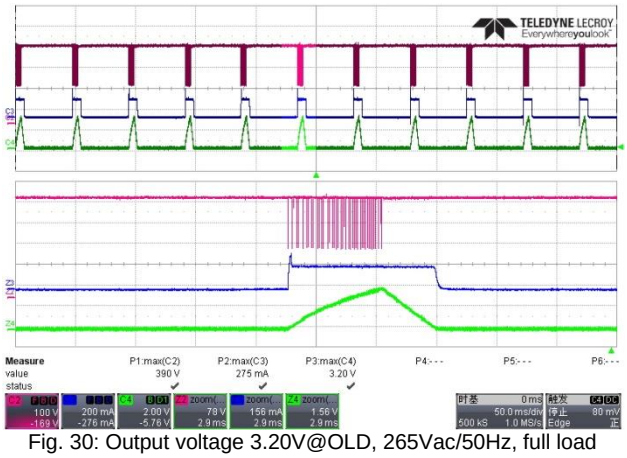

Fig. 30: Output voltage 3.20V@OLD, 265Vac/50Hz, full load

5.3.3 Over Load Protection (OLP) Test

The over load protection point is tested as below: increase the loading by 10mA/step until the system cannot maintain a stable output, and then mark the loading level as over load protection point.

Table 12: Over Load Protection Point test

AC input voltage	Over load protection point(mA)
85Vac/60Hz	250
115Vac/60Hz	250
230Vac/50Hz	250
265Vac/50Hz	250

5.4 Thermal Test

The thermal test is under ambient temperature after 1-hour aging. The board has no case in open frame. Thermal imager is used to observe the surface temperature of AP3917C and the free-wheeling diode, D1.

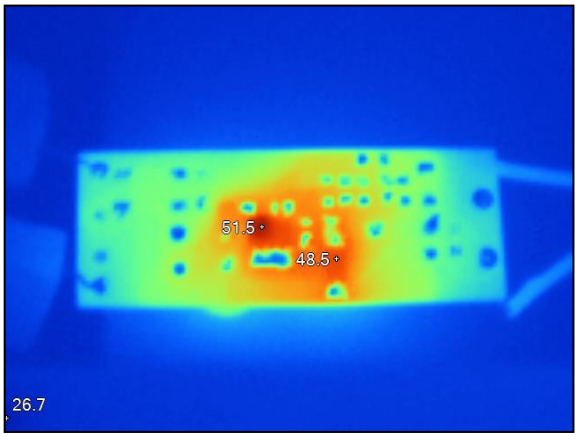

Figure 31: AP3917C, 51.5℃; D1, 48.5℃
@85Vac/60Hz, full load, ambient temperature, 25℃.

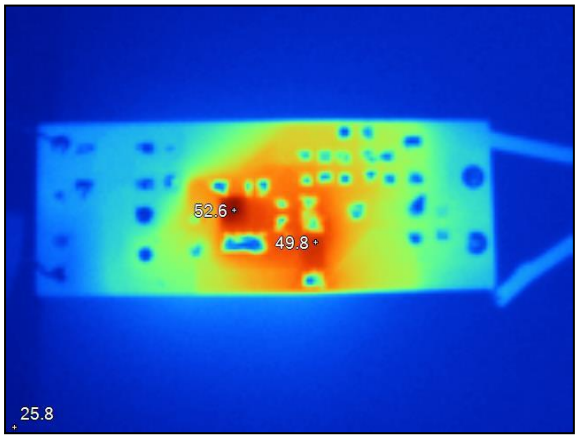

Figure 32: AP3917C, 52.6℃; D1, 49.8℃
@ 265Vac/50Hz, full load, ambient temperature, 25℃.

5.5 System EMI Scan

The power supply meets EN55022 Class B (for 230Vac input) and FCC part 15 (for 110Vac input) EMI requirements with more than 6dB margin.

5.5.1 Conduction EMI Test of 230V@full load

The test result can pass EN55022 Class B limit with more than 6dB margin.

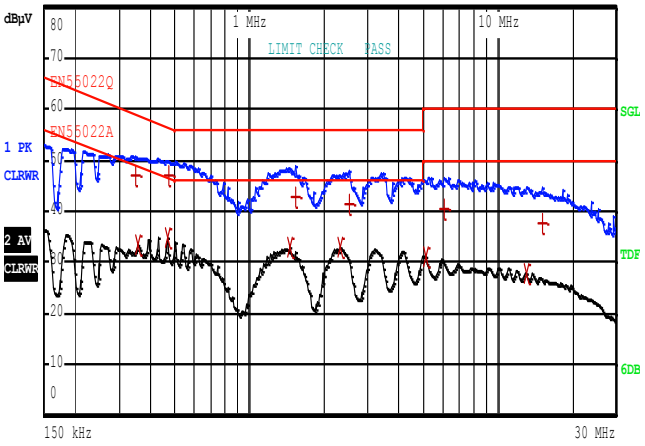

Fig. 33, L line conduction waveform@230Vac/50Hz, full load.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	346.008411606 kHz	47.22	-11.83
2	Average	352.963180679 kHz	33.33	-15.55
2	Average	466.367062279 kHz	34.69	-11.88
1	Quasi Peak	471.030732902 kHz	47.22	-9.27
2	Average	1.44998824519 MHz	32.79	-13.20
1	Quasi Peak	1.52395221823 MHz	42.87	-13.12
2	Average	2.31456322894 MHz	32.80	-13.19
1	Quasi Peak	2.50634031306 MHz	41.30	-14.69
2	Average	5.13072753076 MHz	30.96	-19.03
1	Quasi Peak	6.07634335085 MHz	40.44	-19.55
2	Average	12.9439466322 MHz	27.88	-22.11
1	Quasi Peak	15.0275202 MHz	37.77	-22.22

Fig. 34, L line conduction data@230Vac/50Hz, full load.

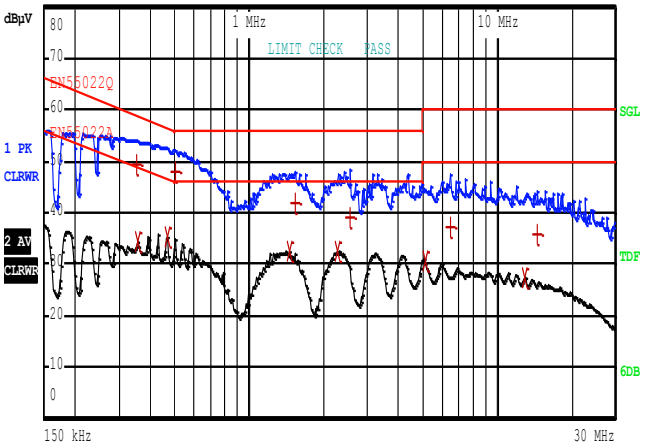

Figure 35: N line conduction waveform@230Vac/50Hz, full load.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	349.468495722 kHz	49.55	-9.42
2	Average	352.963180679 kHz	34.28	-14.61
2	Average	466.367062279 kHz	35.39	-11.18
1	Quasi Peak	505.008700673 kHz	48.16	-7.83
2	Average	1.44998824519 MHz	32.58	-13.41
1	Quasi Peak	1.52395221823 MHz	41.99	-14.00
2	Average	2.26895718944 MHz	32.37	-13.62
1	Quasi Peak	2.53140371619 MHz	39.14	-16.85
2	Average	5.13072753076 MHz	30.55	-19.44
1	Quasi Peak	6.45016090889 MHz	37.20	-22.79
2	Average	12.8157887448 MHz	27.51	-22.48
1	Quasi Peak	14.4411515385 MHz	35.83	-24.16

Figure 36: N line conduction data@230Vac/50Hz, full load.

5.5.2 Conduction EMI Test of 110V@full load

The test result can pass FCC part 15 limit with more than 6dB margin.

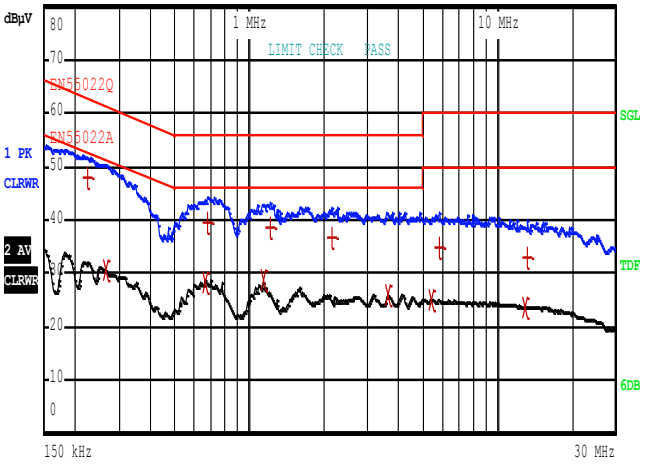

Figure 37: L line conduction waveform@110Vac/60Hz, full load.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	221.118376275 kHz	47.97	-14.80
2	Average	264.49018761 kHz	30.76	-20.52
2	Average	660.656865747 kHz	28.35	-17.64
1	Quasi Peak	673.936068749 kHz	39.44	-16.56
2	Average	1.13065507631 MHz	28.56	-17.43
1	Quasi Peak	1.21221527836 MHz	38.78	-17.21
1	Quasi Peak	2.1374603093 MHz	36.76	-19.23
2	Average	3.6218534158 MHz	25.73	-20.26
2	Average	5.39244619915 MHz	24.87	-25.12
1	Quasi Peak	5.83924652649 MHz	34.64	-25.35
2	Average	12.8157887448 MHz	23.83	-26.16
1	Quasi Peak	13.0733860985 MHz	33.12	-26.87

Figure 38: L line conduction data@110Vac/60Hz, full load.

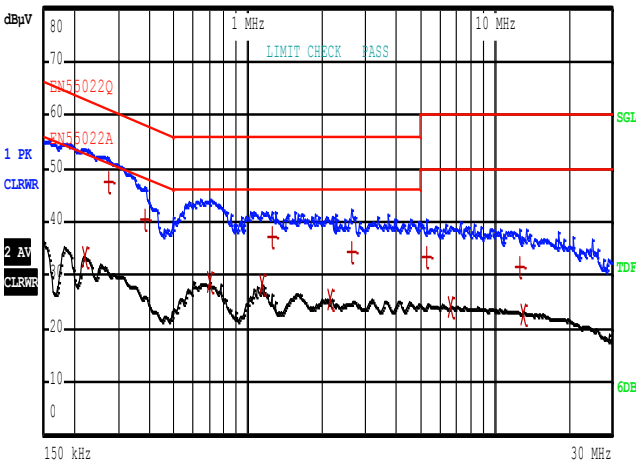

Figure 39: N line conduction waveform@110Vac/60Hz, full load.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	216.761470714 kHz	33.49	-19.44
1	Quasi Peak	272.504504785 kHz	47.46	-13.57
1	Quasi Peak	382.208547038 kHz	40.61	-17.61
2	Average	694.357005568 kHz	28.86	-17.13
2	Average	1.13065507631 MHz	28.30	-17.69
1	Quasi Peak	1.2489466135 MHz	37.25	-18.74
2	Average	2.1374603093 MHz	25.31	-20.68
1	Quasi Peak	2.634188858 MHz	34.41	-21.58
1	Quasi Peak	5.28619370567 MHz	33.38	-26.62
2	Average	6.57980914316 MHz	24.15	-25.84
1	Quasi Peak	12.5632670765 MHz	31.55	-28.44
2	Average	12.9439466322 MHz	22.89	-27.11

Figure 40: N line conduction data@110Vac/60Hz, full load.

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