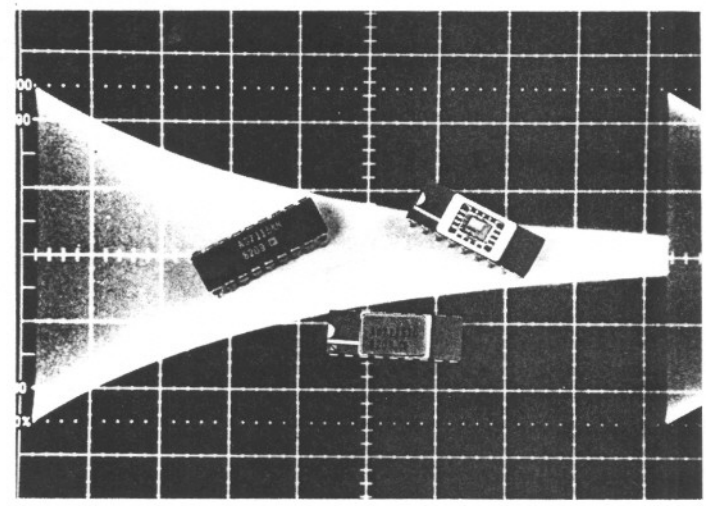
LOGDAC™
CMOS 0.1dB Step Attenuator
AD7115

FEATURES
Dynamic Range: 0 to 19.9dB Plus Full Muting
Resolution: 0.1dB
2 1/2 Digit BCD Input Coding
On-Chip Data Latches
Full ±25V Input Range
Low Distortion and Noise
Latch-Up Free (No Protection Schottky Required)
TTL Compatible

APPLICATIONS
Audio Attenuators
Function Generators
Test Equipment
Digitally Controlled AGC Systems



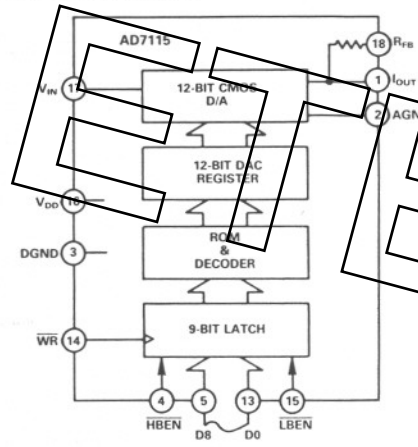
GENERAL DESCRIPTION
The AD7115 is a digitally programmable attenuator which attenuates an analog input signal over the range 0 to −19.9dB in 0.1dB steps.

The degree of attenuation is controlled by a 2 1/2 digit BCD coded input word which is latched into on-chip data latches using microprocessor compatible control signals $\overline{WR}$, $\overline{LBEN}$ and $\overline{HBEN}$. Operating frequency range of the device is from dc to several hundred kHz.

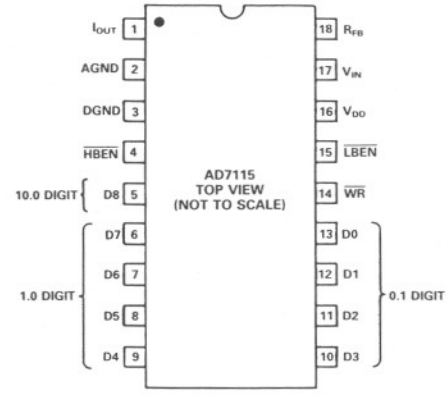
The device is packaged in an 18-pin dual-in-line plastic, cerdip or ceramic package.

PRODUCT HIGHLIGHTS
1. High resolution 0.1dB steps from 0 to 19.9dB with step accuracies better than ±0.04dB allow precision attenuators and other special purpose function generators to be built at low cost.
2. A resolution of 0.1dB is equivalent to step sizes of 1% of reading.
3. The 2 1/2 digit BCD input code can be loaded into the on-chip latches in one $\overline{WRITE}$ operation. Alternatively, for use with an 8-bit data bus, data can be loaded in two $\overline{WRITE}$ operations by using byte enable signals $\overline{HBEN}$ and $\overline{LBEN}$.
4. The AD7115 can be used in series with standard attenuator blocks to position its attenuation range as required, e.g., −40dB to −60dB in 0.1dB steps.
5. Analog input signal can be up to ±25V with V_{DD} = +5V.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



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SPECIFICATIONS (V_{DD} = +5V, V_{IN} = −10V dc, V_{PIN1} = V_{PIN2} = 0V, output amplifier AD544 except where stated)

Parameter	T_A = +25°C	T_A = T_{min}, T_{max}	Units	Conditions/Comments
NOMINAL RESOLUTION	0.1	0.1	dB	Full range is from 0 to 19.9dB. A resolution of 0.1dB is equivalent to steps of 1% of Reading
ACCURACY RELATIVE TO 0dB ATTENUATION	±0.04	±0.05	dB max	Accuracy is measured using circuit of Figure 4 and excludes any gain error effects due to mismatch between R_{FB} and the R-2R ladder circuit.
GAIN ERROR (at 0dB)	±0.1	±0.12	dB max	Typical gain change over 100°C range is ±0.01dB
INPUT RESISTANCE V_{IN} (pin 17), R_{FB} (pin 18)	7/11/18	7/11/18	kΩ min/typ/max	
DIGITAL INPUTS V_{IH} (Input High Voltage) V_{IL} (Input Low Voltage) Input Leakage Current	 2.4 0.8 ±1	 2.4 0.8 ±10	 V min V max µA max	 Digital Inputs = V_{DD} or 0V
SWITCHING CHARACTERISTICS[2] t_{WR} t_{DS} t_{DH} t_{ENS} t_{ENH} t_{REFSH}	 600 170 10 0 0 4	 800 250 10 0 0 6	 ns min ns min ns min ns min ns min µs min	 Write Pulse Width. See Figure 1. Data Valid to Write Setup Time Data Valid to Write Hold Time Byte Enable to Write Setup Time Byte Enable to Write Hold Time Refresh Time
POWER SUPPLY V_{DD} I_{DD}	 +5 4	 +5 4	 V mA max	 Digital Inputs = V_{IH} or V_{IL}, See Figure 10.

NOTES
[1]Temperature range as follows: KN Version; 0 to +70°C
BQ Version; −25°C to +85°C
TD Version; −55°C to +125°C
[2]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test
V_{DD} = +5V, V_{IN} = −10V dc except where stated, V_{PIN1} = V_{PIN2} = 0V, output amplifier AD544 except where stated.

Parameter	T_A = +25°C	T_A = T_{min}, T_{max}	Units	Conditions/Comments
DC SUPPLY REJECTION $\Delta GAIN/\Delta V_{DD}$	0.0066	0.033	dB per V max	ΔV_{DD} = ±0.5V Input Code = 00.0 BCD
PROPAGATION DELAY	5	7	µs max	Full Scale Change Measured from $\overline{WR}$ going HIGH, $\overline{LBEN}$ = $\overline{HBEN}$ = 0V. See definitions on next page.
DIGITAL TO ANALOG CHARGE INJECTION, QDA	600	–	nV secs typ	Measured with ADLH0032CG as output amplifier for input code transition 00.0 BCD to Full Mute Code. See Figure 4, C1 = 0pF.
OUTPUT CAPACITANCE, PIN 1	150	150	pF max	For 00.0 input code. Output capacitance is code dependent and decreases with increasing attenuation.
FEEDTHROUGH AT 1kHz[1]	−92 −96	−68 −76	dB max dB typ	Feedthrough is also determined by circuit layout (see Figure 5).
TOTAL HARMONIC DISTORTION	−91	−91	dB typ	V_{IN} = 6V rms at 1kHz
OUPUT NOISE VOLTAGE DENSITY	70	70	nV/√Hz typ	Includes AD544 amplifier noise. From 20Hz to 20kHz.
SIGNAL INPUT CAPACITANCE V_{IN} (pin 17), R_{FB} (pin 18)	10	10	pF max	
DIGITAL INPUT CAPACITANCE Control Input Data Input	 10 5	 10 5	 pF max pF max	

NOTES
[1] Feedthrough may be further reduced by grounding the metal lid on the suffix D package.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	+7V
V_{IN} to AGND	±35V
V_{RFB} to AGND	±35V
Digital Input Voltage to DGND	−0.3V to V_{DD}
Output Voltage (Pin 1) to AGND	−0.3V to V_{DD}
AGND to DGND	0 to V_{DD}
DGND to AGND	0 to V_{DD}
Power Dissipation (Package)	
Plastic (suffix N)	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic (Suffix D) or Cerdip (Suffix Q)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial Plastic (KN Version)	0 to +70°C
Industrial Cerdip (BQ Version)	−25°C to +85°C
Military Ceramic (TD Version)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

Resolution: Nominal change in attenuation when moving between two adjacent codes.

Monotonicity: The device is monotonic if the analog output decreases (or remains constant) as the digital code (attenuation setting) increases.

Feedthrough Error: That portion of the input signal which reaches the output when the DAC is muted. See section on Dynamic Performance.

Output Leakage Current: Current which appears on the I_{OUT} terminal when the DAC is muted.

Total Harmonic Distortion: A measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

Gain Error: Gain Error is due to mismatch between R_{FB} and the R-2R ladder circuit and is a constant percentage of reading (i.e. constant dB offset) over the entire code range. Gain error can be trimmed to zero.

Accuracy: The difference (measured in dB) between the ideal transfer function and the actual transfer function as measured with the device after calibration for 0dB gain error.

Output Capacitance: Capacitance from I_{OUT} to ground.

Digital to Analog Charge Injection (QDA): The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Secs or nV-Secs depending upon whether the glitch is measured as a current or voltage signal. QDA is measured with V_{IN} = AGND.

Propagation Delay: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

ORDERING INFORMATION

		Temperature Range and Package		
Relative Accuracy T_{min} to T_{max}	Gain Error T_A = +25°C	Plastic 0 to +70°C	Cerdip[1] −25°C to +85°C	Ceramic −55°C to +125°C
±0.05dB	±0.1dB	AD7115KN	AD7115BQ	AD7115TD

NOTE:
[1]Analog Devices reserves the right to ship ceramic packages in lieu of Cerdip packages.

CIRCUIT DESCRIPTION

The AD7115 consists of a 12-bit R-2R CMOS multiplying D/A converter with extensive digital logic. The logic translates the 2 1/2 digit BCD input code into a 12-bit word which is used to drive the D/A converter. Input data is loaded into the input latches under the control of $\overline{WR}$ (WRITE) and byte enable signals $\overline{LBEN}$ (LOW BYTE ENABLE) and $\overline{HBEN}$ (HIGH BYTE ENABLE). The rising edge of $\overline{WR}$ latches the input data. See Figure 1 for the data loading waveforms using an 8-bit data bus.

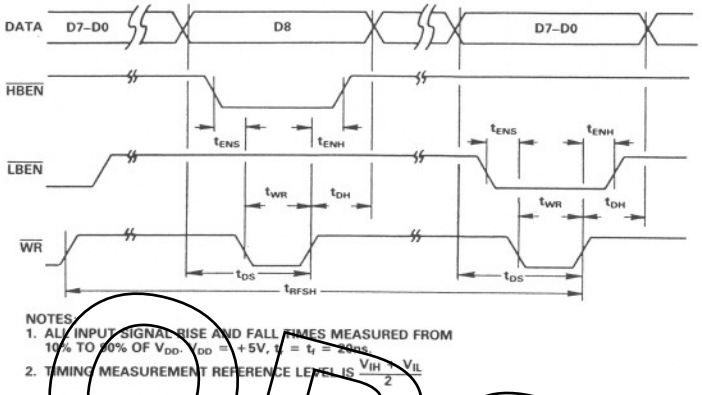


Figure 1. Data Loading Waveforms with 8-Bit Data Bus

In applications where the input data bus is at least nine bits wide $\overline{LBEN}$ and $\overline{HBEN}$ can be exercised together to load new data in one write operation. For 8-bit data bus applications two write operations are required to load completely new data into the AD7115. Table 1 shows the data loading truth table.

AD7115 Control Inputs			AD7115 Operation
$\overline{WR}$	$\overline{HBEN}$	$\overline{LBEN}$	
1	X	X	No Operation
X	1	1	No Operation
↓	0	1	Load HIGH Byte
↓	1	0	Load LOW Byte and Update DAC Register
↓	0	0	Load HIGH and LOW Byte and Update DAC Register

NOTES
1. X indicates "don't care" states.
2. ↓ indicates LOW to HIGH transition.

Table 1. Data Loading Truth Table

Note that $\overline{HBEN}$ and $\overline{WR}$ simply load D8 data into the input latch whereas $\overline{LBEN}$ and $\overline{WR}$ load D7–D0 into the input latch and on the rising edge of $\overline{WR}$ updates the DAC register with the input latch contents (D8–D0) approximately 5μs later. Thus the proper sequence for loading completely new data into the AD7115 from an 8-bit bus is a high byte load followed by a low byte load. After any low byte load operation a minimum time is required for the data to propagate through the decoder before another low byte load operation is attempted. This time is the refresh time, t_{RFSH}, of Figure 1.

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7115 and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices, approximately doubles every 10°C – see Figure 12. The resistor R_O as shown in Figure 3 is the equivalent output resistance of the device which varies with input code from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the current steering switches S1 to S12 and varies from about 40pF to 150pF depending upon the digital input. For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" which is available from Analog Devices, Inc., Publication Number G479–15–8/78.

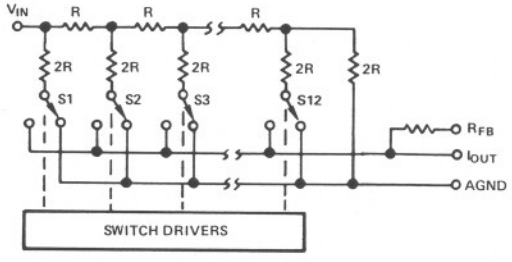


Figure 2. Simplified D/A Circuit of AD7115

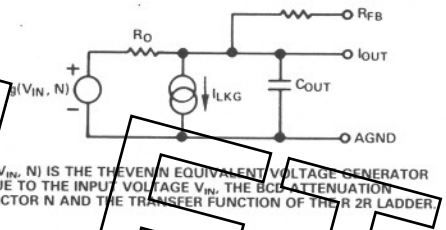


Figure 3. Equivalent Analog Output Circuit of AD7115

TYPICAL CIRCUIT CONFIGURATION

Figure 4 shows the AD7115 in a typical circuit configuration with an AD544. The transfer function for this circuit is given by:

$$V_O = -V_{IN}\ 10\ \exp\ -\left(\frac{0.1N}{20}\right)$$

Where 0.1 is the step size (resolution) in dB and N is the BCD input code, 0 to 199.

Note that a number of non-BCD codes exist which allow the user to mute the output, i.e., to achieve infinite attenuation. The basic mute code is XX0XX1111 for D8 to D0 respectively where X is a "don't care" input.

For example, 000001111 is one such suitable code.

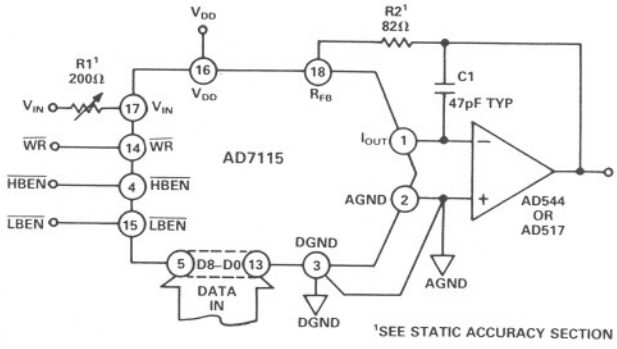


Figure 4. Typical Circuit Configuration

DYNAMIC PERFORMANCE

The dynamic performance of the AD7115 will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Figure 5 shows a printed circuit layout which minimizes feedthrough from V_{IN} to the output in multiplying applications. Circuit layout is most important if the optimum performance of the AD7115 is to be achieved. Most application problems stem from poor layout, grounding errors, or inappropriate choice of amplifier.

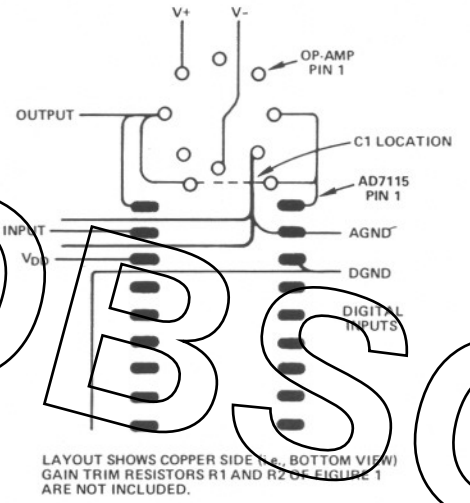


Figure 5. Suggested Layout for AD7115 and Op-Amp (Not to Scale)

It is recommended that when using the AD7115 with a high speed amplifier, a capacitor (C1) be connected in the feedback path as shown in Figure 4. This capacitor, which should be between 20pF and 50pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 6 and 7 show the performance of the AD7115 using the AD517, a fully compensated high gain superbeta amplifier, and the AD544, a fast FET input amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit is shown in the bottom trace.

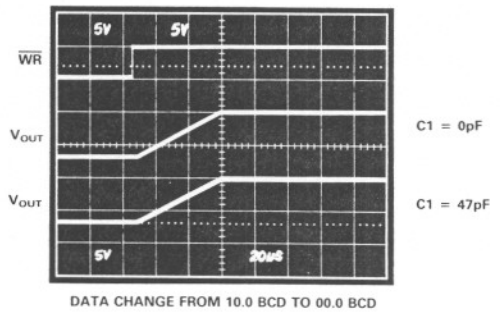


Figure 6. Response of AD7115 with AD517

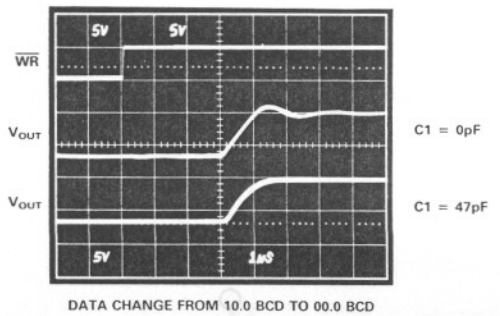


Figure 7. Response of AD7115 with AD544

For operation beyond 250kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figures 7 and 11. In circuits when C1 is not included, the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7115.

Feedthrough and absolute accuracy are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7115 be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 12.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7115 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

STATIC ACCURACY PERFORMANCE

The choice of output amplifier will be strongly influenced by the absolute attenuation range over which the AD7115 is to operate, e.g., from 0 to −20dB, −20dB to −40dB, −40dB to −60dB, etc. To obtain optimum static performance from the device (especially at high absolute attenuation levels as shown for Figure 8), it is necessary to play close attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to the current flowing through the feedback resistor R_{FB}. It is recommended that an amplifier with an input bias current of less than 10nA be used (e.g., AD517 or AD544) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7115 output impedance) varies as a function of attenuation level. This has the effect of varying the "noise" gain of the amplifier, thus creating a varying error due to amplifier offset voltage. It is recommended that an amplifier with less than 50μV of input offset be used (such as the AD517 or AD OP-07) in dc applications. Amplifiers with higher offset voltage may cause audible "thumps" in ac applications due to dc output changes.

The AD7115 accuracy is specified and tested using only the internal feedback resistor. Any Gain Error (i.e., mismatch of R_{FB} to the R-2R ladder) that may exist in the AD7115 D/A converter circuit results in a constant attenuation error over the whole range. The AD7115 accuracy is specified relative to 0dB attenuation, hence "Gain" trim resistors – R1 and R2 in Figure 4 – can be used to adjust $V_{OUT} = V_{IN}$ precisely (i.e., 0dB attenuation) with input code 00.0BCD. The accuracy specifications of the AD7115 are not affected in any way by this gain trim procedure. For the AD7115K/B/T grades, suitable values for R1 and R2 of Figure 4 are R1 = 200Ω, R2 = 82Ω.

For additional information on gain error the reader is referred to Application Note "Gain Temperature Coefficient of CMOS Multiplying DACs" by Phil Burton available from Analog Devices, Inc., Publication Number E630–10–6/81.

0 TO 80dB ATTENUATOR WITH 0.1dB RESOLUTION

It is possible to extend the attenuation range beyond 20dB by using a precision attenuator or programmable gain amplifier in series with the AD7115 to provide a fixed amount of the total attenuation required. Figure 8 shows one possible configuration where a precision resistor divider string provides tapped outputs at signal levels 0dB, −20dB, −40dB and −60dB below the input signal level. The switch used, an AD7591DI, is a quad SPST switch with on-chip data latches. The output signal is buffered by an AD517 amplifier before being applied to the input pin, V_{IN}, of the AD7115. The accuracy and monotonicity range, particularly when switching from one 20dB segment to another is critically dependant on the resistor divider tolerances. Other error sources include leakage currents of the AD7591DI switches, signal source impedance, offset drift of the buffer AD517 amplifier and feed-through. These may be minimized by operating the circuit as close to +25°C as possible and by paying due attention to circuit layout and shielding.

Decoder Inputs D10	D9	Attenuation
0	0	0dB via S1
0	1	−20dB via S2
1	0	−40dB via S3
1	1	−60dB via S4

Table 2. Decoder Truth Table for Figure 8

Note that the data inputs D10–D0 of Figure 8 may be driven by a three digit BCD coded word. The lower two digits and the "1" line of digit 3 control the AD7115. The "4" and "2" lines of digit 3 feed D10 and D9 respectively to control the precision divider. This arrangement allows the circuit attenuation to be programmed from 0dB to 79.9dB with 0.1dB resolution by a corresponding three digit BCD word.

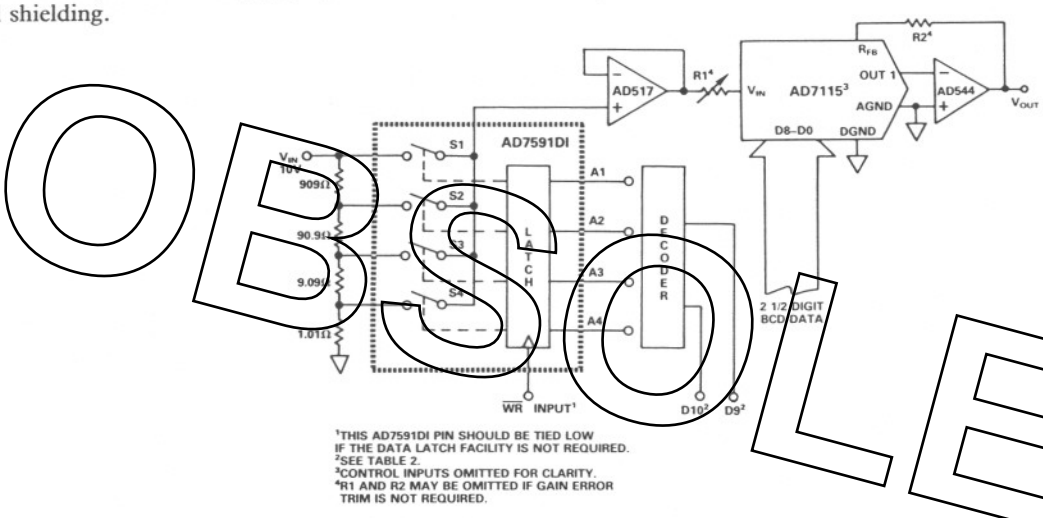


Figure 8. 0 to 80dB Attenuator with 0.1dB Resolution

THUMBWHEEL SWITCH ATTENUATOR

Figure 9 shows the AD7115 when used as a simple stand-alone thumbwheel switch attenuator. The BCD coded thumbwheel assembly applies BCD data to the AD7115 data inputs. Resistor R3 limits current if make before break switches are used. The facility to mute the output is provided by gates G1 to G6 and SPDT switch S1. A number of alternatives exist for generating the $\overline{WR}$ pulse required to load new data into the AD7115, a push-button switch S2 as shown in Figure 9 being the simplest. Alternatively the $\overline{WR}$ input can be driven by a simple oscillator to provide continuous $\overline{WR}$ pulses. Another option allows automatic loading of new data whenever any of the thumbwheel switches are moved. This requires switches which have guaranteed make before break action. Moving any thumbwheel switch to a new setting will cause a momentary pulse of current through R3 and produce a voltage glitch on the switch side of R3. This voltage glitch can be detected and stretched to provide a properly timed $\overline{WR}$ signal for the AD7115.

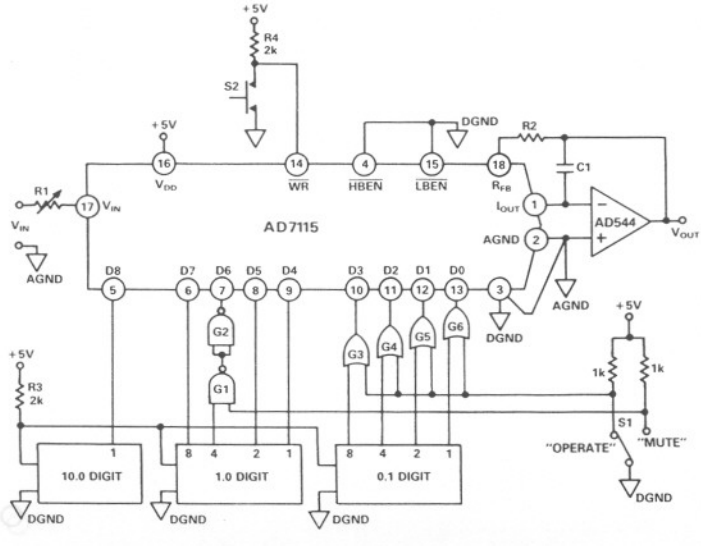


Figure 9. Thumbwheel Switch Attenuator

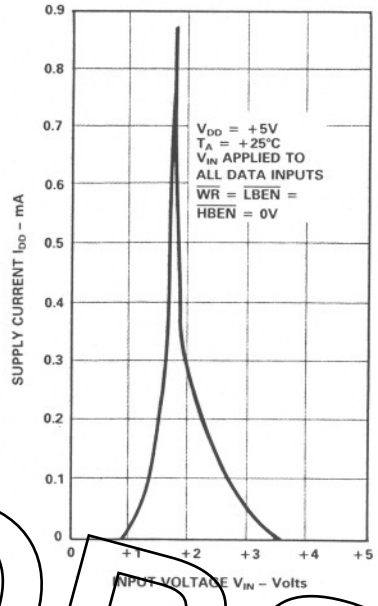


Figure 10. Typical Supply Current vs. Logic Input Level

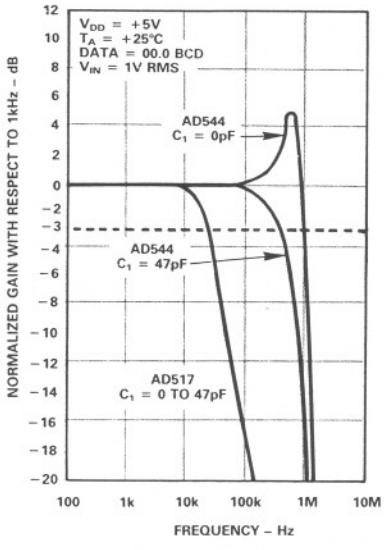


Figure 11. Frequency Response with AD544 and AD517 Amplifiers

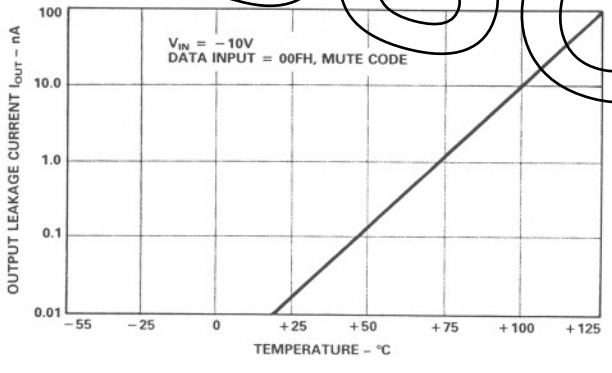


Figure 12. Typical Output Leakage Current vs. Temperature

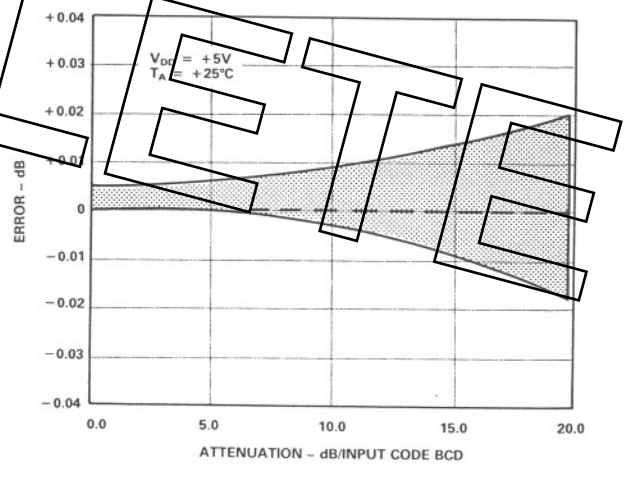


Figure 13. Typical Attenuation Error vs. Attenuation/Input Code

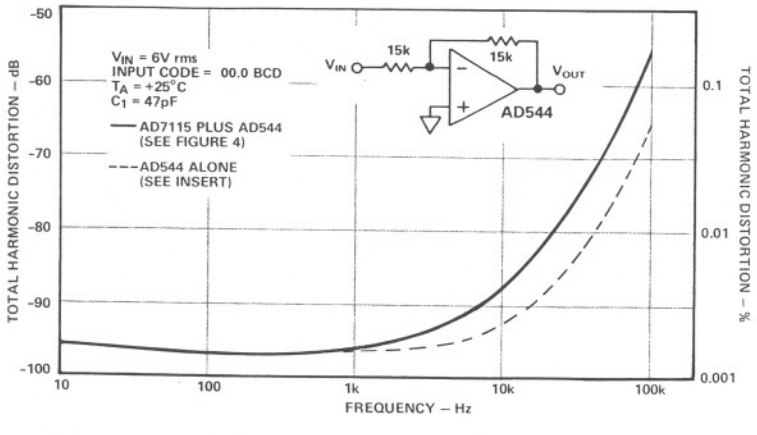


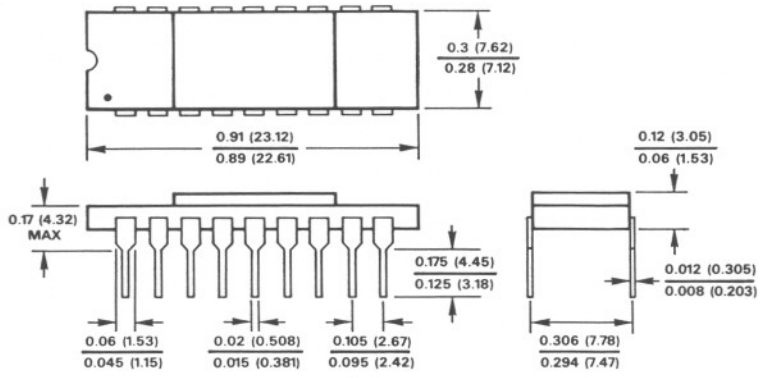
Figure 14. Typical Distortion vs. Frequency Using AD544 Amplifier

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

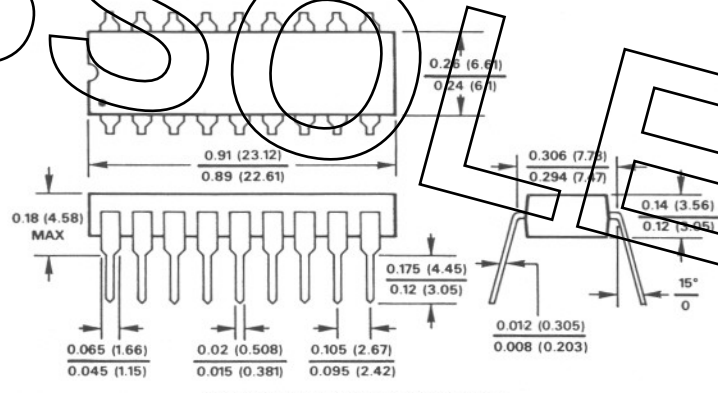
Dimensions shown in inches and (mm).

18-PIN CERAMIC DIP (SUFFIX D)



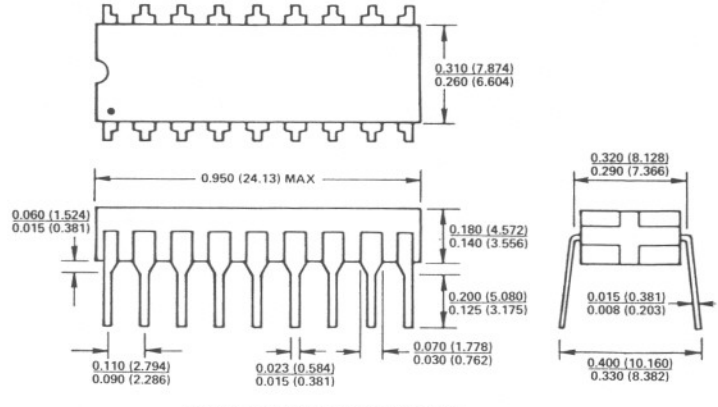
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS WILL BE EITHER GOLD OR TIN PLATED
IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

18-PIN PLASTIC DIP (SUFFIX N)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

18-PIN CERDIP (SUFFIX Q)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH

C728–9–7/82

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