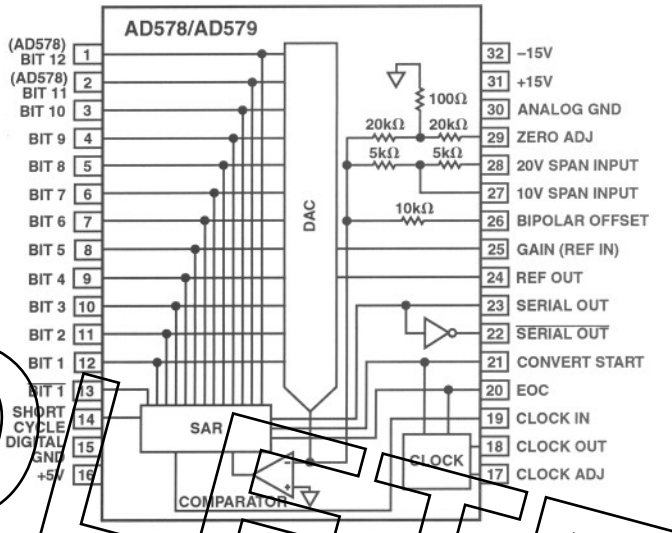
Very Fast, Complete 10- or 12-Bit A/D Converters

AD578/AD579

FEATURES

- Complete 12-Bit ADC with Reference and Clock
- Fast Conversion: 3 μs Max
- Buried Zener Reference for Long-Term Stability and Low Gain TC: ±30 ppm/°C Max (AD578)
  ±40 ppm/°C Max (AD579)
- Max Nonlinearity: <±0.012%
- No Missing Codes over Temperature
- Low Power: 555 mW (AD578); 775 mW (AD579)
- Available to MIL-STD-883
- Positive-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- Precision 10 V Reference for External Applications
- Adjustable Internal Clock
- Z Models for ±12 V Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD578 and AD579 are high speed 12-bit and 10-bit successive approximation ADCs that include an internal clock, reference, and comparator. Their hybrid design utilizes MSI digital and linear ICs in conjunction with a 12-bit or 10-bit monolithic, monotonic DAC to provide superior performance and versatility with IC size, price, and reliability.

Important performance characteristics of the AD578 include ±1/2 LSB_{12} linearity error maximum at +25°C, maximum gain temperature coefficient of ±30 ppm/°C, and maximum conversion time of 3 μs at a typical power dissipation of 555 mW. The 10-bit AD579 provides ±1/2 LSB_{10} maximum linearity error at 1.8 μs maximum and 775 mW typical P_D.

Both the AD578 and AD579 include scaling resistors that provide analog input signal ranges of ±5 V, ±10 V, and 0 V to +10 V. Both are contained in 32-lead ceramic side-brazed DIP packages and are available with MIL-STD-883 Class B processing.

The serial output function is no longer supported on this product after date code 9623.

PRODUCT HIGHLIGHTS

1. Both the AD578 and AD579 are complete ADCs. No external components are required to perform a conversion.
2. The fast conversion rates—3 μs for the AD578 and 1.8 μs for the AD579—make them ideal candidates for high speed data acquisition systems requiring high throughput.
3. The internal buried Zener reference is laser trimmed to high initial accuracy and low TC and is available externally.
4. Precision thin-film scaling resistors on the DAC provide for excellent thermal tracking.
5. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolution.

REV. C

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AD578/AD579—SPECIFICATIONS (Typical @ 25°C, ±15 V and +5 V, unless otherwise noted.)

Parameter	AD578J	AD578K	AD578L
RESOLUTION	12 Bits	12 Bits	12 Bits
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±5.0 V, ±10 V	±5.0 V, ±10 V	±5.0 V, ±10 V
Unipolar	0 V to +10 V, 0 V to +20 V	0 V to +10 V, 0 V to +20 V	0 V to +10 V, 0 V to +20 V
Input Impedance			
0 V to +10 V, ±5 V	5 kΩ	5 kΩ	5 kΩ
±10 V, 0 V to +20 V	10 kΩ	10 kΩ	10 kΩ
DIGITAL INPUTS			
Convert Command[1]	1 LSTTL Load	1 LSTTL Load	1 LSTTL Load
Clock Input	1 LSTTL Load	1 LSTTL Load	1 LSTTL Load
TRANSFER CHARACTERISTICS			
Gain Error[2, 3]	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max
Unipolar Offset[3]	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max
Bipolar Error[3, 4]	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max
Linearity Error, 25°C	±1/2 LSB max	±1/2 LSB max	±1/2 LSB max
T_{MIN} to T_{MAX}	±3/4 LSB	±3/4 LSB	±3/4 LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)			
25°C	12 Bits	12 Bits	12 Bits
T_{MIN} to T_{MAX}	12 Bits	12 Bits	12 Bits
POWER SUPPLY SENSITIVITY			
+15 V ± 10%	0.005%/%ΔV_S max	0.005%/%ΔV_S max	0.005%/%ΔV_S max
–15 V ± 10%	0.005%/%ΔV_S max	0.005%/%ΔV_S max	0.005%/%ΔV_S max
+5 V ± 10%	0.005%/%ΔV_S max	0.005%/%ΔV_S max	0.005%/%ΔV_S max
TEMPERATURE COEFFICIENTS			
Gain	±15 ppm/°C typ	±15 ppm/°C typ	±15 ppm/°C typ
	±30 ppm/°C max	±30 ppm/°C max	±30 ppm/°C max
Unipolar Offset	±3 ppm/°C typ	±3 ppm/°C typ	±3 ppm/°C typ
	±10 ppm/°C max	±10 ppm/°C max	±10 ppm/°C max
Bipolar Offset	±8 ppm/°C typ	±8 ppm/°C typ	±8 ppm/°C typ
	±20 ppm/°C max	±20 ppm/°C max	±20 ppm/°C max
Differential Linearity	±2 ppm/°C typ	±2 ppm/°C typ	±2 ppm/°C typ
CONVERSION TIME[5, 6, 7] (max)	6.0 µs	4.5 µs	3 µs
PARALLEL OUTPUTS			
Unipolar Code	Binary	Binary	Binary
Bipolar Code	Offset Binary/Twos Complement	Offset Binary/Twos Complement	Offset Binary/Twos Complement
Output Drive	2 LSTTL Loads	2 LSTTL Loads	2 LSTTL Loads
SERIAL OUTPUTS (NRZ FORMAT)			
Unipolar Code	Binary/Complementary Binary	Binary/Complementary Binary	Binary/Complementary Binary
Bipolar Code	Offset Binary/Comp. Offset Binary	Offset Binary/Comp. Offset Binary	Offset Binary/Comp. Offset Binary
Output Drive	2 LSTTL Loads	2 LSTTL Loads	2 LSTTL Loads
END OF CONVERSION (EOC)	Logic 1 During Conversion	Logic 1 During Conversion	Logic 1 During Conversion
Output Drive	8 LSTTL Loads	8 LSTTL Loads	8 LSTTL Loads
INTERNAL CLOCK[7]			
Output Drive	2 LSTTL Loads	2 LSTTL Loads	2 LSTTL Loads
INTERNAL REFERENCE			
Voltage	10.000 ± 100 mV	10.000 ± 100 mV	10.000 ± 100 mV
Drift	±12 ppm/°C, ±20 ppm/°C max	±12 ppm/°C, ±20 ppm/°C max	±12 ppm/°C, ±20 ppm/°C max
External Current	±1 mA max	±1 mA max	±1 mA max
POWER SUPPLY REQUIREMENTS[8]			
Range for Rated Accuracy	+4.75 to +5.25 and ±13.5 to ±16.5	+4.75 to +5.25 and ±13.5 to ±16.5	+4.75 to +5.25 and ±13.5 to ±16.5
Supply Current +15 V	5 mA typ, 8 mA max	5 mA typ, 8 mA max	5 mA typ, 8 mA max
–15 V	22 mA typ, 35 mA max	22 mA typ, 35 mA max	22 mA typ, 35 mA max
+5 V	30 mA typ, 40 mA max	30 mA typ, 40 mA max	30 mA typ, 40 mA max
Power Dissipation	555 mW typ	555 mW typ	555 mW typ
TEMPERATURE RANGE			
Operating	0°C to +70°C	0°C to +70°C	0°C to +70°C
Storage	–65°C to +150°C	–65°C to +150°C	–65°C to +150°C

See Page 3 for notes.

Parameter	AD578SD[9]	AD578TD[9]
RESOLUTION	12 Bits	12 Bits
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±5.0 V, ±10 V	±5.0 V, ±10 V
Unipolar	0 V to +10 V, 0 V to +20 V	0 V to +10 V, 0 V to +20 V
Input Impedance		
0 V to +10 V, ±5 V	5 kΩ	5 kΩ
±10 V, 0 V to +20 V	10 kΩ	10 kΩ
DIGITAL INPUTS		
Convert Command[1]	1 LSTTL Load	1 LSTTL Load
Clock Input	1 LSTTL Load	1 LSTTL Load
TRANSFER CHARACTERISTICS		
Gain Error[2, 3]	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max
Unipolar Offset[3]	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max
Bipolar Error[3, 4]	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max
Linearity Error, 25°C	±1/2 LSB max	±1/2 LSB max
T_{MIN} to T_{MAX}	±3/4 LSB max	±3/4 LSB max
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)		
25°C	12 Bits	12 Bits
T_{MIN} to T_{MAX}	12 Bits	12 Bits
POWER SUPPLY SENSITIVITY		
+15 V ± 10%	0.005%/%ΔV_S max	0.005%/%ΔV_S max
–15 V ± 10%	0.005%/%ΔV_S max	0.005%/%ΔV_S max
+5 V ± 10%	0.005%/%ΔV_S max	0.005%/%ΔV_S max
TEMPERATURE COEFFICIENTS		
Gain	±15 ppm/°C typ	±15 ppm/°C typ
	±50 ppm/°C max	±30 ppm/°C max
Unipolar Offset	±3 ppm/°C typ	±3 ppm/°C typ
	±15 ppm/°C max	±10 ppm/°C max
Bipolar Offset	±8 ppm/°C typ	±8 ppm/°C typ
	±25 ppm/°C max	±20 ppm/°C max
Differential Linearity	±2 ppm/°C typ	±2 ppm/°C typ
CONVERSION TIME[5, 6, 7] (max)	6.0 µs	4.5 µs
PARALLEL OUTPUTS		
Unipolar Code	Binary	Binary
Bipolar Code	Offset Binary/Twos Complement	Offset Binary/Twos Complement
Output Drive	2 LSTTL Loads	2 LSTTL Loads
SERIAL OUTPUTS (NRZ FORMAT)		
Unipolar Code	Binary/Complementary Binary	Binary/Complementary Binary
Bipolar Code	Offset Binary/Comp. Offset Binary	Offset Binary/Comp. Offset Binary
Output Drive	2 LSTTL Loads	2 LSTTL Loads
END OF CONVERSION (EOC)	Logic 1 During Conversion	Logic 1 During Conversion
Output Drive	8 LSTTL Loads	8 LSTTL Loads
INTERNAL CLOCK[7]		
Output Drive	2 LSTTL Loads	2 LSTTL Loads
INTERNAL REFERENCE		
Voltage	10.000 ± 100 mV	10.000 ± 100 mV
Drift	±12 ppm/°C, ±20 ppm/°C max	±12 ppm/°C, ±20 ppm/°C max
External Current	±1 mA max	±1 mA max
POWER SUPPLY REQUIREMENTS[8]		
Range for Rated Accuracy	+4.75 to +5.25 and ±13.5 to ±16.5	+4.75 to +5.25 and ±13.5 to ±16.5
Supply Current +15 V	5 mA typ, 8 mA max	5 mA typ, 8 mA max
–15 V	22 mA typ, 35 mA max	22 mA typ, 35 mA max
+5 V	30 mA typ, 40 mA max	30 mA typ, 40 mA max
Power Dissipation	555 mW typ	555 mW typ
TEMPERATURE RANGE		
Operating	–55°C to +125°C	–55°C to +125°C
Storage	–65°C to +150°C	–65°C to +150°C

NOTES
[1]Positive pulse 200 ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.
[2]With 50 Ω, 1% fixed resistor in place of gain adjust potentiometer.
[3]Adjustable to 0.
[4]With 50 Ω, 1% resistor between REF OUT and BIPOLAR OFFSET (Pins 24 and 26).
[5]Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.
[6]Each grade is specified at the conversion speed shown.
[7]Externally adjustable by a resistor or capacitor (see Figure 6).
[8]For Z models, order AD578ZJ, AD578ZK, or AD578ZL (±11.6 V to ±16.5 V).
[9]Available to MIL-STD-883, Level B. See ADI Military Products Databook for detailed specifications.
Specifications subject to change without notice.

Parameter	AD579JN	AD579KN
RESOLUTION	10 Bits	10 Bits
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±5.0 V, ±10 V	±5.0 V, ±10 V
Unipolar	0 V to +10 V, 0 V to +20 V	0 V to +10 V, 0 V to +20 V
Input Impedance		
0 V to +10 V, ±5 V	5 kΩ (±20%)	5 kΩ (±20%)
±10 V, 0 V to +20 V	10 kΩ (±20%)	10 kΩ (±20%)
DIGITAL INPUTS		
Convert Command[1]	1 LSTTL Load	1 LSTTL Load
Clock Input	1 LSTTL Load	1 LSTTL Load
TRANSFER CHARACTERISTICS		
Gain Error[2, 3]	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max
Unipolar Offset[3]	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max
Bipolar Error[3, 4]	±0.1% FSR, ±0.25% FSR max	±0.1% FSR, ±0.25% FSR max
Linearity Error, 25°C	±1/2 LSB max	±1/2 LSB max
T_{MIN} to T_{MAX}	±3/4 LSB	±3/4 LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)		
25°C	10 Bits	10 Bits
T_{MIN} to T_{MAX}	10 Bits	10 Bits
POWER SUPPLY SENSITIVITY		
+15 V ± 10%	0.005%/%ΔV_S max	0.005%/%ΔV_S max
−15 V ± 10%	0.005%/%ΔV_S max	0.005%/%ΔV_S max
+5 V ± 10%	0.001%/%ΔV_S max	0.001%/%ΔV_S max
Z Versions		
+12 V ± 5%	0.007%/%ΔV_S max	0.007%/%ΔV_S max
−12 V ± 5%	0.007%/%ΔV_S max	0.007%/%ΔV_S max
TEMPERATURE COEFFICIENTS		
Gain	±25 ppm/°C typ	±25 ppm/°C typ
	±40 ppm/°C max	±40 ppm/°C max
Unipolar Offset	±5 ppm/°C typ	±5 ppm/°C typ
	±15 ppm/°C max	±15 ppm/°C max
Bipolar Offset	±8 ppm/°C typ	±8 ppm/°C typ
	±20 ppm/°C max	±20 ppm/°C max
Differential Linearity	±2 ppm/°C typ	±2 ppm/°C typ
CONVERSION TIME[5, 6] (max)	2.2 µs	1.8 µs
T_{MIN} to T_{MAX}	2.4 µs	2.0 µs
PARALLEL OUTPUTS		
Unipolar Code	Binary	Binary
Bipolar Code	Offset Binary/Twos Complement	Offset Binary/Twos Complement
Output Drive	2 LSTTL Loads	2 LSTTL Loads
SERIAL OUTPUTS (NRZ FORMAT)		
Unipolar Code	Binary/Complementary Binary	Binary/Complementary Binary
Bipolar Code	Offset Binary/Comp. Offset Binary	Offset Binary/Comp. Offset Binary
Output Drive	2 LSTTL Loads	2 LSTTL Loads
END OF CONVERSION (EOC)	Logic 1 During Conversion	Logic 1 During Conversion
Output Drive	8 LSTTL Loads	8 LSTTL Loads
INTERNAL CLOCK[7]		
Output Drive	2 LSTTL Loads	2 LSTTL Loads
INTERNAL REFERENCE		
Voltage	10.000 ± 100 mV typ	10.000 ± 100 mV typ
Temperature Coefficient	±15 ppm/°C	±15 ppm/°C
External Current	±1 mA max	±1 mA max
POWER SUPPLY REQUIREMENTS		
Range for Rated Accuracy	+4.75 to +5.25 and ±13.5 to ±16.5	+4.75 to +5.25 and ±13.5 to ±16.5
Z Models[8]	+4.75 to +5.25 and ±11.4 to ±16.5	+4.75 to +5.25 and ±11.4 to ±16.5
Supply Current +15 V	5 mA typ, 8 mA max	5 mA typ, 8 mA max
−15 V	22 mA typ, 35 mA max	22 mA typ, 35 mA max
+5 V	100 mA typ, 150 mA max	100 mA typ, 150 mA max
Power Dissipation	775 mW typ	775 mW typ
TEMPERATURE RANGE		
Operating	0°C to +70°C	0°C to +70°C
Storage	−65°C to +150°C	−65°C to +150°C

NOTES

[1]Positive pulse 200 ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.

[2]With 50 Ω, 1% fixed resistor in place of gain adjust potentiometer.

[3]Adjustable to zero.

[4]With 50 Ω, 1% resistor between REF OUT and BIPOLAR OFFSET (Pins 24 and 26).

[5]Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.

(Continued on page 5)

Parameter	AD579TD[9]
RESOLUTION	10 Bits
ANALOG INPUTS	
Voltage Ranges	
Bipolar	±5.0 V, ±10 V
Unipolar	0 V to +10 V, 0 V to +20 V
Input Impedance	
0 V to +10 V, ±5 V	5 kΩ (±20%)
±10 V, 0 V to +20 V	10 kΩ (±20%)
DIGITAL INPUTS	
Convert Command[1]	1 LSTTL Load
Clock Input	1 LSTTL Load
TRANSFER CHARACTERISTICS	
Gain Error[2, 3]	±0.1% FSR, ±0.25% FSR max
Unipolar Offset[3]	±0.1% FSR, ±0.25% FSR max
Bipolar Error[3, 4]	±0.1% FSR, ±0.25% FSR max
Linearity Error, 25°C	±1/2 LSB max
T_{MIN} to T_{MAX}	±3/4 LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)	
25°C	10 Bits
T_{MIN} to T_{MAX}	10 Bits
POWER SUPPLY SENSITIVITY	
+15 V ± 10%	0.005%/%ΔV_S max
–15 V ± 10%	0.005%/%ΔV_S max
+5 V ± 10%	0.001%/%ΔV_S max
Z Versions	
+12 V ± 5%	0.007%/%ΔV_S max
–12 V ± 5%	0.007%/%ΔV_S max
TEMPERATURE COEFFICIENTS	
Gain	±25 ppm/°C typ
	±40 ppm/°C max
Unipolar Offset	±5 ppm/°C typ
	±15 ppm/°C max
Bipolar Offset	±8 ppm/°C typ
	±20 ppm/°C max
Differential Linearity	±2 ppm/°C typ
CONVERSION TIME[5, 6] (max)	1.8 µs
T_{MIN} to T_{MAX}	2.0 µs
PARALLEL OUTPUTS	
Unipolar Code	Binary
Bipolar Code	Offset Binary/Twos Complement
Output Drive	2 LSTTL Loads
SERIAL OUTPUTS (NRZ FORMAT)	
Unipolar Code	Binary/Complementary Binary
Bipolar Code	Offset Binary/Comp. Offset Binary
Output Drive	2 LSTTL Loads
END OF CONVERSION (EOC)	Logic 1 During Conversion
Output Drive	8 LSTTL Loads
INTERNAL CLOCK[7]	
Output Drive	2 LSTTL Loads
INTERNAL REFERENCE	
Voltage	10.000 ± 100 mV typ
Temperature Coefficient	±15 ppm/°C
External Current	±1 mA max
POWER SUPPLY REQUIREMENTS	
Range for Rated Accuracy	+4.75 to +5.25 and ±13.5 to ±16.5
Z Models[8]	+4.75 to +5.25 and ±11.4 to ±16.5
Supply Current +15 V	5 mA typ, 8 mA max
–15 V	22 mA typ, 35 mA max
+5 V	100 mA typ, 150 mA max
Power Dissipation	775 mW typ
TEMPERATURE RANGE	
Operating	–55°C to +125°C
Storage	–65°C to +150°C

NOTES (continued)
[6]Each grade is specified at the conversion speed shown.
[7]Externally adjustable by a resistor or capacitor. See Figure 8 for appropriate connections.
[8]For Z models, order AD579ZJN, AD579ZKN, or AD579ZTD.
[9]Available to MIL-STD-883, Level B. See ADI Military Products Databook for detailed specifications.
Specifications subject to change without notice.

ORDERING GUIDE[1]

Model	Resolution	Conversion Speed	Temperature Range	Package Option[2]
AD578JN (JD)	12 Bits	6.0 µs	0°C to +70°C	DH-32B
AD578KN (KD)	12 Bits	4.5 µs	0°C to +70°C	DH-32B
AD578LN (LD)	12 Bits	3.0 µs	0°C to +70°C	DH-32B
AD578SD	12 Bits	6.0 µs	–55°C to +125°C	DH-32B
AD578TD	12 Bits	4.5 µs	–55°C to +125°C	DH-32B
AD578SD/883B	12 Bits	6.0 µs	–55°C to +125°C	DH-32B
AD578TD/883B	12 Bits	4.5 µs	–55°C to +125°C	DH-32B
AD579JN	10 Bits	2.2 µs	0°C to +70°C	DH-32B
AD579KN	10 Bits	1.8 µs	0°C to +70°C	DH-32B
AD579TD	10 Bits	1.8 µs	–55°C to +125°C	DH-32B
AD579TD/883B	10 Bits	1.8 µs	–55°C to +125°C	DH-32B

NOTES
[1]For ±12 V operation, Z Version, order AD578ZTD.
[2]DH = Side Brazed Ceramic DIP.

THEORY OF OPERATION

The AD578 is a complete pretrimmed 12-bit ADC that requires no external components to provide the successive approximation analog-to-digital conversion function. A block diagram of the AD578/AD579 is shown in Figure 1.

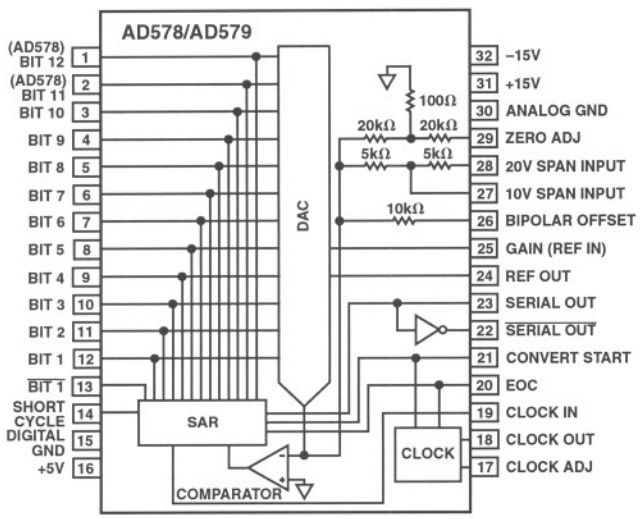
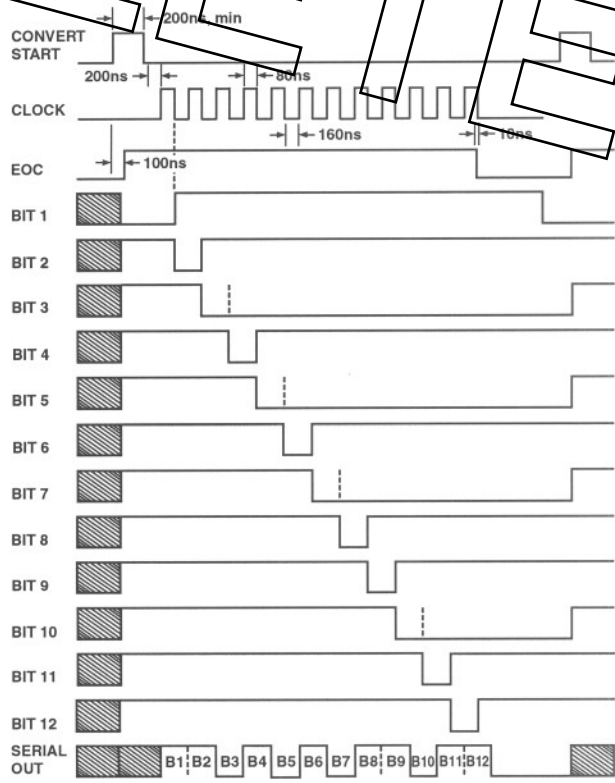


Figure 1. AD578/AD579 Functional Block Diagram and Pinout

When the control section is commanded to initiate a conversion, it enables the clock and resets the successive approximation register (SAR). The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section. The control section disables the clock and brings the output status flag low. The data bits are valid on the falling edge of the clock pulse starting with t_1 and ending with t_{12} (Figures 2a and 2b) and accurately represent the input signal to within ±1/2 LSB.



CLOCK
INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH MINIMUM PERIOD, T_{MIN} OF 100ns.

NOTE
THE RISING EDGE OF CONVERT START PULSE RESETS THE MSB TO ZERO, AND THE LSBs TO ONE. THE TRAILING EDGE INITIATES CONVERSION.

Figure 2a. AD578 Timing Diagram

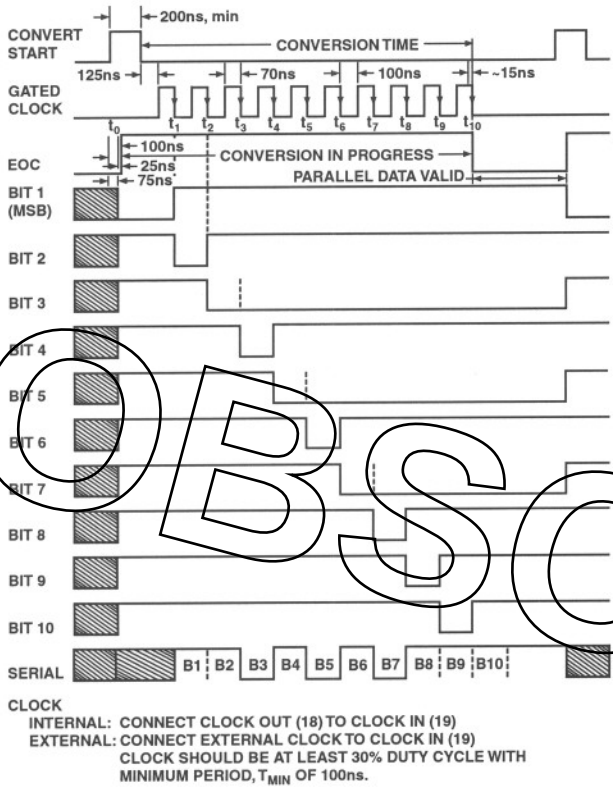


Figure 2b. AD579 Timing Diagram

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10 V ± 1.0%; it is buffered and can supply up to 1 mA to an external load in addition to the current required to drive the reference input resistor (0.5 mA) and bipolar offset resistor (1 mA). The thin-film application resistors are trimmed to match the full-scale output current of the DAC. Two 5 kΩ input scaling resistors allow either a 10 V or a 20 V span. The 10 kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 V reference for bipolar operation.

UNIPOLAR CALIBRATION

The AD578/AD579 are intended to have a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2 LSB.

If Pin 26 is connected to Pin 30, the unit will behave in this manner, within specifications. Refer to Table I, Table II, and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±25 mV of offset trim range.

The full-scale trim is done by applying a signal 1 1/2 LSB below the nominal full scale. Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 11111).

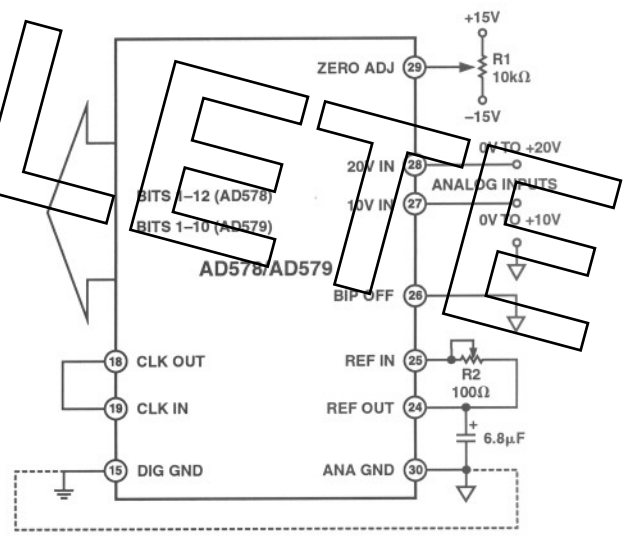


Figure 3. Unipolar Input Connections

Table I. AD578 Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

Analog Input—Volts (Center of Quantization Interval)				Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 V to +10 V Range	0 V to +20 V Range	–5 V to +5 V Range	–10 V to +10 V Range	B1 (MSB) B12 (LSB)
+9.9976	+19.9951	+4.9976	+9.9951	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+19.9902	+4.9952	+9.9902	1 1 1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0024	+10.0049	+0.0024	+0.0049	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0024	+0.0051	–4.9976	–9.9951	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	–5.0000	–10.0000	0 0 0 0 0 0 0 0 0 0 0 0

Table II. AD579 Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

Analog Input—Volts (Center of Quantization Interval)				Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 V to +10 V Range	0 V to +20 V Range	–5 V to +5 V Range	–10 V to +10 V Range	B1 (MSB) B12 (LSB)
+9.9902	+19.9804	+4.9902	+9.9804	1 1 1 1 1 1 1 1 1 1 1 1
+9.9804	+19.9609	+4.9804	+9.9609	1 1 1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0097	+10.0195	+0.0097	+0.0195	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0097	+0.0195	–4.9902	–9.9804	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	–5.0000	–10.0000	0 0 0 0 0 0 0 0 0 0 0 0

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, the 100 Ω trimmer shown can be replaced by a 50 Ω ± 1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). A signal 1 1/2 LSB below positive full scale is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

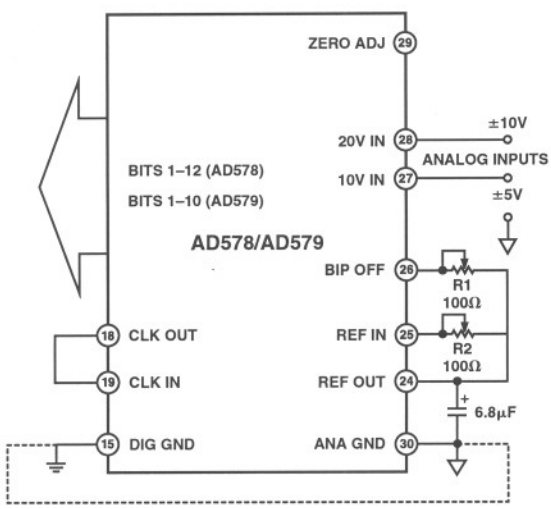


Figure 4. Bipolar Input Connections

LAYOUT CONSIDERATIONS

Many data acquisition components have two or more ground pins that are not connected together within the device. These grounds are usually referred to as the logic power return, analog common (analog power return), and analog signal ground. These grounds must be tied together at one point, usually at the system power supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD578 or AD579. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way, supply currents and logic-gate return currents are not summed into the same return path as analog signals, where they would cause measurement errors.

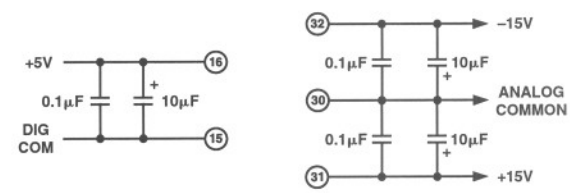


Figure 5. Basic Bypassing Practice

Each of the AD578 or AD579 supply terminals should be capacitively decoupled as close to the ADC as possible. A large value capacitor such as 10 µF in parallel with a 0.1 µF capacitor is usually sufficient. Analog supplies are bypassed to the analog power return pin and the logic supply is bypassed to the digital GND pin.

To minimize noise, the reference output (Pin 24) should be decoupled by a 6.8 µF capacitor to Pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 5.6 µs (AD578) or 4.8 µs (AD579). It can be adjusted for either faster or slower conversion rates. For faster conversions, connect the appropriate 1% resistor between Pins 17 and 18 and short Pin 18 to Pin 19 (see Figures 6, 7, and 8).

For slower conversions (AD578 only), connect a capacitor between Pins 15 and 17.

Note that the No Missing Code operation is not guaranteed when operating in this mode if a particular grade's conversion speed specification is exceeded.

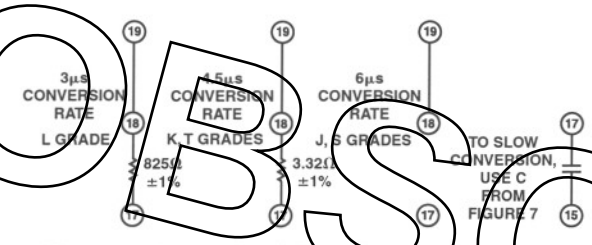


Figure 6. AD578 Clock Rate Control Connection

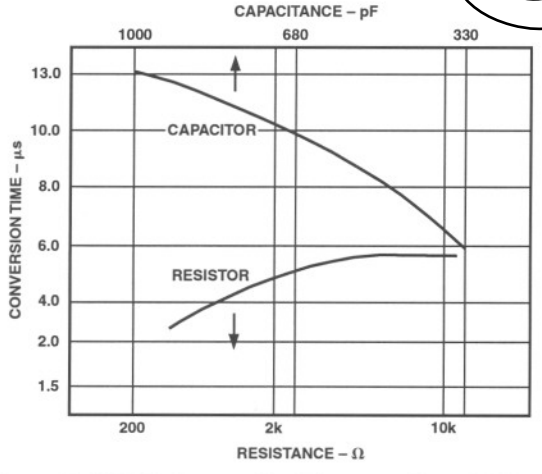


Figure 7. AD578 Conversion Times vs. R or C Values

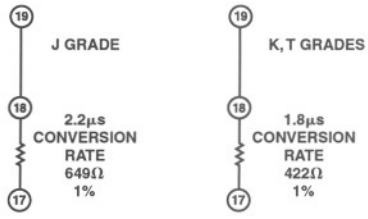


Figure 8. AD579 Clock Rate Control Connection

Short Cycle Input—A short cycle input, Pin 14, permits the timing cycle to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applications not requiring the full 10-bit (AD579) or 12-bit (AD578) resolution. Short cycle pin connections and associated conversion times are summarized in Tables III and IV.

Table III. AD578 Short Cycle Connections

For Resolution Bit	Connect Pin 14 to	Conversion Speed (µs)
12	Pin 16	3
10	Pin 2	2.5
8	Pin 4	2

Table IV. AD579 Short Cycle Connections

For Resolution Bit	Connect Pin 14 to	Conversion Speed (µs)
10	Pin 2	1.8
8	Pin 4	1.5

External Clock—An external clock may be connected directly to the clock input, Pin 19. When operating in this mode, the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle. A positive-going pulse width of 100 ns to 200 ns will provide a continuous string of conversions that start on the first rising edge of the external clock after the EOC output has gone low.

External Buffer Amplifier—In applications where the AD578 or AD579 is to be driven from high impedance sources or directly from an analog multiplexer, a fast slewing, wideband op amp like the AD711 should be used (see Figure 9).

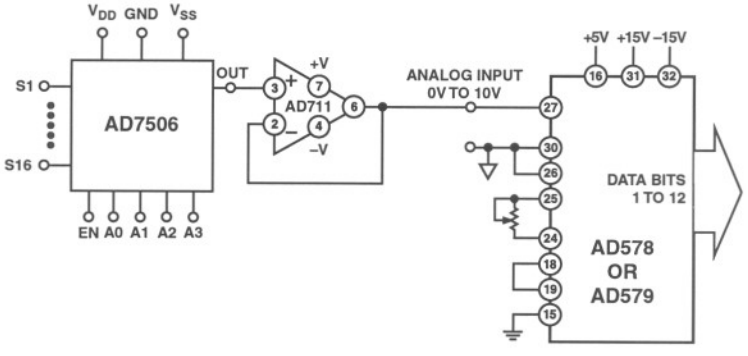
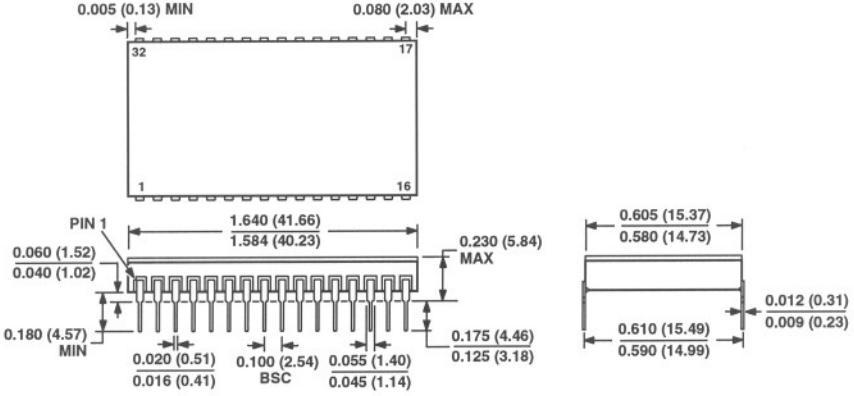


Figure 9. Input Buffer

OUTLINE DIMENSIONS

32-Lead Side Brazed Ceramic DIP [SBDIP/H]
(DH-32B)

Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
10/03—Data Sheet changed from REV. B to REV. C	
Change analog-to-digital converter to ADC	Universal
Replaced OUTLINE DIMENSIONS	10
3/03—Data Sheet changed from REV. A to REV. B	
Added text to GENERAL DESCRIPTION	1
Reformatted SPECIFICATIONS	2
Renumbered Figures 6–9	9
Updated OUTLINE DIMENSIONS	10