1214GN-1200VG

1200 Watts • 50 Volts • 300us, 10%
1200-1400 MHz L-Band Radar

GENERAL DESCRIPTION

The 1214GN-1200VG is an internally matched, COMMON SOURCE, class AB GaN on SiC HEMT transistor capable of providing over 16.3dB gain, 53% drain efficiency, 1200 Watts of pulsed RF output power at 300µs pulse width, 10% duty factor across the 1200 to 1400 MHz band. The transistor has internal pre-match for optimal performance. This transistor is ideal for use in L-band pulsed primary radar output stages. It utilizes gold metallization and eutectic attach to provide highest reliability and superior ruggedness.

ABSOLUTE MAXIMUM RATINGS

Maximum Power Dissipation

Device Dissipation @ 25°C 2500 W

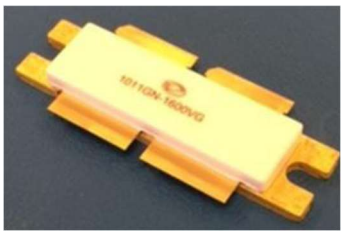
Maximum Voltage and Current

Drain-Source Voltage (V_{DSS}) 65 V
Gate-Source Voltage (V_{GS}) -8 to +0 V

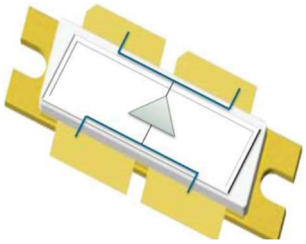
Maximum Temperatures

Storage Temperature (T_{STG}) -55 to +150°C
Operating Junction Temperature +200°C

CASE OUTLINE
55_Q11A
Common Source



0.400"X1.610"



Single Ended

ELECTRICAL CHARACTERISTICS @ 25°C

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Units
P_{OUT}	Output Power	Pout=1200W, Freq=1200, 1300, 1400 MHz	1200			W
G_P	Power Gain	Pout=1200W, Freq=1200, 1300, 1400 MHz	16.3	17.0		dB
η_P	Drain Efficiency	Pout=1200W, Freq=1200, 1300, 1400 MHz	54	60		%
Dr	Droop	Pout=1200W, Freq=1200, 1300, 1400 MHz			0.8	dB
VSWR-T	Load Mismatch Tolerance	Pout=1200W, Freq=1400 MHz			3:1	
Θ_{JC}	Thermal Resistance	Pulse Width=170uS, Duty=10%			0.07	°C/W

- **Constant Gate Bias Condition: Vdd=+50V, I_{DQ}=280mA average current (V_{GS}= -2.0 ~ -4.5V)**

FUNCTIONAL CHARACTERISTICS @ 25°C

$I_{D(Off)}$	Drain leakage current	V_{GS} = -8V, V_D = 150V			24	mA
$I_{G(Off)}$	Gate leakage current	V_{GS} = -8V, V_D = 0V			12	mA

Export Classification: EAR-99

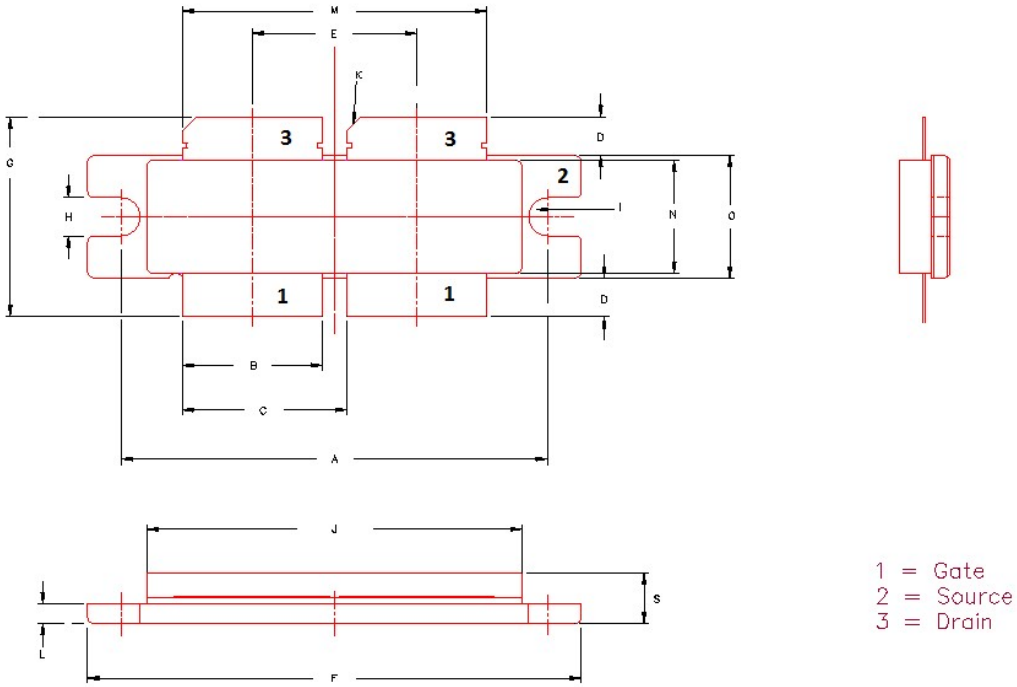
TYPICAL BROAD BAND PERFORMACE DATA

1214GN-1200VG VDD = 50V IDQ = 400mA VGS = -3.21V Pulsing: 300µS - 10%

Frequency	P_{IN} (dBm)	P_{IN} (W)	P_{OUT} (dBm)	P_{OUT} (W)	G_P (dB)	IRL (dB)	η_D (%)	Droop (dB)
1200 MHz	44.5	28.2	61.1	1288	16.6	-9.8	53%	0.5
1300 MHz	43.5	22.4	61.18	1312	17.68	-9.9	58%	0.4
1400 MHz	43.5	22.4	61.11	1291	17.61	--12	65%	0.25

Text Fixture will be available on request.

55-Q11A PACKAGE DRAWING
mm (inches)



1 = Gate
2 = Source
3 = Drain

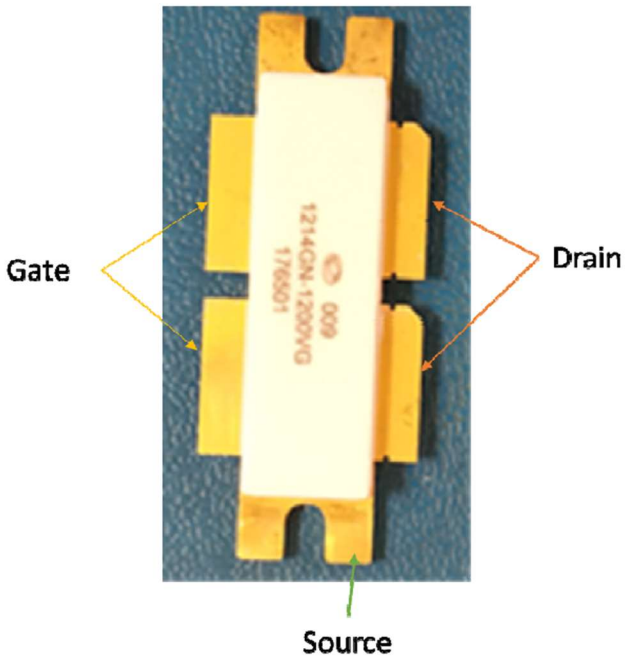
Dimension	Min (mil)	Min (mm)	Max (mil)	Max (mm)
A	1395	35.43	1405	35.68
B	450	11.43	470	11.94
C	530	13.46	550	13.97
D	117	2.97	137	3.48
E	535	13.59	545	13.84
F	1610	40.89	1630	41.40
G	644	16.36	664	16.86
H	122	3.10	128	3.25
I	R=.0625		R=1.59	
J	1218	30.93	1242	31.55
K	47 x 45°±5°		1.19x 4°±5°	
L	63	1.60	65	1.65
M	990	25.15	1010	25.65
N	365	9.27	375	9.53
O	398	10.11	406	10.31
S	158	4.01	172	4.37

1214GN-1200VG Mounting Procedure and Tips

1. Background

The 1214GN-1200VG model used Q11A package with 8 GaN die configuration. This is a long package and only uses the package's two end "eared" sides to bolt down. Thus, it is possible that a less than ideal contact between flange bottom surface and heatsink slot surface can occur if careful attention is not made to the bolt down. Poor contact will cause transistor thermal and electrical ground defects and make the transistor easily prone to oscillation and low output power. Therefore, good flange and heatsink contact will be an important task during transistor mounting process.

2. Transistor Gate and source and drain photo



- Gate side has normal rectangular configuration.
- Drain side has small notch-cut at both sides and chamfer at upper right side.
- The Source is the flange to heatsink bolt down slot to form both a thermal path and electrical ground surface.
- The flange bottom concave specification is 0mil -1 mil, therefore slot surface flatness required +/-0.5 mil flatness. The maximum gap between flange and slot is 1.5 mills.

3. Transistor mounting location should be in the middle of TF.

- Transistor location should be in the middle of slot with two gate leads.
- The unit should be pushed to drain side.

4. Slot surface flatness requirement is +/- 0.5 mil or less that you can achieve at reasonable cost.

5. The gap between flange bottom surface and heatsink slot needs thermal compound to fill the gap. You should make sure no visible particles are left on the flange bottom and slot surface to avoid voiding and poor contact.

6. The clamp post that contact ear areas of package should be as smoothly flat asmechanic milling machine tolerance can achieve.

7. The 4-40 screw locking down the unit should apply force symmetrically on both sides. Use screwdriver with certain amount torque level set for both sides.

8. Tips to identify the non-perfect contact between flange and slot surfaces:

a. At 1.4GHz, you can easily identify non-perfect contact: when you apply Pin=24dbm or below input power, you can observe over 18dB gain. Therefore 1.4GHz RF test should be started first.
b. Ensure the return loss level did not move up with increasing input power level.
c. Observe if the gain jumps significantly when input power level increasing.

9. Remount the device to get best contact when non-perfect contact is identified. Move the deviceup and down several times slightly in the slot and repeat action item 3 and 7 until close to the specification and any supplied RF test data at 1.4GHz. Maximum gain should be at about Pin=36dbm at room temperature.

Bias Instruction for Constant Gate Bias

Before connection to sample DUT, please check if Vgs and VDS solder location have are not damaged. After Vgs and Vds power supply and RF in terminal and RF out terminal have been connected to DUT, please follow this procedure to turn on and off the device:

Turn ON procedure:

1. Set Vgs = -8V with current limit 200mA.
2. Use DMM to measure Vgs (input side of circuit) to make sure that Vgs = -8V
3. Slowly increase Vds (Drain voltage) from 0V to 50V & set limit current to 9.8A.
4. Slowly increase Vgs until Idq = 280mA (Vgs~=-3.061V)
5. Apply RF input power & increase to spec (Pin=44dBm)

Turn OFF instruction:

1. Slowly decrease RF input power to minimum level and turn off.
2. Reduce Vgs to -8V.
3. Slowly decrease Vdd from 50V to 0V and turn off.
4. After large storage capacitor has been discharged fully and ensure Vdd (drain voltage) is completely turned off (0 Volts, no current).
5. Disconnect Vdd from DUT
6. Turn off Vgs.

Example Test Data

Model:	1214GN-1200VG			pulse format	170us, 10%						
Date:	10/20/2020			work order	176501	SN	7				
Test by:	WS			Vd=50V	Idq=280mA		Vgs=-3.054V				
		TF6192		use new clamp 3							
10/20/2020				170us@10%		after seal					
S/NR7	Freq (MHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain	IA	RL(raw)	RTL(dB)	Eff (%)	Droop	Gmax
Vgs=-3.054V	1200	45.5	61.8	1514	16.3	5.436	35.5	-10	0.58	0.4	
Idq=276mA		45	61.58	1439	16.58	5.31	35.2	-9.8	0.56	0.4	17.88
3rd test		44.5	61.28	1343	16.78	5.133	34.2	-10.3	0.54	0.45	
		44	60.97	1250	16.97	4.965	34	-10	0.52	0.5	
		43	60.2	1047	17.2	4.564	32.7	-10.3	0.48	0.5	
		42	59.39	869	17.39	4.177	31.5	-10.5	0.43	0.5	
		39	56.67	465	17.67	3.123	28.3	-10.7	0.32	0.5	
		36	53.72	236	17.72	2.315	25.2	-10.8	0.22	0.3	
		33	50.55	114	17.55	1.683	22.7	-10.3	0.15	0.3	
		45	61.74	1493	16.74	5.103	36.5	-8.5	0.61	0.3	
		44.5	61.61	1449	17.11	5.063	35.9	-8.6	0.59	0.3	
		44	61.36	1368	17.36	4.927	35.2	-8.8	0.58	0.35	
Idq=283mA	1300	43.5	61.11	1291	17.61	4.79	34.5	-9	0.56	0.4	18.63
2nd test		43	60.8	1202	17.8	4.638	34	-9	0.54	0.4	
		42	60.12	1028	18.12	4.283	32.7	-9.3	0.50	0.45	
		41	59.26	843	18.26	3.9	31.8	-9.2	0.45	0.45	
		39	57.51	564	18.51	3.225	29.5	-9.5	0.37	0.45	
		36	54.63	290	18.63	2.398	27	-9	0.26	0.4	
		33	51.52	142	18.52	1.76	24	-9	0.18	0.3	
		45	61.38	1374	16.38	4.41	33	-12	0.65	0.2	
		44.5	61.16	1306	16.66	4.31	32.4	-12.1	0.63	0.25	
		44	60.95	1245	16.95	4.208	31.8	-12.2	0.62	0.25	
Idq=283mA	1400	43.7	60.81	1205	17.11	4.144	31.5	-12.2	0.61	0.25	18.61
1st test		43	60.4	1096	17.4	3.952	30.8	-12.2	0.58	0.25	
		42	59.74	942	17.74	3.67	29.9	-12.1	0.54	0.3	
		40.5	58.57	719	18.07	3.221	28.6	-11.9	0.47	0.25	
		39	57.32	540	18.32	2.8	27.4	-11.6	0.41	0.25	
		36	54.45	279	18.45	2.077	24.9	-11.1	0.29	0.2	
		33	51.4	138	18.4	1.468	21.7	-11.3	0.21	0.1	

Proper Cooling Considerations

Below is a photo of a sample test fixture circuit with the fan cooling system, please monitor flange temperature closely. A water cooling system for can be used for best RF performance and long-life operation. The suggestions for fan cooling during an RF test are:

1. The fan should be the highest power that is available in the lab.
2. The fan's wind channel should be aimed to heatsink fin area like the photo1.
3. During RF full power test, it should not be over 2 minutes at full power level.
4. Between different frequencies tests, wait 3-4 minutes and let Idq decrease back to around 280mA level after you RF power is turned off and then change to another test frequency.

Test Fixture Photo

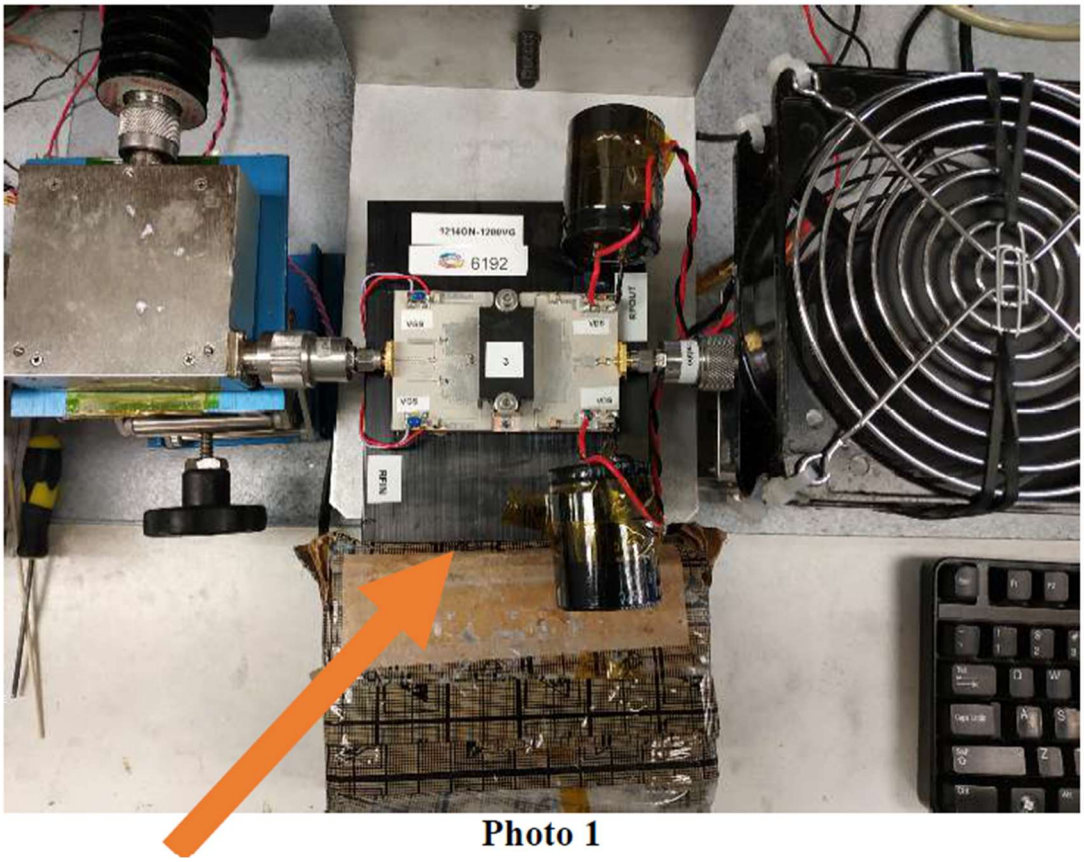
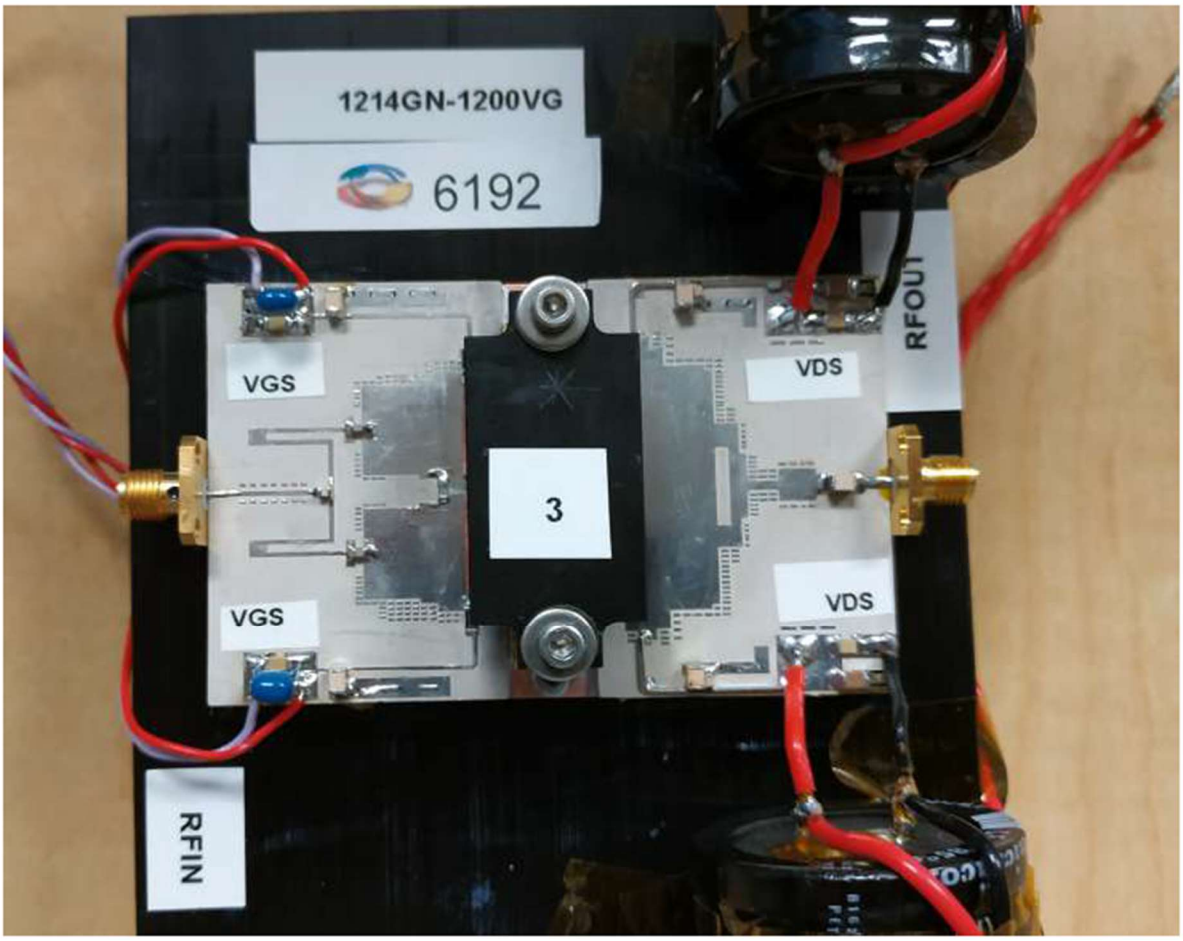


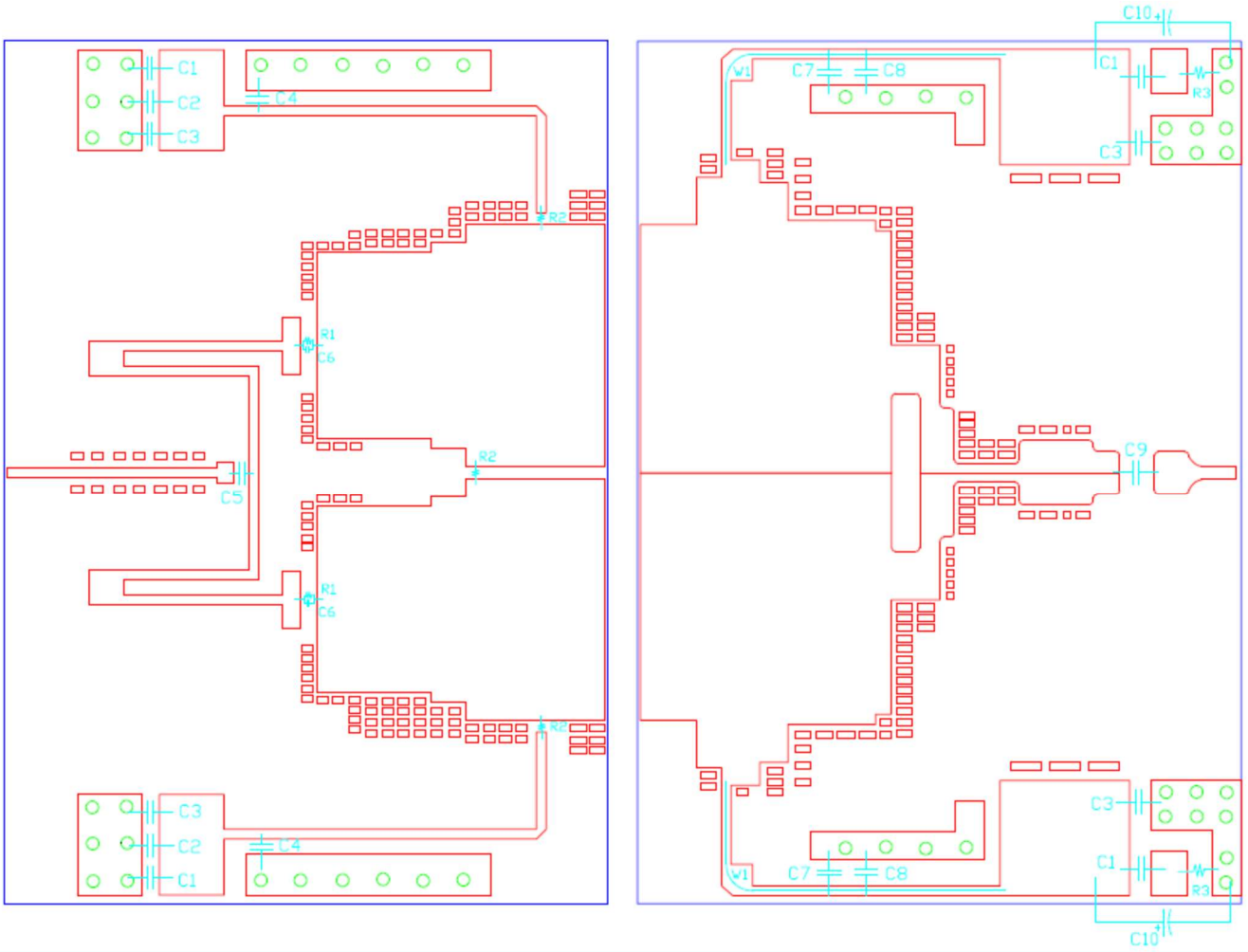
Photo 1

The fan's wind channel needs to be focused on the heatsink fins to make best air flow to carry maximum heat away. The fan required will be high speed and larger size (see example below).



TF 6192 detailed photo

Test Circuit and BOM



COMPONENTS LIST (1214GN-1200VG-W12-w2:

1) C1 (QTY=4): 0.1uF Size 200B ATC Chip Cap
2) C2 (QTY=2): 2.2uF Tantalum Cap
3) C3 (QTY=4): 1000pF Size 1206 Chip Cap, 200V
4) C4 (QTY=4): 100pF Size 100B ATC Chip Cap
5) C5 (QTY=1): 100pF Size 800A ATC Chip Cap
6) C6 (QTY=2): 18uF Size 600S ATC Chip Cap
7) C7 (QTY=2): 150pF Size 100B ATC Chip Cap
8) C8 (QTY=2): 33pF Size 800A ATC Chip Cap
9) C9 (QTY=1): 180pF Size 800B ATC Chip Cap
10) C10 (QTY=2): 1200uF, 63V Electrolytic Cap
11) R1 (QTY=2): 604 Ohm Size 0805 Chip Resistor
12) R2 (QTY=3): 20 Ohm Size 1206 Chip Resistor
13) R3 (QTY=2): 2.2 Ohm Size 1206 Chip Resistor
14) W1 (QTY=2): 22 AWG Cu Wire soldered on RF Choke

NOTE: C6 Caps are soldered directly on top of the R1 Resistors (2 places)

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