# MP3425

## 3A, 55V Boost Converter with Programmable Switching Frequency and UVLO

The Future of Analog IC Technology

## DESCRIPTION

The MP3425 is a current mode step-up converter with a 3.5A, 90mΩ internal switch to provide a highly efficient regulator with fast response. The MP3425 features a programmed frequency up to 2MHz allowing for easy filtering and low noise. An external compensation pin gives the user flexibility in setting loop dynamics, and operates with small, low-ESR ceramic output capacitors. Soft-start results in small inrush current and can be programmed with an external capacitor. The MP3425 operates from an input voltage as low as 3.1V and can generate 48V at up to 350mA from a 12V supply.

The MP3425 includes under-voltage lockout, current limiting and thermal overload protection to prevent damage in the event of an output overload. The MP3425 is available in a low profile 14-pin 3x4mm QFN package with exposed pad.

## FEATURES

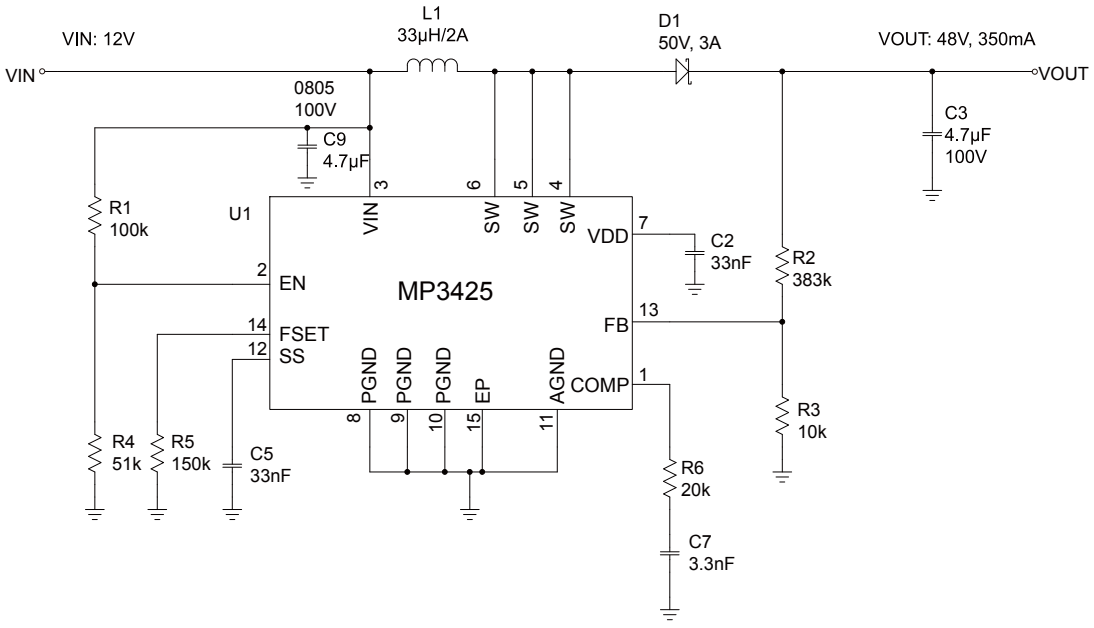
- 3.5A, 90mΩ, 55V Power MOSFET
- Uses Tiny Capacitors and Inductors
- Wide input range: 3.1V to 22V
- Output Voltage as High as 55V
- Programmable Fsw: 300kHz – 2 MHz
- Programmable UVLO, Soft-Start, UVLO Hysteresis
- Micropower shutdown <1μA
- Thermal Shutdown 160 °C
- Available in 14-Pin 3x4mm QFN Package

## APPLICATIONS

- Telecom – Power Supply
- Audio - Microphone and Tuner Bias
- Automotive



## TYPICAL APPLICATION

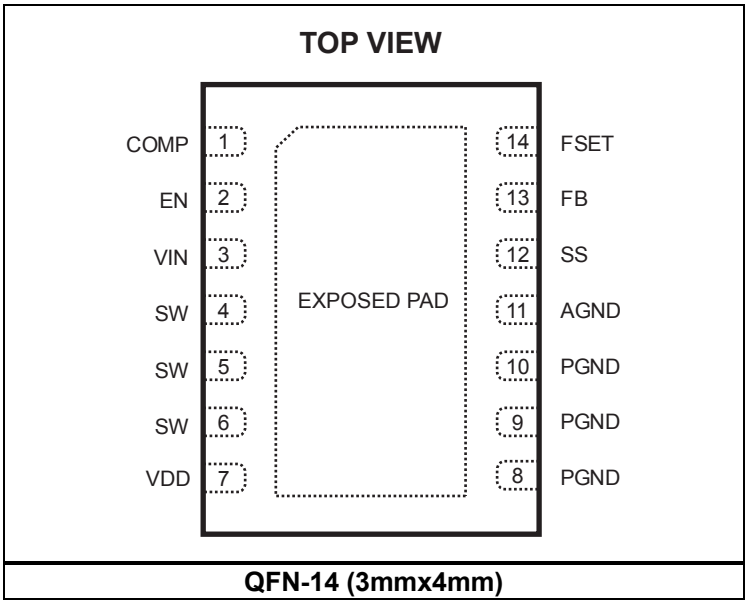


## ORDERING INFORMATION

| Part Number* | Package | Top Marking | Free Air Temperature ($T_A$) |
|---|---|---|---|
| MP3425DL | QFN-14 (3mmx4mm) | 3425 | -40°C to +85°C |

* For Tape & Reel, add suffix –Z (e.g. MP3425DL–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP3425DL–LF–Z)

## PACKAGE REFERENCE




QFN-14 (3mmx4mm)

## ABSOLUTE MAXIMUM RATINGS (1)

SW .....-0.5V(-3V for 10ns) to +55V
IN .....-0.5V to +22V
All Other Pins.....-0.3V to +6.5V
Continuous Power Dissipation ($T_A$ = +25°C) (2)
QFN14 ..... 2.5W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

### *Recommended Operating Conditions* (3)

Supply Voltage $V_{IN}$ .....3.1V to 22V
Output Voltage $V_{OUT}$.....3.1V to 55V
Operating Junct. Temp ($T_J$)..... - 40°C to +125°C

| *Thermal Resistance* | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| QFN-14 (3mmx4mm) | 50 | 12 | °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$(MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = $V_{EN}$ = 5V, $T_A$ = +25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Operating Input Voltage | $V_{IN}$ | | 3.1 | | 22 | V |
| Undervoltage Lockout | | $V_{IN}$ Rising | 2.8 | | 3.1 | V |
| Undervoltage Lockout Hysteresis | | | | 250 | | mV |
| VDD Voltage Gate drive Voltage supply | $V_{VDD}$ | C = 10nF | | | 6 | V |
| Supply Current (Shutdown) | | $V_{EN}$ = 0V | | | 1 | μA |
| Supply Current (Quiescent) | | $V_{FB}$ = 1.35V | | 650 | 900 | μA |
| Switching Frequency | | FSET = 84.5kΩ | 0.44 | 0.55 | 0.66 | MHz |
| Minimum Off time | | $V_{FB}$ = 0V | | 100 | | ns |
| Minimum On time | | $V_{FB}$ = 1.35V | | 100 | | ns |
| EN High Threshold | | $V_{EN}$ Rising (switching) | 1.45 | 1.5 | 1.55 | V |
| EN High Threshold | | $V_{EN}$ Rising (micro power) | | | 1.0 | V |
| EN Low Threshold | | | 0.5 | | | V |
| EN Input Bias Current | | $V_{EN}$ = 0V, 5V | | 0.1 | 1 | μA |
| UVLO Hysteresis current into EN pin | | 1.0 < EN < 1.4 | | 4 | | μA |
| Soft-Start Current | | | | 5 | | μA |
| FB Voltage | | | 1.200 | 1.225 | 1.250 | V |
| FB Input Bias Current | | | -200 | -100 | | nA |
| Error Amp Voltage Gain | $A_{VEA}$ | | | 300 | | V/V |
| Error Amp Transconductance ($\frac{\mu A}{V}$) | $G_{EA}$ | | | 160 | | μA/V |
| Error Amp Output Current | | | | 20 | | μA |
| GCS : I(SW) / Vcomp | $G_{CS}$ | | | 9 | | A/V |
| SW On-Resistance | $R_{ON}$ | | | 90 | | mΩ |
| SW Current Limit | | Duty Cycle = 0% | 3.5 | 5 | | A |
| Thermal Shutdown | | | | 160 | | °C |

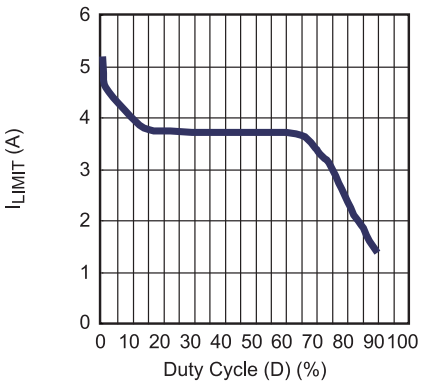
## PIN FUNCTIONS

| QFN14 Pin # | Name | Description |
|---|---|---|
| 1 | COMP | Compensation Pin. Connect a capacitor and resistor in series to Analog ground for loop stability. |
| 2 | EN | Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input source (through a 100kΩ pull-up resistor if $V_{IN}$ > 6V) for automatic startup. EN pin can also be used to program Vin UVLO. EN cannot be left floating. |
| 3 | VIN | Input Supply Pin. IN must be locally bypassed. |
| 4, 5, 6 | SW | Power Switch Output. SW is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW. |
| 7 | VDD | LDO Output |
| 8, 9, 10, Exposed Pad | PGND | The bottom exposed pad is the power ground. For best thermal resistance, solder the exposed pad to underlying copper backplane |
| 11 | AGND | Analog Ground. Connect to ground plane through exposed pad. |
| 12 | SS | Soft-Start Control Pin. Connect a soft-start capacitor to this pin. The soft-start capacitor is charged with a constant current of 5μA. Leave SS disconnected if the soft-start is not used. |
| 13 | FB | Feedback Input. Reference voltage is 1.225V. Connect a resistor divider this pin. |
| 14 | FSET | Frequency Programming Pin. Connect a resistor from this pin to AGND. FSET pin voltage is internally regulated to 0.5V. The current flowing out of this pin linearly sets the operation frequency. |
| 15 | EP | Exposed Pad. The bottom exposed pad is the power ground. For best thermal resistance, solder the exposed pad to underlying cooper backplane. |

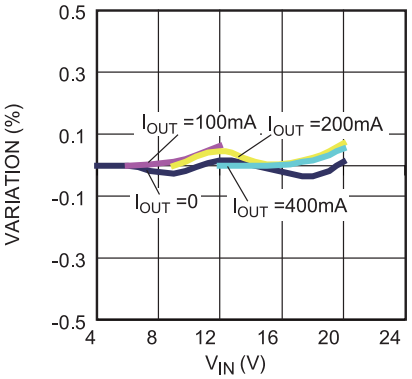
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$=12V, $V_{OUT}$=48V, L=33µH, $C_{OUT}$=4.7µF, $f_{SW}$=300kHz, $T_A$=+25°C, unless otherwise noted.**

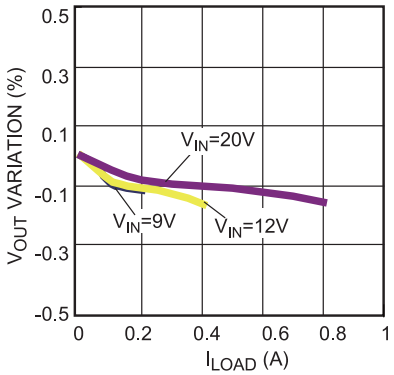
### $I_{LIMIT}$ (A) vs. Duty Cycle (D)



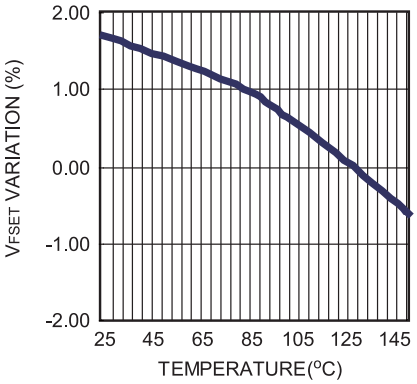

### Line Regulation



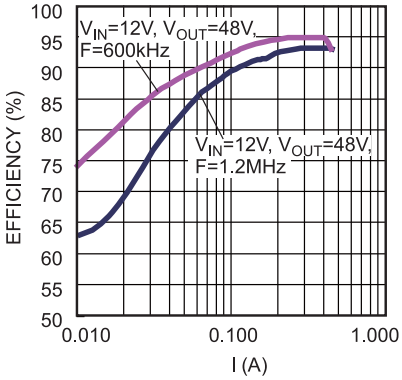

### Load Regulation



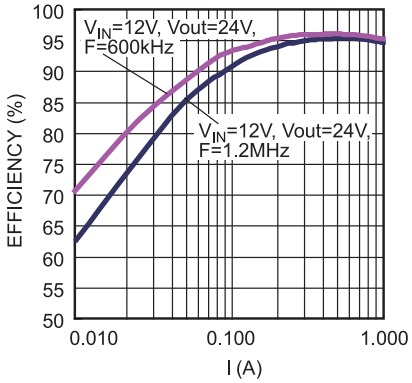

### $V_{FSET}$ vs. Temperature (C)



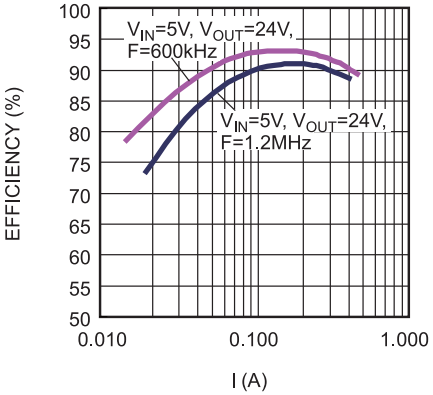

### Efficiency



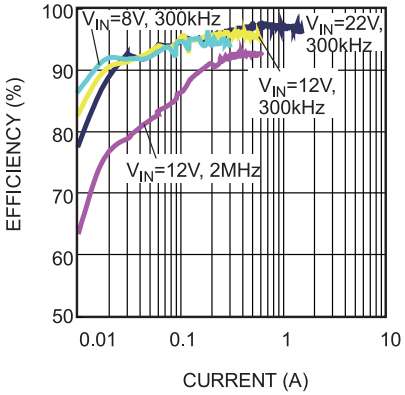

### Efficiency




### Efficiency



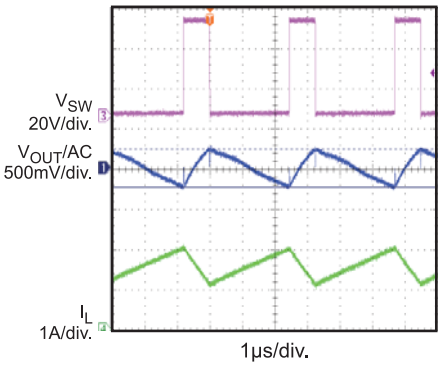

### Efficiency



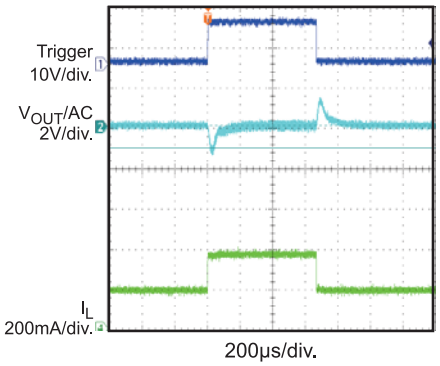
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$=12V, $V_{OUT}$=48V, L=33µH, $C_{OUT}$=4.7µF, $f_{SW}$=300kHz, $T_A$=+25°C, unless otherwise noted.**

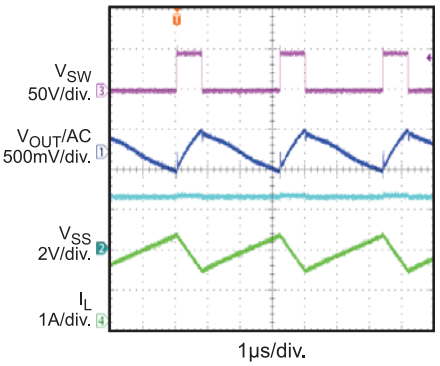
### $V_{OUT}$ Ripple
$V_{IN}$ = 12V, $V_{OUT}$ = 48V,
$I_{OUT}$ = 400mA



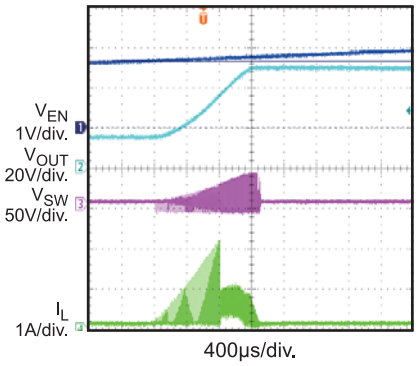

### Transient Response
$V_{IN}$ = 12V, $V_{OUT}$ = 48V,
200mA-400mA Step



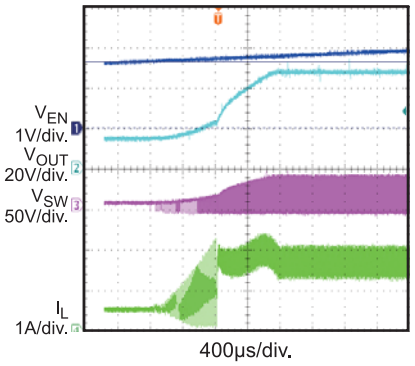

### 25°C–$V_{OUT}$,$V_{SS}$,$V_{SW}$, $I_L$ No/Full Load
$V_{IN}$ = 12V, Load=400mA



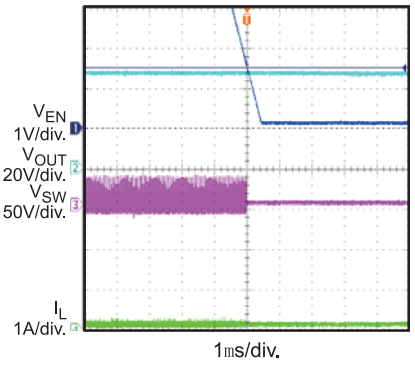

### EN Start-Up
$V_{IN}$ = 12V, Load=0A



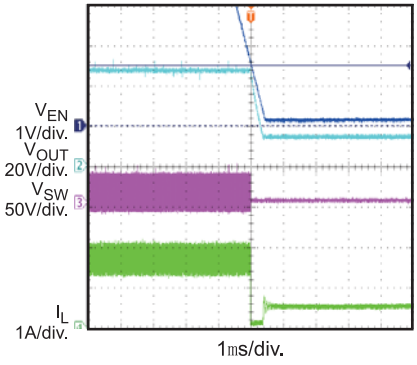

### EN Start-Up
$V_{IN}$ = 12V, Load=400mA



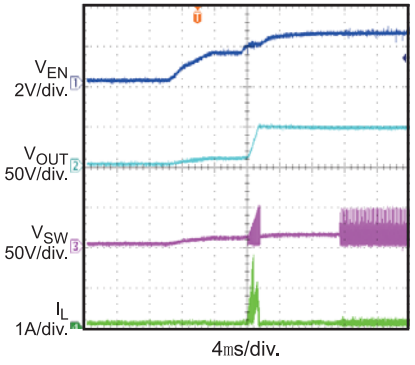

### EN Shutdown
$V_{IN}$ = 12V, Load=0A



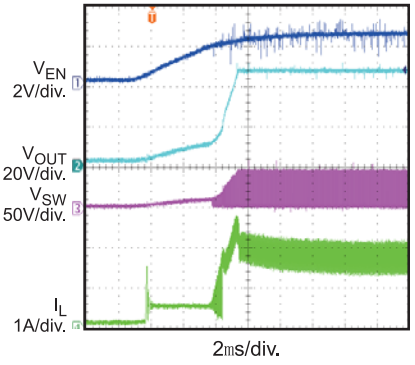

### EN Shutdown
$V_{IN}$ = 12V, Load=400mA




### $V_{IN}$ Start-Up
$V_{IN}$ = 12V, Load=0A



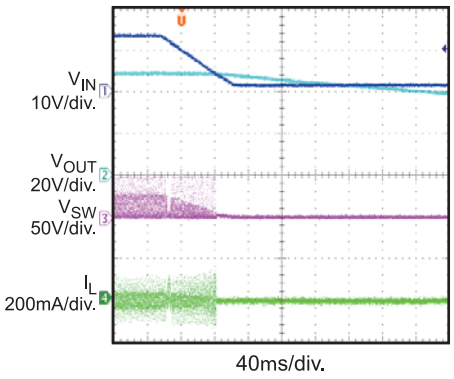

### $V_{IN}$ Start-Up
$V_{IN}$ = 12V, Load=400mA



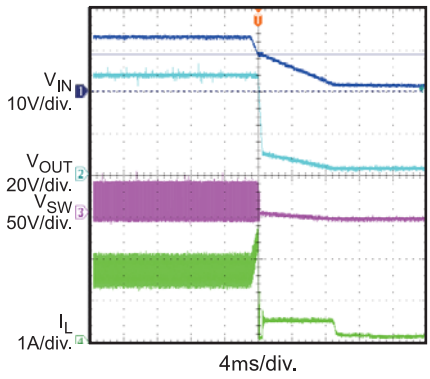
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$=12V, $V_{OUT}$=48V, L=33µH, $C_{OUT}$=4.7µF, $f_{SW}$=300kHz, $T_A$=+25°C, unless otherwise noted.**

**Vin Shutdown**
$V_{IN}$ = 12V, Load = 0A




**Vin Shutdown**
$V_{IN}$ = 12V, Load = 400mA



## BLOCK DIAGRAM

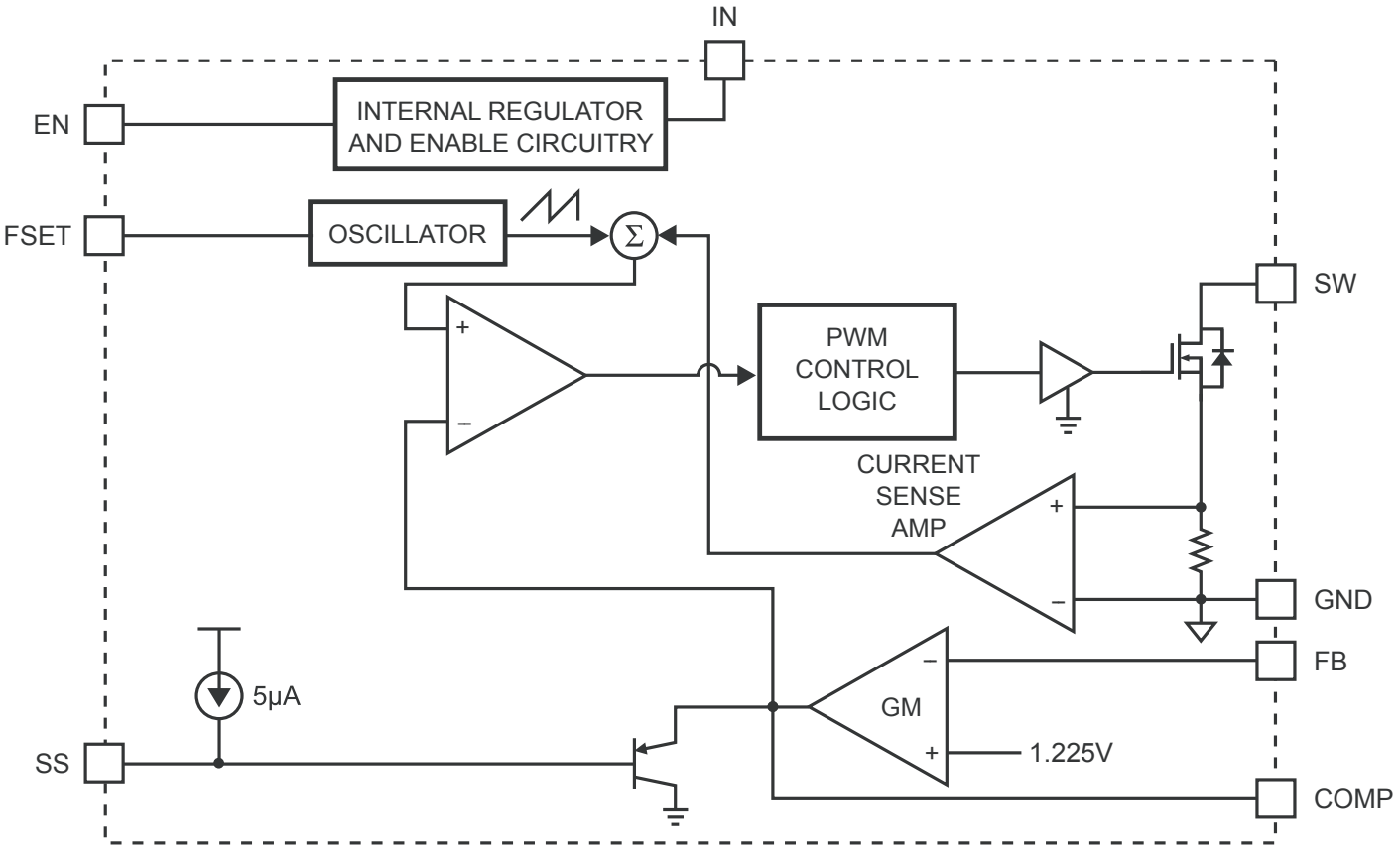



**Figure 1—Function Block Diagram**

# APPLICATION INFORMATION

**Components referenced below apply to the "*Typical Application Circuit*".**

### Theory of Operation

The MP3425 uses a constant frequency, peak current mode boost regulation architecture to regulate the feedback voltage. The operation of the MP3425 can be understood by referring to the block diagram of Functional.

At the beginning of each cycle, the N-Channel MOSFET switch is turned on, forcing the inductor current to rise. The current at the source of the switch is internally measured and converted to a voltage by the current sense amplifier. That voltage is compared to the error voltage at comp. The voltage at the output of the error amplifier is an amplified version of the difference between the 1.225V reference voltage and the feedback voltage.

When theses two voltages are equal, the PWM comparator turns off the switch forcing the inductor current to the output capacitor through the external rectifier. This causes the inductor current to decrease. The peak inductor current is controlled by the voltage at COMP, which in turn is controlled by the output voltage. Thus the output voltage is regulated by the inductor current to satisfy the load. The use of current mode regulation improves the transient response and control loop stability.

### Selecting the Switching Frequency

The switching frequency is set by R5. The equation is:

$$F_{SET} = 23 \times \left(R5^{-0.86}\right)$$

Where R5 is in kΩ, $F_{SET}$ is in MHz.

### UVLO Hysteresis

The MP3425 features a programmable UVLO hysteresis. Upon power up a 4μA current sink is applied to the resistor divider attached to the EN pin. This means that on power up VIN must increase by an extra amount to overcome the current sink. That extra amount is the current sink times the resistor from VIN to EN. Once the EN pin reaches about 1.5V the current sink will turn off to create the reverse hysteresis for VIN falling:

$$UVLOHysteresis = 4\mu A \times R_{TOP}$$

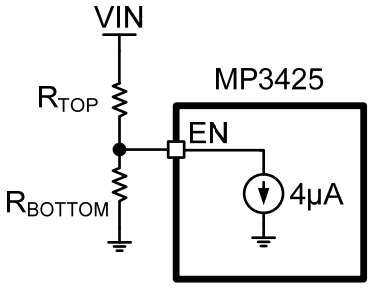



**Table1—Frequency Selection**

| R5 (kΩ) | Freq (MHz) |
|---|---|
| 180 | 0.26 |
| 160 | 0.29 |
| 150 | 0.31 |
| 143 | 0.32 |
| 66.5 | 0.62 |
| 35.7 | 1.06 |
| 25 | 1.44 |
| 18 | 1.91 |
| 16 | 2.12 |
| 14 | 2.37 |

### Selecting the Soft-Start Capacitor

The MP3425 includes a soft-start timer that limits the voltage at COMP during startup to prevent excessive current at the input. This prevents premature termination of the source voltage at startup due to input current overshoot. When power is applied to the MP3425, and enable is asserted, a 5μA internal current source charges the external capacitor at SS. As the SS capacitor is charged, the voltage at SS rises. When the SS voltage reaches 250mV, the MP3425 starts switching at ¼ of the programmed frequency (frequency fold back mode). At 800mV the switching frequency becomes the programmed value. The soft-start ends when the voltage at SS reaches 2.5V. This limits the inductor current at start-up, forcing the input current to rise slowly to the current required to regulate the output voltage.

The soft-start period is determined by the equation:

$$t_{SS} = \frac{C_{SS} \times 10^{-9} \times 2.5V}{5\mu A}$$

Where $C_{SS}$ (nF) is the soft-start capacitor from SS to GND, and $t_{SS}$ is the soft-start period.

**Setting the Output Voltage**

This is the actual output voltage. It is fed back through two sense resistors in series. The feedback voltage is 1.225V typical. The equation to the output voltage is:

$$V_{OUT} = V_{REF} \times (1 + \frac{R2}{R3})$$

Where:
R2 is the top feedback resistor
R3 in the bottom feedback resistor
$V_{REF}$ is the reference voltage (1.225V typical)

Choose the feedback resistors to be in the 10k or higher range for good efficiency.

**Selecting the Input Capacitor**

An input capacitor is required to supply the AC ripple current to the inductor, while limiting noise at the input source. A low ESR capacitor is required to keep the noise at the IC to a minimum. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

Use an input capacitor value greater than 4.7μF. The capacitor can be electrolytic, tantalum or ceramic. However since it absorbs the input switching current it requires an adequate ripple current rating. Use a capacitor with a RMS current rating greater than the inductor ripple current (see "Selecting The Inductor" to determine the inductor ripple current).

To insure stable operation place the input capacitor as close to the IC as possible. Alternately a smaller high quality ceramic 0.1 μF capacitor may be placed closer to the IC with the larger capacitor placed further away. If using this technique, it is recommended that the larger capacitor be a tantalum or electrolytic type. All ceramic capacitors should be placed close to the MP3425.

**Selecting the Output Capacitor**

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple to a minimum. The characteristic of the output capacitor also affects the stability of the regulation control system. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. In the case of ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated to be:

$$V_{RIPPLE} \cong \frac{(1 - \frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times F_{SW}}$$

Where Vripple is the output ripple voltage, Vin and Vout are the DC input and output voltages respectively, Iload is the load current, Fsw is the switching frequency, and $C_{OUT}$ is the capacitance of the output capacitor.

In the case of tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, and so the output ripple is calculated as:

$$V_{RIPPLE} \cong \frac{(1 - \frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times F_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}}$$

Where $R_{ESR}$ is the equivalent series resistance of the output capacitors.

Choose an output capacitor to satisfy the output ripple and load transient requirements of the design. A 4.7μF – 22μF ceramic capacitor is suitable for most applications.

**Selecting the Inductor**

The inductor is required to force the higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current that results in lower peak inductor current, reducing stress on the internal N-Channel switch. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturations current.

A good rule of thumb is to allow the peak-to-peak ripple current to be approximately 30-50% of the maximum input current. Make sure that the peak inductor current is below 75% of the current limit at the operating duty cycle to prevent loss of regulation due to the current limit. Also make sure that the inductor does not saturate under the worst-case load transient and startup conditions. Calculate the required inductance value by the equation:

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times F_{SW} \times \Delta I}$$

$$I_{IN(max)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta}$$

Where :
$I_{LOAD}$(max) is the maximum load current
ΔI is the peak-to-peak inductor ripple current
ΔI = (30% - 50%) x $I_{IN\ (MAX)}$
η is efficiency.

**Selecting the Diode**

The output rectifier diode supplies current to the inductor when the internal MOSFET is off. To reduce losses due to diode forward voltage and recovery time, use a Schottky diode with the MP3425. The diode should be treated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current.

**Compensation**

The output of the transconductance error amplifier (COMP) is used to compensate the regulation control system. The system uses two poles and one zero to stabilize the control loop. The poles are $F_{P1}$ set by the output capacitor $C_{OUT}$ and the load resistance, and $f_{P2}$ start from origin, the zero fz1 set by the compensation capacitor $C_{COMP}$ and the compensation resistor $R_{COMP}$. These are determined by the equations:

$$F_{P1} = \frac{1}{2 \times \Pi \times R_{LOAD} \times C_{OUT}} \quad (Hz)$$

$$F_{P2} = \frac{G_{EA}}{2 \times \Pi \times A_{VEA} \times C_{COMP}} \quad (Hz)$$

$$F_{Z1} = \frac{1}{2 \times \Pi \times R_{COMP} \times C_{COMP}} \quad (Hz)$$

Where $R_{LOAD}$ is the load resistance, $G_{EA}$ is the error amplifier transconductance, and $A_{VEA}$ is the error amplifier voltage gain.

The DC loop gain is

$$A_{VDC} = \frac{A_{VEA} \times V_{IN} \times R_{LOAD} \times V_{FB} \times G_{CS}}{0.5 \times V_{OUT}^{2}} \quad (V/V)$$

Where $G_{CS}$ is the compensation voltage to inductor current gain, and the $V_{FB}$ is the feedback regulation threshold.

There is also a right-half-plane zero ($F_{RHPZ}$) that exists in continuous conduction mode (inductor current does not drop to zero on each cycle) step-up converters. The frequency of the right half plane zero is:

$$F_{RHP} = \frac{R_{LOAD}}{2 \times \Pi \times L} \times (\frac{V_{IN}}{V_{OUT}})^2 \quad (Hz)$$

The “Component Selection” table lists generally recommended compensation components for different input voltages, output voltages and capacitances of most frequently used output ceramic capacitors. Ceramic capacitors have extremely low ESR, therefore the second compensation capacitor (from COMP to GND) is not required.

**Table 2—Component Selection**

| $V_{IN}$ (V) | $V_{OUT}$ (V) | $C_{OUT}$ (µF) | Rcomp (kΩ) | Ccomp (nF) | Switching Frequency (kHz) | Inductor (µH) |
|---|---|---|---|---|---|---|
| 3 | 12 | 4.7 | 10 | 6.8 | 600 | 8.2 |
| 3 | 12 | 10 | 15 | 6.8 | 600 | 8.2 |
| 3 | 12 | 22 | 30 | 6.8 | 600 | 8.2 |
| 5 | 12 | 10 | 12 | 4.9 | 600 | 6.8 |
| 5 | 12 | 22 | 25 | 4.9 | 600 | 6.8 |
| 5 | 18 | 4.7 | 12 | 4.9 | 600 | 10 |
| 5 | 18 | 10 | 25 | 4.9 | 600 | 10 |
| 5 | 18 | 22 | 50 | 4.9 | 600 | 10 |
| 12 | 24 | 4.7 | 10 | 6.8 | 600 | 10 |
| 12 | 24 | 10 | 20 | 6.8 | 600 | 10 |
| 12 | 24 | 22 | 40 | 6.8 | 600 | 10 |
| 12 | 48 | 4.7 | 30 | 4.7 | 600 | 33 |
| 12 | 48 | 10 | 60 | 4.7 | 600 | 33 |
| 12 | 48 | 22 | 60 | 10 | 600 | 33 |

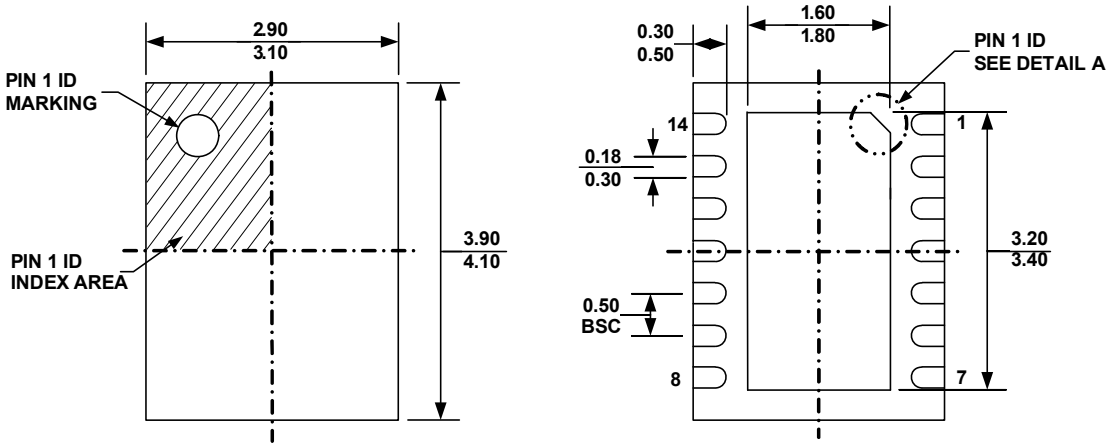
For faster control loop and better transient response, set the capacitor C7 to the recommended value in the table. Then slowly increase the resistor R6 and check the load step response on a bench to make sure the ringing and overshoot on the output voltage at the edge of the load steps is minimal. Finally, the compensation needs to be checked by calculating the DC loop gain and the crossover frequency. The crossover frequency where the loop gain drops to 0dB (a gain of 1) can be obtained visually by placing a -20dB/decade slope at each pole, and a +20dB/decade slope at each zero. The crossover frequency should be at least one decade below the frequency of the right-half-plane zero at maximum output load current to obtain high enough phase margin for stability.

**Layout Considerations**

High frequency switching regulators require very careful layout for stable operation and low noise. All components must be placed as close to the IC as possible. Keep the path between L1, D1, and $C_{OUT}$ extremely short for minimal noise and ringing. $C_{IN}$ must be placed close to the IN pin for best decoupling. All feedback components must be kept close to the FB pin to prevent noise injection on the FB pin trace. The ground return of $C_{IN}$ and $C_{OUT}$ should be tied close to the GND pin. See the MP3425 demo board layout for reference.

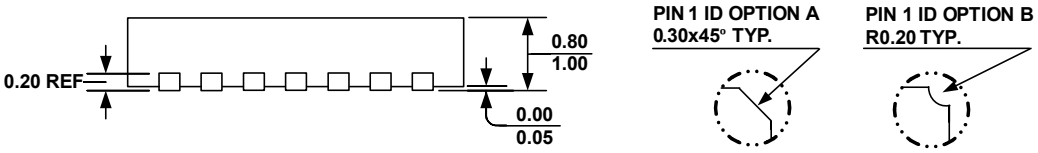
# PACKAGE INFORMATION

## QFN-14 (3mmx4mm)



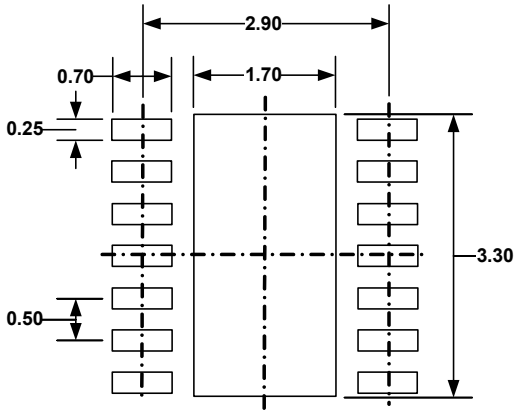

TOP VIEW

BOTTOM VIEW




SIDE VIEW

DETAIL A




RECOMMENDED LAND PATTERN

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETER MAX
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE