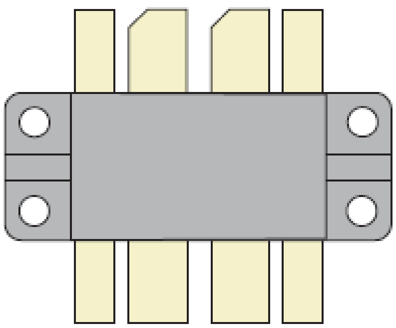
ARF475FL

500 V, 900 W, 128 MHz RF Power MOSFET

Product Overview

The ARF475FL is a matched pair of RF power transistors in a common source configuration in a T3A package. It is designed for high-voltage push-pull or parallel operation in narrow band ISM and MRI power amplifiers up to 128 MHz.



Features

- Specified 500 V, 128 MHz characteristics:
  - Output power = 900 W peak
  - Gain = 15 dB (Class AB)
  - Efficiency = 50% minimum
- High-performance push-pull RF package
- High-voltage breakdown and large SOA for superior ruggedness
- Low thermal resistance
- RoHS compliant

1. Device Specifications

This section shows the specifications of the ARF475FL device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the ARF475FL device. T_C = 25 °C unless otherwise specified.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-source voltage	500	V
V_{DGO}	Drain-gate voltage	500	
I_D	Continuous drain current	10	A
V_{GS}	Gate-source voltage	±30	V
P_D	Total power dissipation (per side)	910	W
T_J, T_{STG}	Operating and storage junction temperature range	–55 to 175	°C
T_L	Lead temperature: 0.063" from case for 10 seconds	300	

1.2 Electrical Performance

The following table shows the static characteristics of the ARF475FL device. T_C = 25 °C unless otherwise specified.

Table 1-2. Static Characteristics

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 μA	500			V
$V_{DS(ON)}$	On-state drain voltage[1]	$I_{D(ON)}$ = 5 A, V_{GS} = 10 V		2.9	4	
I_{DSS}	Zero-gate voltage drain current	V_{DS} = V_{DSS}, V_{GS} = 0 V			100	μA
		V_{DS} = 50 V, V_{GS} = 0 V, T_C = 125 °C			500	
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 5 A	4.2	5.1		S
g_{fs1}/g_{fs2}	Forward transconductance match ratio	V_{DS} = 15 V, I_D = 5 A	0.9		1.1	S
$V_{GS(th)}$	Gate-source threshold voltage	V_{DS} = V_{GS}, I_D = 200 mA	2	3.3	4	V
$DV_{GS(th)}$	Gate threshold voltage match	V_{DS} = V_{GS}, I_D = 200 mA			0.2	V

Note:

1. Pulse test: Pulse width < 380 μs, Duty Cycle < 2%.

The following table shows the thermal characteristics of the ARF475FL device.

Table 1-3. Thermal Characteristics (per side)

Symbol	Characteristic	Min	Typ	Max	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance		0.15	0.165	°C/W
$R_{\theta JHS}$	Junction-to-sink thermal resistance (Use high-efficiency thermal grease and planar heat sink surface.)		0.30	0.33	

The following table shows the dynamic characteristics of the ARF475FL device. T_C = 25 °C unless otherwise specified.

Table 1-4. Dynamic Characteristics (per Section)

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz		740	830	pF
C_{oss}	Output capacitance			125	130	
C_{rss}	Reverse transfer capacitance			7	9	
$t_{d(on)}$	Turn-on delay time	V_{GS} = 15 V, V_{DD} = 250 V, I_D = $I_{D[Cont.]}$ at 25 °C, R_g = 1.6 Ω		5.1	10	ns
t_r	Rise time			4.1	8	
$t_{d(off)}$	Turn-off delay time			12	18	
t_f	Fall time			4.0	7	

The following table shows the functional characteristics of the ARF475FL device. T_C = 25 °C unless otherwise specified.

Table 1-5. Functional Characteristics (Push-Pull Configuration)

Parameter	Characteristic	Test Conditions	Min	Typ	Max	Unit
G_{PS}	Common source amplifier power gain	f = 128 MHz, V_{DD} = 150 V, I_{DQ} = 15 mA, P_{out} = 900 W, PW = 3 ms, 10% duty cycle	14	16		dB
η	Drain efficiency		50	55		%
Ψ	Electrical ruggedness VSWR 5:1		No degradation in output power			

1.3 Typical Performance Curves

This section shows the typical performance curves of the ARF475FL device per transistor section unless otherwise specified.

Figure 1-1. Output Characteristics

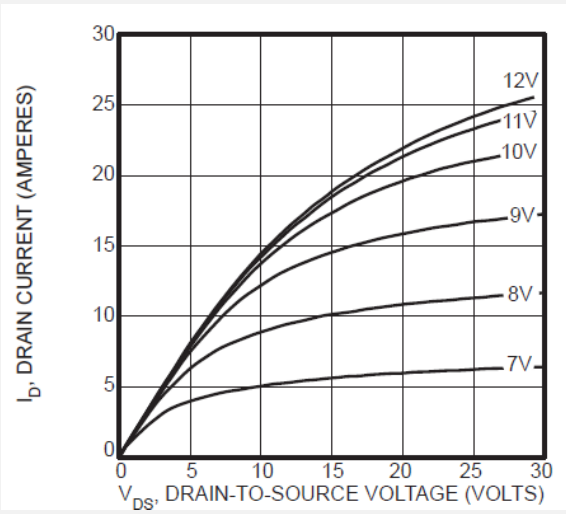


Figure 1-2. Capacitance vs. Drain-to-Source Voltage

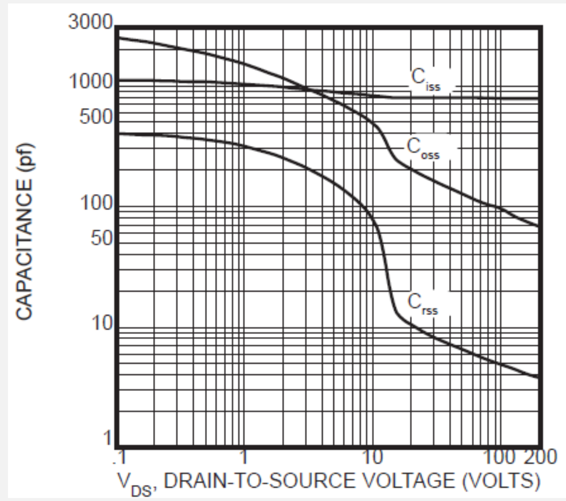


Figure 1-3. Transfer Characteristics

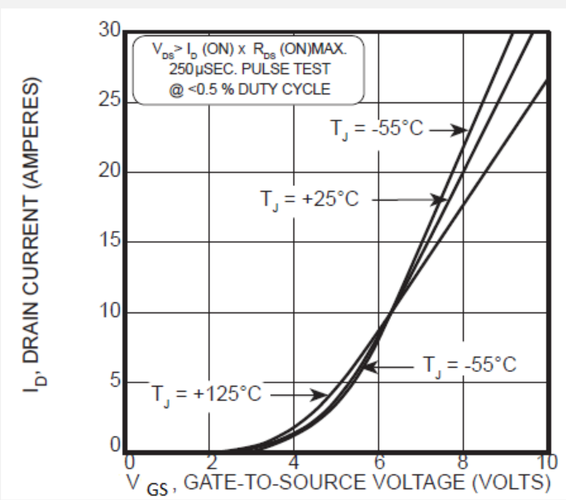


Figure 1-4. Threshold Voltage vs. Temperature

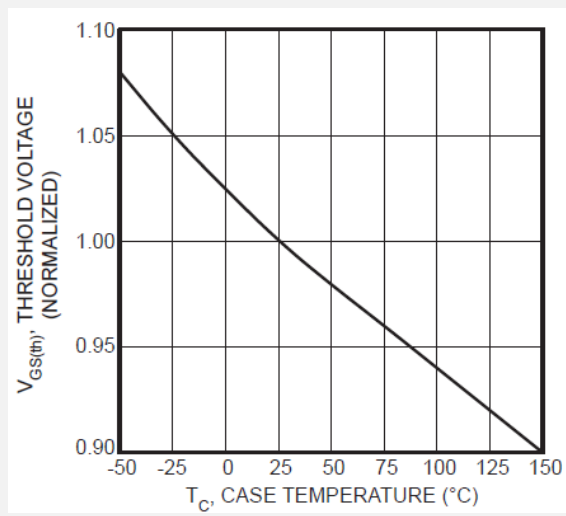


Figure 1-5. Maximum Effective Transient Thermal Impedance Junction-to-Case vs. Pulse Duration

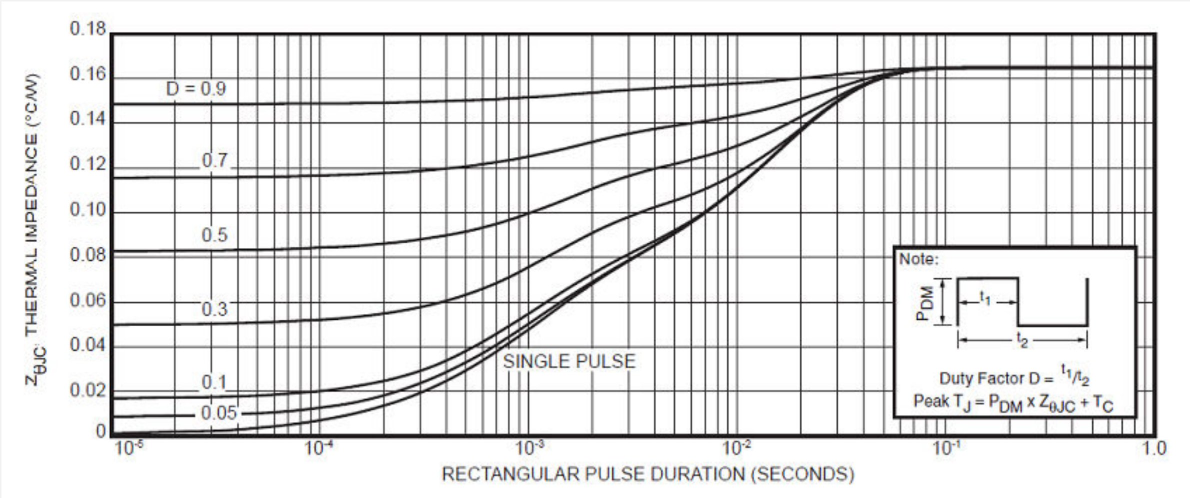


Figure 1-6. Transient Thermal Impedance Model

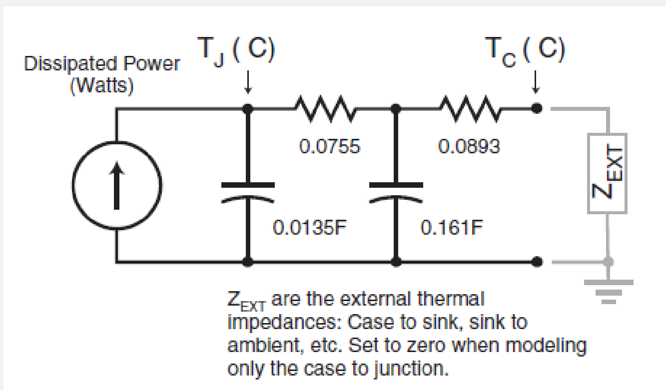
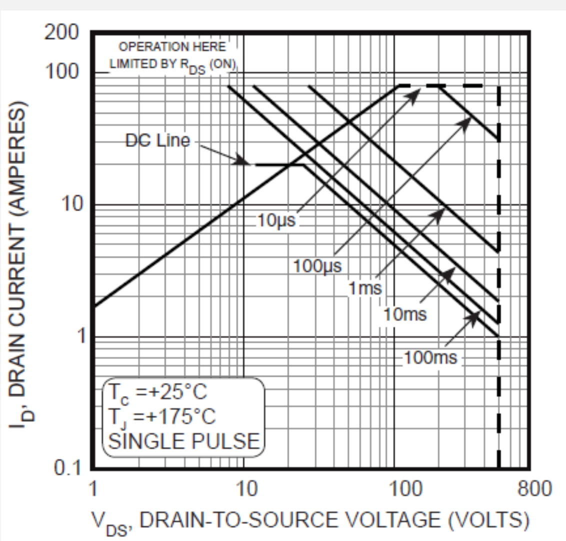


Figure 1-7. Maximum Safe Operating Area



The following table shows the typical Class AB large signal input-output impedance for the ARF475FL device.

Table 1-6. Typical Class AB Large Signal Input–Output Impedance

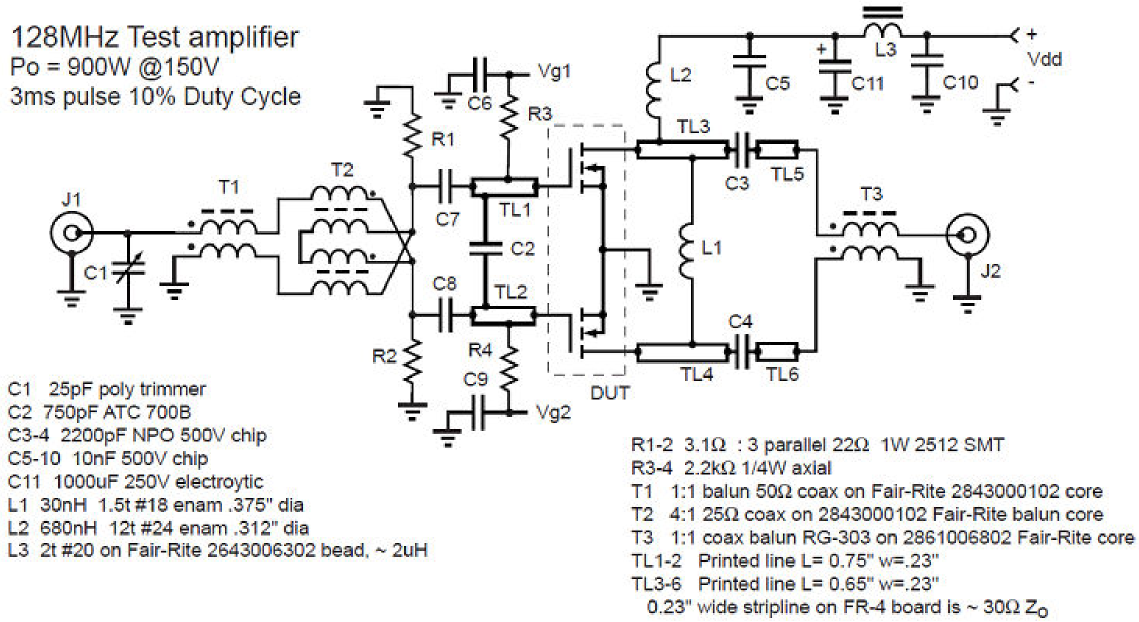
Frequency (MHz)	Z_{in} (Ω) Gate-to-Gate	Z_{out} (Ω) Drain-to-Drain
30	5.2 – j 10	41 – j 20
60	1.37 – j 5.2	26 – j 25
90	0.53 – j 2.6	16 – j 23
120	0.25 – j 1.0	10 – j 20
150	0.25 + j 0.2	6.7 – j 17

Notes:
- Z_{in} — Gate shunted with 25 Ω
- I_{DQ} = 15 mA each side
- Z_{out} — Conjugate of optimum load for 600 W peak output at V_{dd} = 150 V, 25% duty cycle and PW = 5 ms

2. Test Circuits

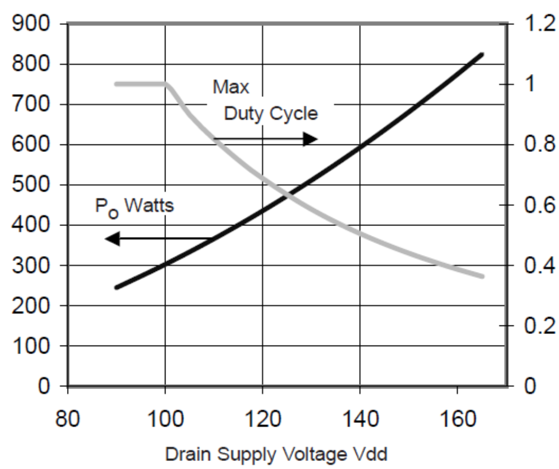
The following figure shows the test circuits of the ARF475FL device.

Figure 2-1. 128 MHz Test Circuit



The following image shows the peak output power versus V_{dd} and duty cycle.

Figure 2-2. Peak Output Power vs. V_{dd} and Duty Cycle



Note: The value of L1 must be adjusted as the supply voltage is changed to maintain resonance in the output circuit. At 128 MHz its value changes from approximately 40 nH at 100 V, to 30 nH at 150 V.
With the 50 Ω drain-to-drain load, the duty cycle above 100 V must be reduced to ensure power dissipation is within the limits of the device. Maximum pulse length should be 100 ms or less.

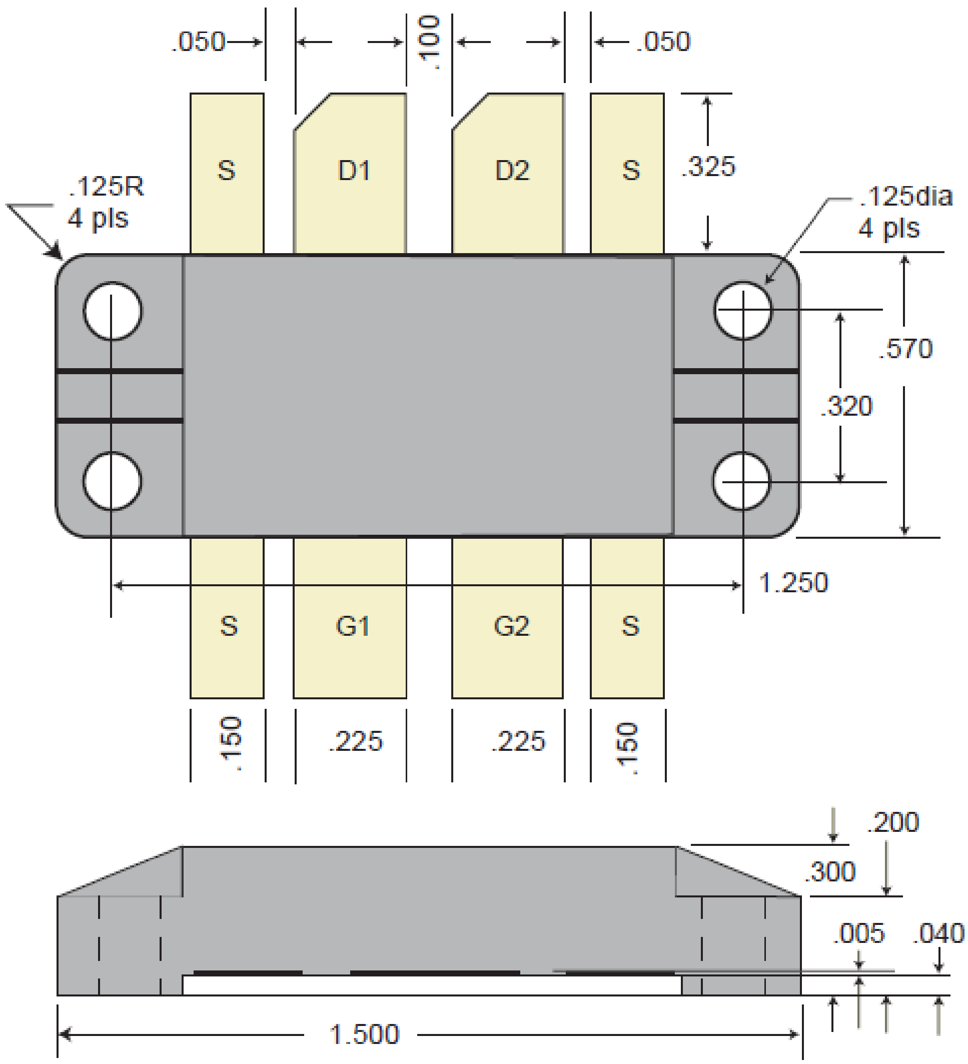
3. Package Specification

This section shows the package specification of the ARF475FL device.

3.1 Package Outline Drawing

The following figure illustrates the package outline of the ARF475FL device.

Figure 3-1. T3A Package Outline



Note: Hazardous Material Warning!
The white ceramic portion of the device between leads and mounting flange is beryllium oxide. Beryllium oxide dust is highly toxic when inhaled. Care must be take during handling and mounting to avoid damage to this area. These devices must never be thrown away with general industrial or domestic waste.

Note: These devices are sensitive to electrostatic discharge. Proper handling procedures should be followed.

Thermal Considerations and Package Mounting

The rated power dissipation is only available when the package mounting surface is at 25 °C and the junction temperature is 175 °C. The thermal resistance between junctions and case mounting surface is 0.16 °C/W. When installed, an additional thermal impedance of 0.15 °C/W between the package base and the mounting surface is typical. Ensure that the mounting surface is smooth and flat. Thermal joint compound must be used to reduce the effects of small surface irregularities. Use the minimum amount necessary to coat the surface. The heat sink should incorporate a copper heat spreader to obtain best results.

The package design clamps the ceramic base to the heat sink. A clamped joint maintains the required mounting pressure while allowing for thermal expansion of both the base and the heat sink. Four 4-40 (M3) screws provide the required mounting force. T = 2.5 - 3.5 in-lb (0.28 - 0.40 N-m).

4. Revision History

Table 4-1. Revision History

Revision	Date	Description
A	02/2022	• Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00004435A,which replaces the previous Microsemi literature number 050-4929. • Changed g_{fs} minimum value from 3 to 4.2 and typical from 3.6 to 5.1 (changed unit from MHOS to S).
Initial releases (Microsemi Revisions A through E)	02/2006 – 12/2010	Previous releases.

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